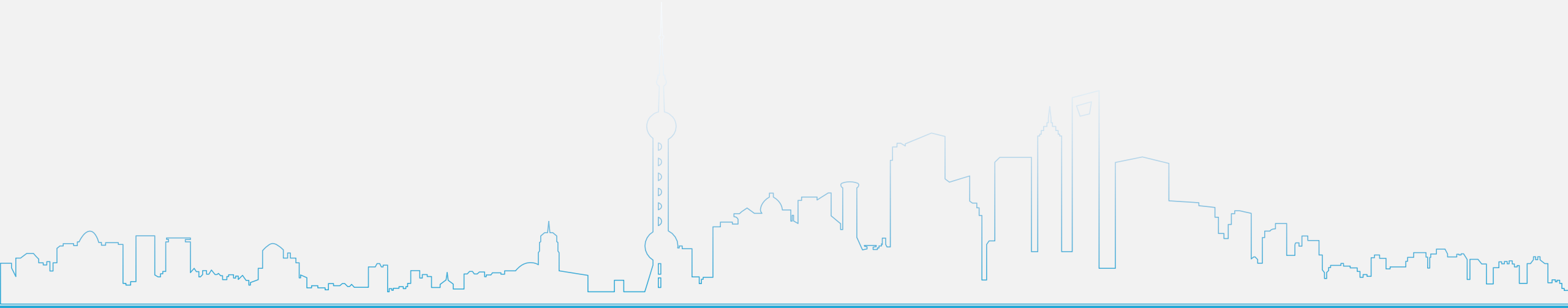


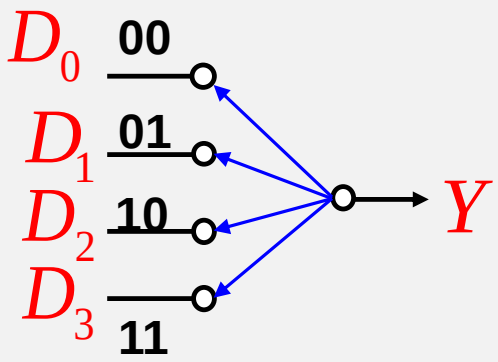
第四章　组合逻辑电路设计（二）

秦磊华　计算机学院

4.7 多路选择器 (Multiplexer)设计

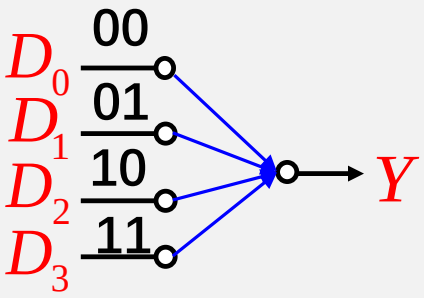
1.多路选择器的基本功能

从一组输入数据中，选择出某一个数据，完成这种功能的逻辑电路称作数据选择器（或称为多路选择开关）



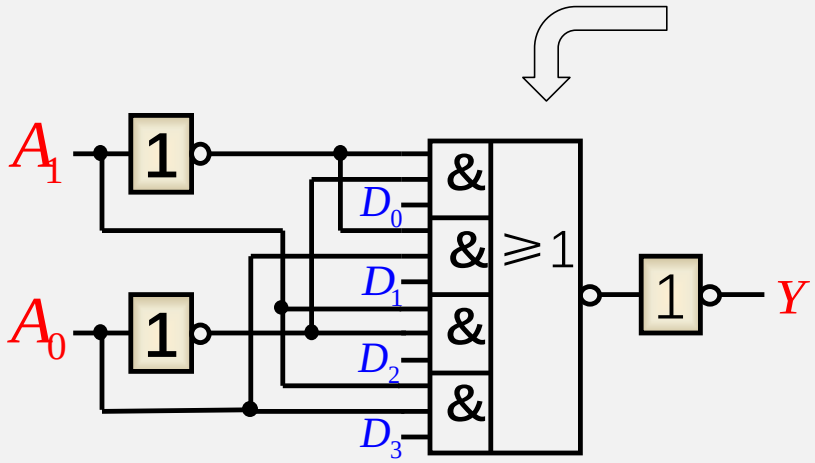
4.7 多路选择器(Multiplexer)设计

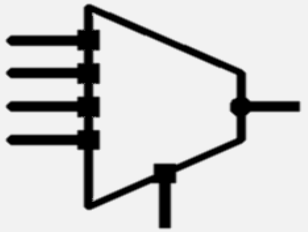
2. 4路数据选择器的设计 (MUX)



A_1	A_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

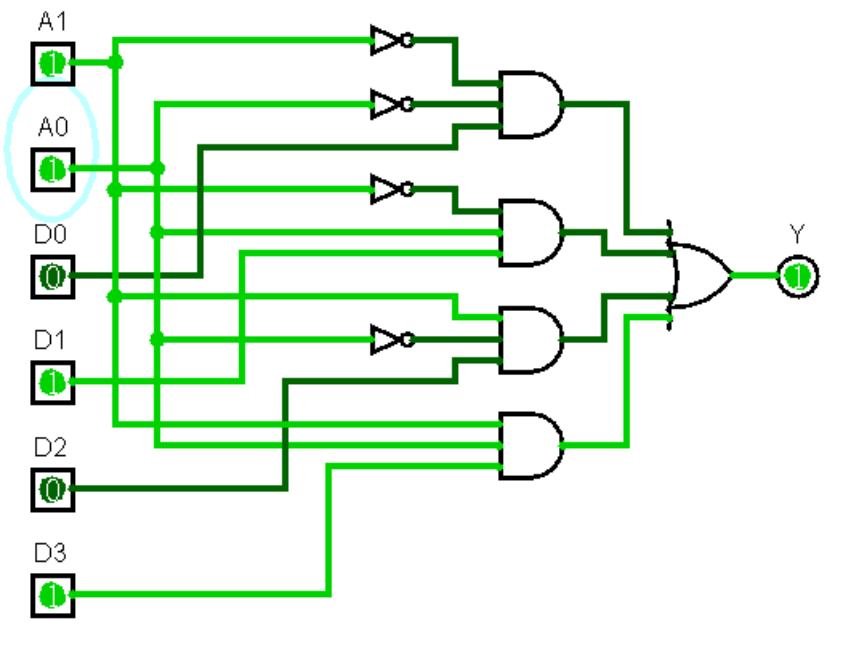
$$Y = \overline{A}_1 \overline{A}_0 D_0 + \overline{A}_1 A_0 D_1 + A_1 \overline{A}_0 D_2 + A_1 A_0 D_3$$





4.7 多路选择器(Multiplexer)设计

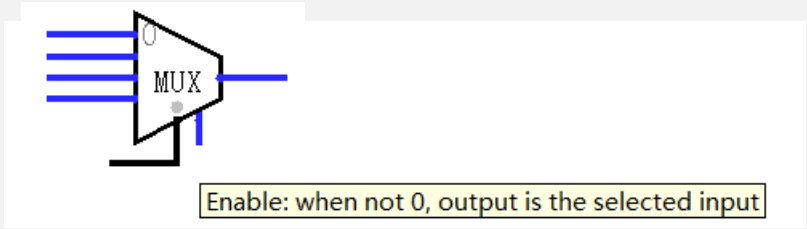
$$Y = \overline{A}_1 \overline{A}_0 D_0 + \overline{A}_1 A_0 D_1 + A_1 \overline{A}_0 D_2 + A_1 A_0 D_3$$



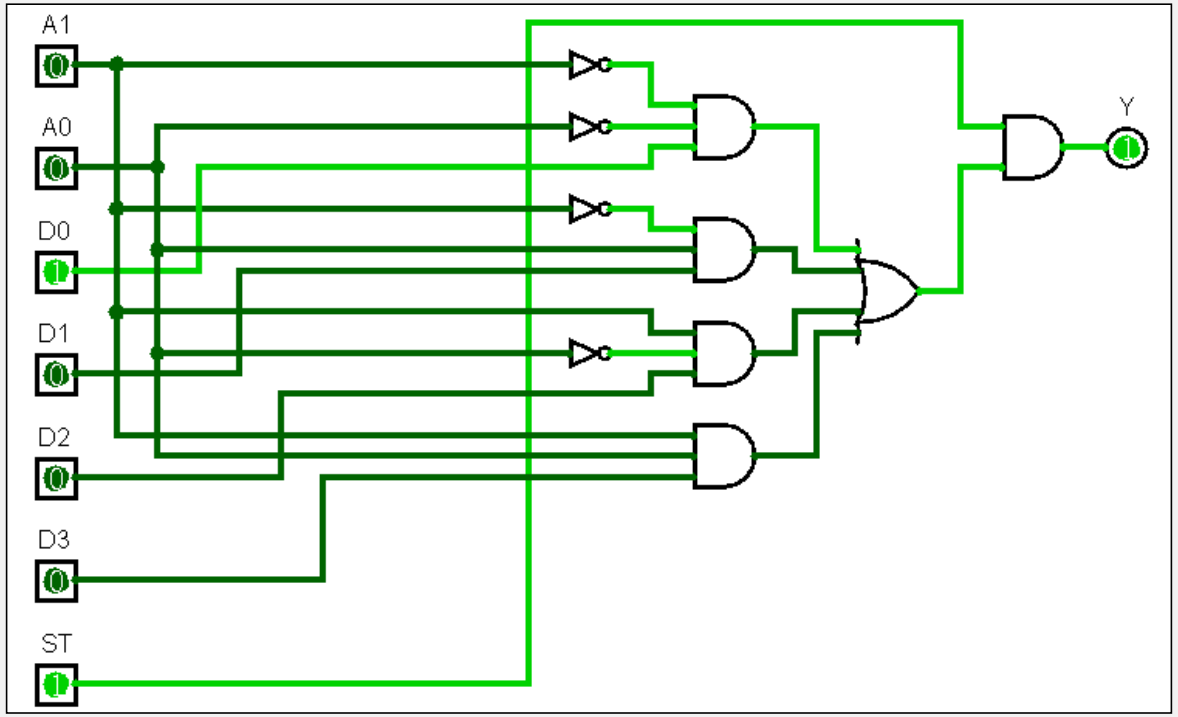
4.7 多路选择器(Multiplexer)设计

$\overline{ST}_1$	A_1	A_0	Y_1
1	X	X	0
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3

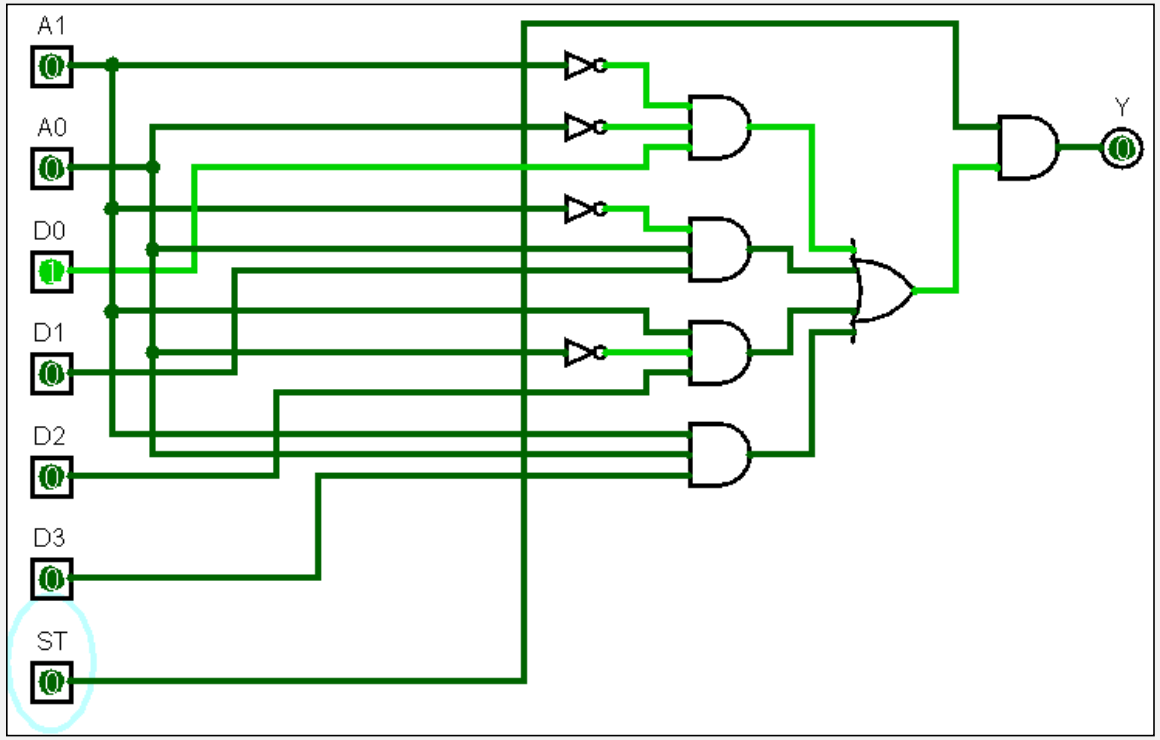
$$Y = \overline{\overline{ST_1}}(\overline{A_1}\,\overline{A_0}D_0 + \overline{A_1}A_0D_1 + A_1\overline{A_0}D_2 + A_1A_0D_3)$$



4.7 多路选择器(Multiplexer)设计



$\overline{ST}_1$	A_1	A_0	Y_1
1	X	X	0
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3



4.7 多路选择器(Multiplexer)设计

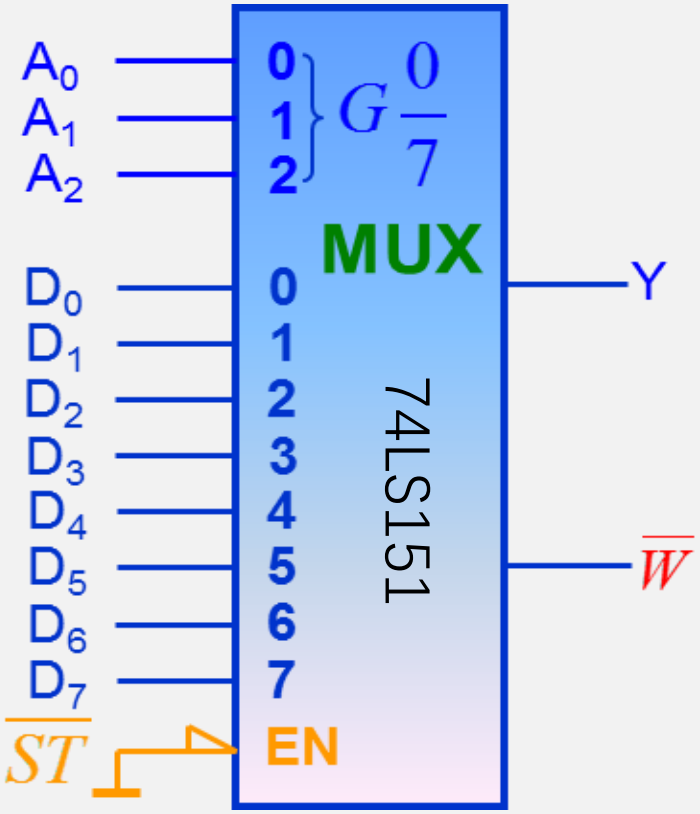
3.带使能和可扩展功能的8路数据选择器设计

$\overline{ST}$	A_2	A_1	A_0	Y	$\overline{W}$
1	X	X	X	0	1
0	0	0	0	D_0	$\overline{D_0}$
0	0	0	1	D_1	$\overline{D_1}$
0	0	1	0	D_2	$\overline{D_2}$
0	0	1	1	D_3	$\overline{D_3}$
0	1	0	0	D_4	$\overline{D_4}$
0	1	1	1	D_5	$\overline{D_5}$
0	1	0	0	D_6	$\overline{D_6}$
0	1	1	1	D_7	$\overline{D_7}$

$\overline{ST}$：选通端，低有效。

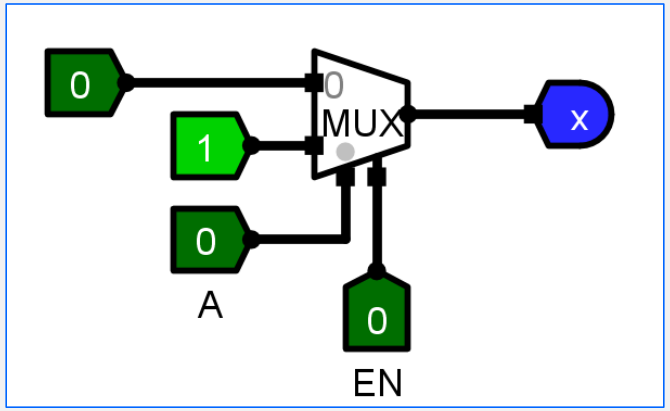
Y,$\overline{W}$：互补输出端。

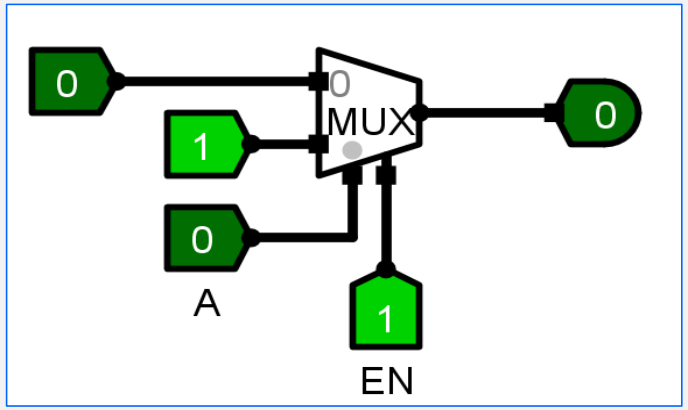
可参照4路选择器写出Y逻辑表达式

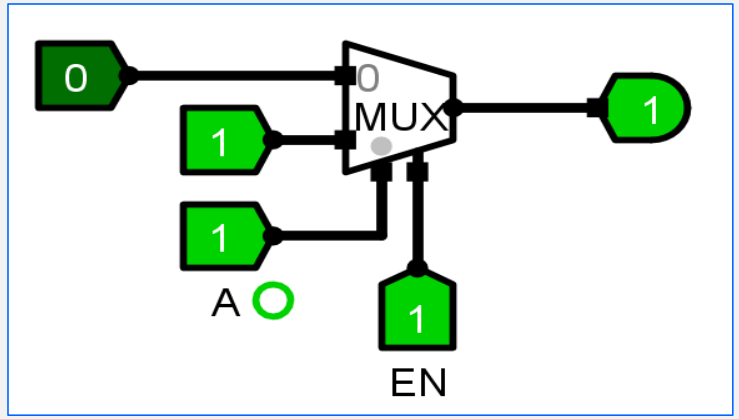


$$Y= \overline{A}_2\overline{A}_1\overline{A}_0 D_0+ \overline{A}_2\overline{A}_1A_0 D_1 + \overline{A}_2A_1\overline{A}_0 D_2 + \overline{A}_2A_1A_0 D_3 + A_2\overline{A}_1\overline{A}_0 D_4 + A_2\overline{A}_1A_0 D_5 + A_2A_1\overline{A}_0 D_6 + A_2A_1A_0 D_7$$

4.7 多路选择器(Multiplexer)设计

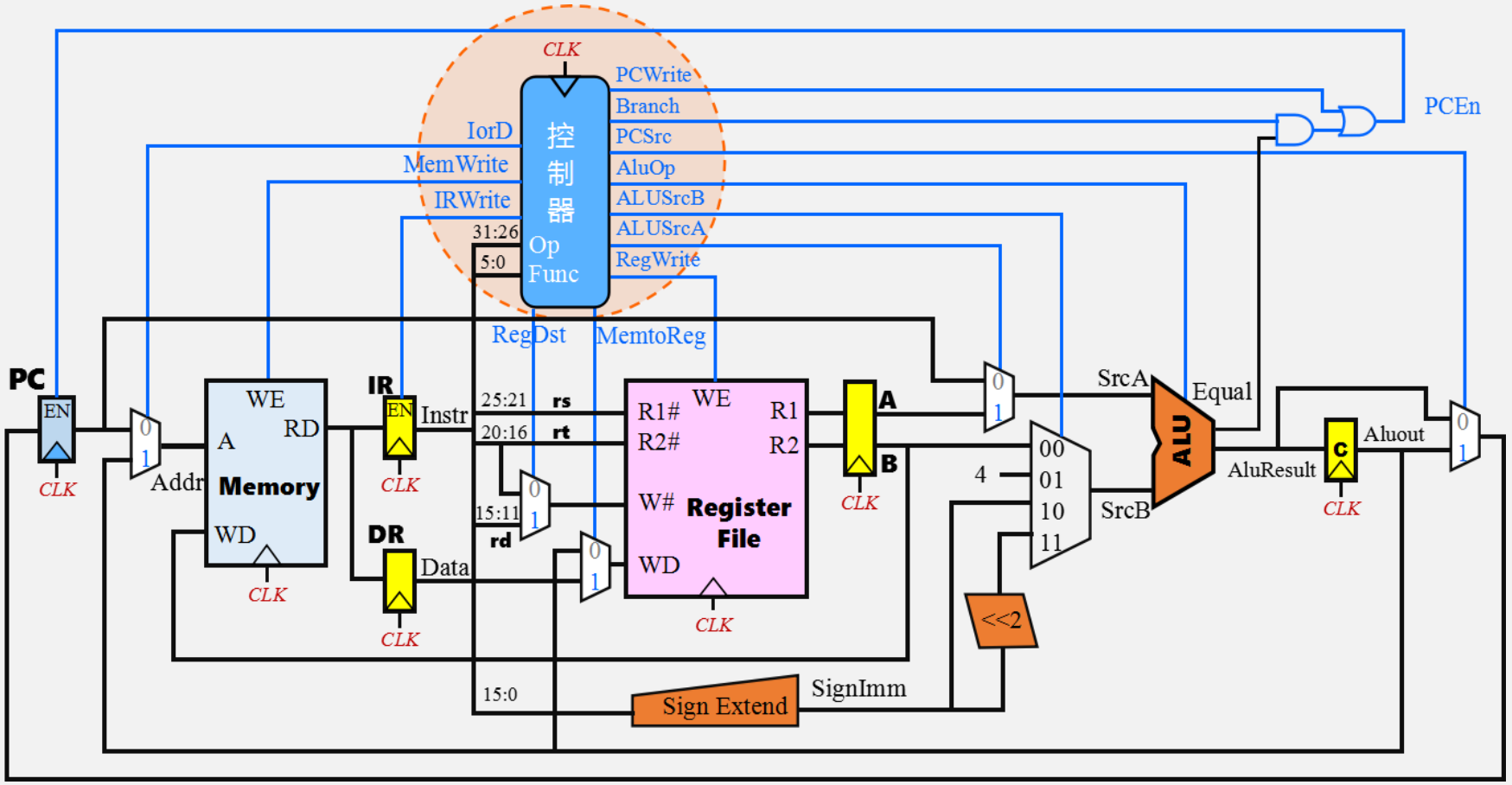






4.7 多路选择器(Multiplexer)设计

4.数据选择器的应用

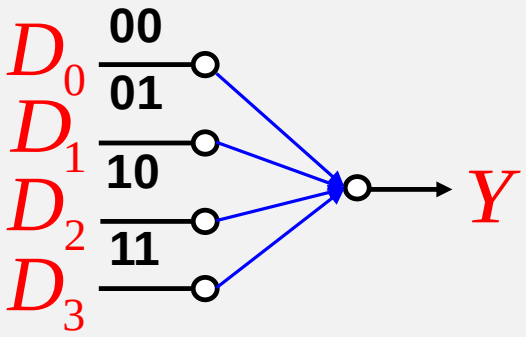


同一目标有多个数据来源时，在其入口处需使用多路选择器

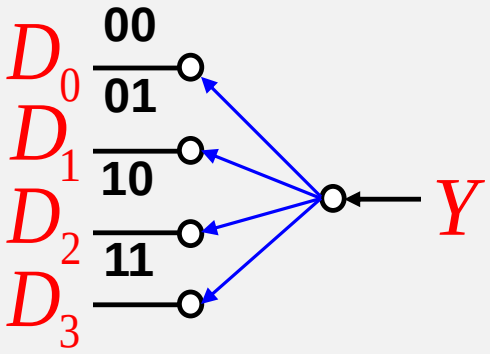
4.8 多路分配器(解复用器 Demultiplexer)

1.多路分配器的基本功能

将1个输入数据，根据需要传送到m个输出端的任何一个输出端的电路，称为数据分配器、多路分配器或解复用器，其逻辑功能正好与多路选择器相反。



MUX



DMX

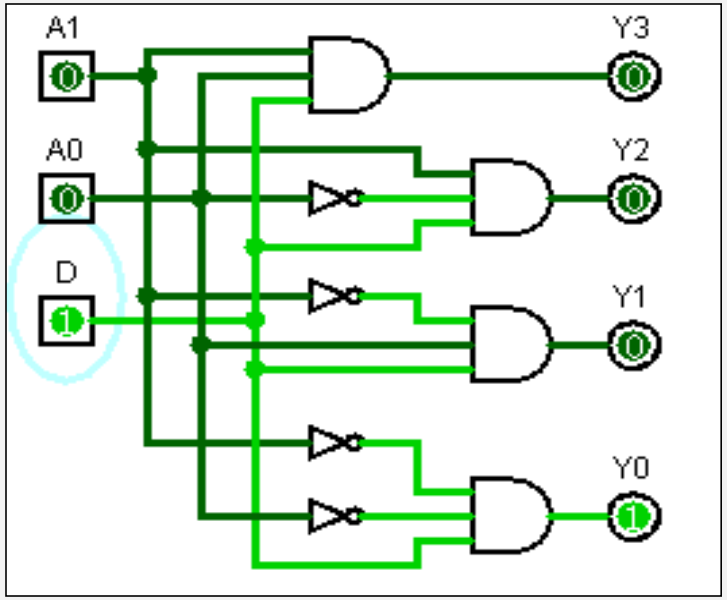
4.8 多路分配器(解复用器 Demultiplexer)

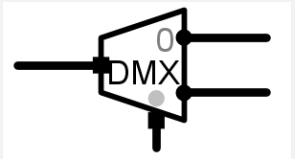
2.多路分配器的设计

A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	D
0	1	0	0	D	0
1	0	0	D	0	0
1	1	D	0	0	0

$$Y_0 = \overline{A_1}\,\overline{A_0}D \qquad Y_1 = \overline{A_1}A_0D$$

$$Y_2 = A_1\overline{A_0}D \qquad Y_3 = A_1A_0D$$

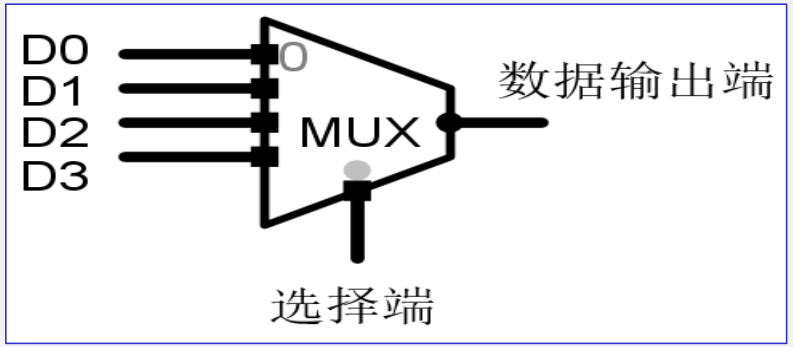


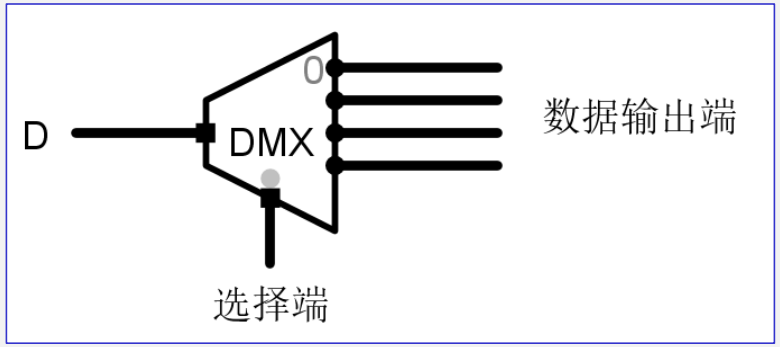


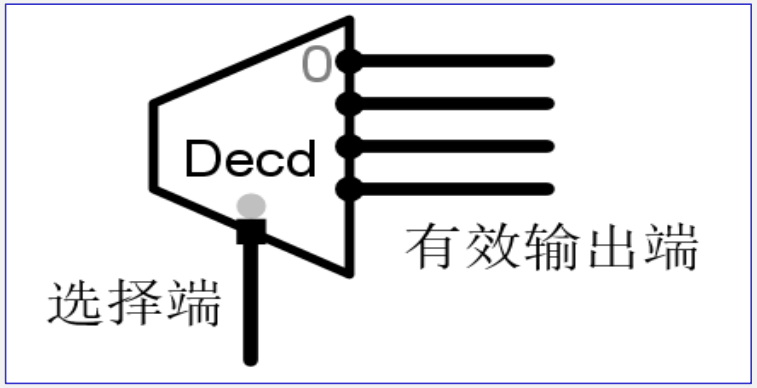
A_1	A_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

多路选择器真值表

4.9 多路选择器、多路分配器、译码器比较







4.10 基于基本组合逻辑功能部件的组合逻辑设计

1.利用变量译码器实现组合逻辑函数

A_1	A_0	Y3	Y2	Y1	Y0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$Y_3 = A_1A_0$　$Y_2 = A_1\bar{A}_0$

$Y_1 = \bar{A}_1A_0$　$Y_0 = \bar{A}_1\bar{A}_0$

一个n变量输入的变量译码器，其输出包含了n个输入变量的全部最小项。用n变量译码器加输出门就能实现任何形式的输入变量不大于n 的组合逻辑函数。

4.10 基于基本组合逻辑功能部件的组合逻辑设计

例1 用译码器实现一组多输出函数

$$F_1 = A\overline{B} + \overline{B}C + AC$$
$$F_2 = \overline{A}\overline{B} + B\overline{C} + ABC$$
$$F_3 = \overline{A}C + BC + A\overline{C}$$

解：三输入变量的多输出函数，用3-8译码器实现

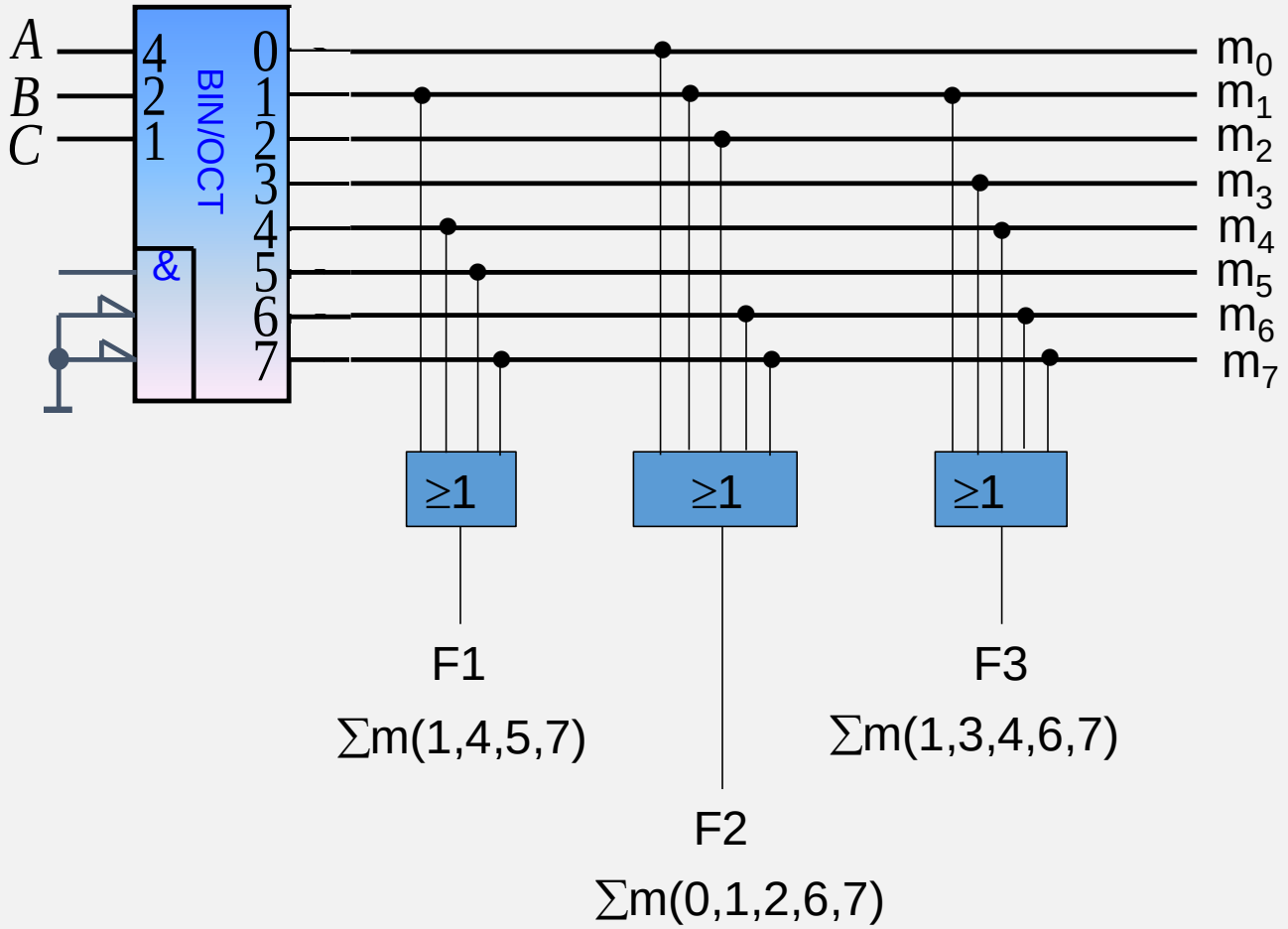
将多输出函数写成最小项之和形式,再配合适当的逻辑门即可。

$$F_1 = A\overline{B} + \overline{B}C + AC = \sum m(1,4,5,7)$$

$$F_2 = \overline{A}\overline{B} + B\overline{C} + ABC = \sum m(0,1,2,6,7)$$

$$F_3 = \overline{A}C + BC + A\overline{C} = \sum m(1,3,4,6,7)$$

4.10 基于基本组合逻辑功能部件的组合逻辑设计



4.10 基于基本组合逻辑功能部件的组合逻辑设计

若译码器是以反变量形式输出，即输出的是mi,则：

$$F_1 = A\overline{B} + \overline{B}C + AC = m_1 + m_4 + m_5 + m_7$$

$$= \overline{\overline{m_1 + m_4 + m_5 + m_7}} = \overline{\overline{m_1} \cdot \overline{m_4} \cdot \overline{m_5} \cdot \overline{m_7}}$$

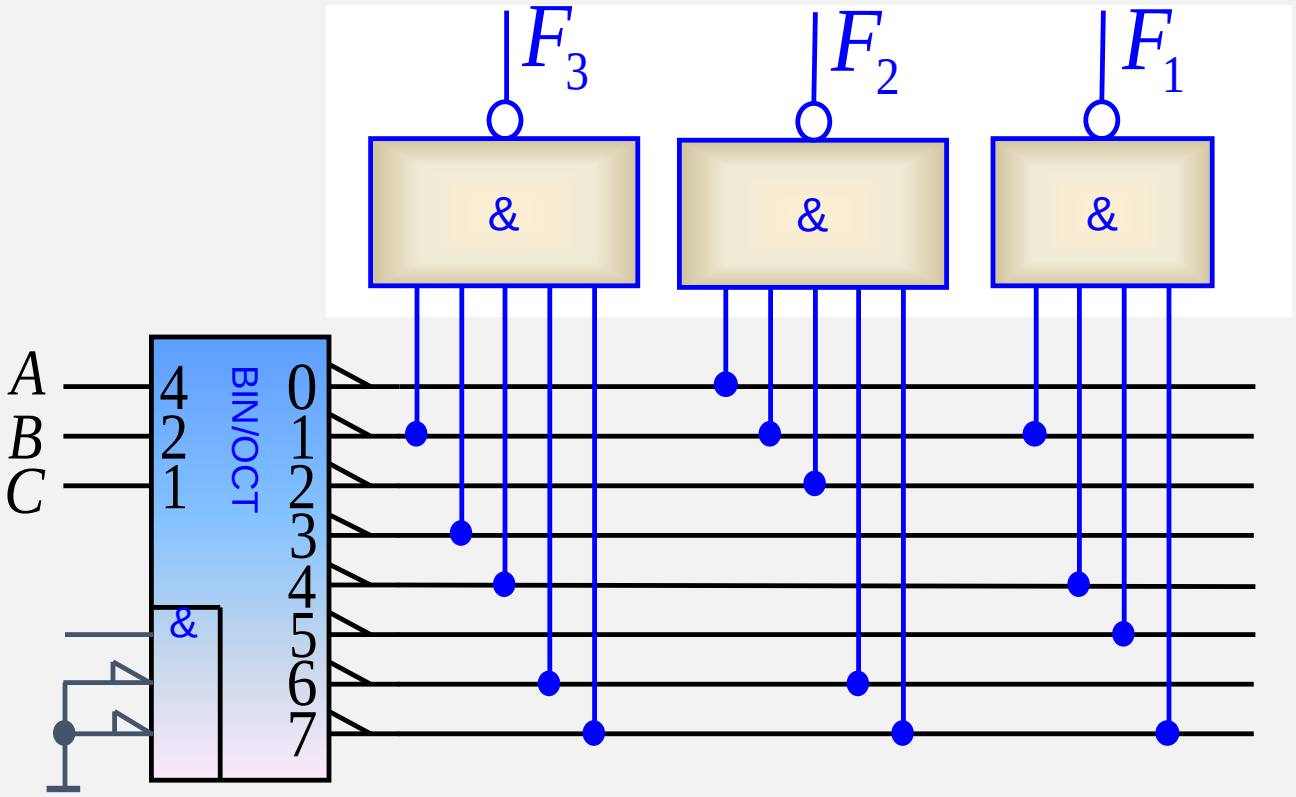
$$= \overline{\overline{Y_1} \cdot \overline{Y_4} \cdot \overline{Y_5} \cdot \overline{Y_7}}$$

$$F_2 = \overline{A}\overline{B} + B\overline{C} + ABC = \sum m(0,1,2,6,7) = \overline{\overline{m_0} \cdot \overline{m_1} \cdot \overline{m_2} \cdot \overline{m_6} \cdot \overline{m_7}}$$

$$= \overline{\overline{Y_0} \cdot \overline{Y_1} \cdot \overline{Y_2} \cdot \overline{Y_6} \cdot \overline{Y_7}}$$

$$F_3 = \overline{A}C + BC + A\overline{C} = \sum m(1,3,4,6,7) = \overline{\overline{Y_1} \cdot \overline{Y_3} \cdot \overline{Y_4} \cdot \overline{Y_6} \cdot \overline{Y_7}}$$

4.10 基于基本组合逻辑功能部件的组合逻辑设计



例2：用2－4译码器和适当的逻辑门实现逻辑函数

$$F_1 = A\overline{B} + \overline{B}C + AC$$
$$F_2 = \overline{A}\overline{B} + B\overline{C} + ABC$$
$$F_3 = \overline{A}C + BC + A\overline{C}$$

$$F_1 = A\overline{B} + \overline{B}C + AC = \overline{\overline{m_1} \cdot \overline{m_4} \cdot \overline{m_5} \cdot \overline{m_7}} = \overline{\overline{Y_1} \cdot \overline{Y_4} \cdot \overline{Y_5} \cdot \overline{Y_7}}$$

$$F_2 = \overline{A}\overline{B} + B\overline{C} + ABC = \overline{\overline{m_0} \cdot \overline{m_1} \cdot \overline{m_2} \cdot \overline{m_6} \cdot \overline{m_7}} = \overline{\overline{Y_0} \cdot \overline{Y_1} \cdot \overline{Y_2} \cdot \overline{Y_6} \cdot \overline{Y_7}}$$

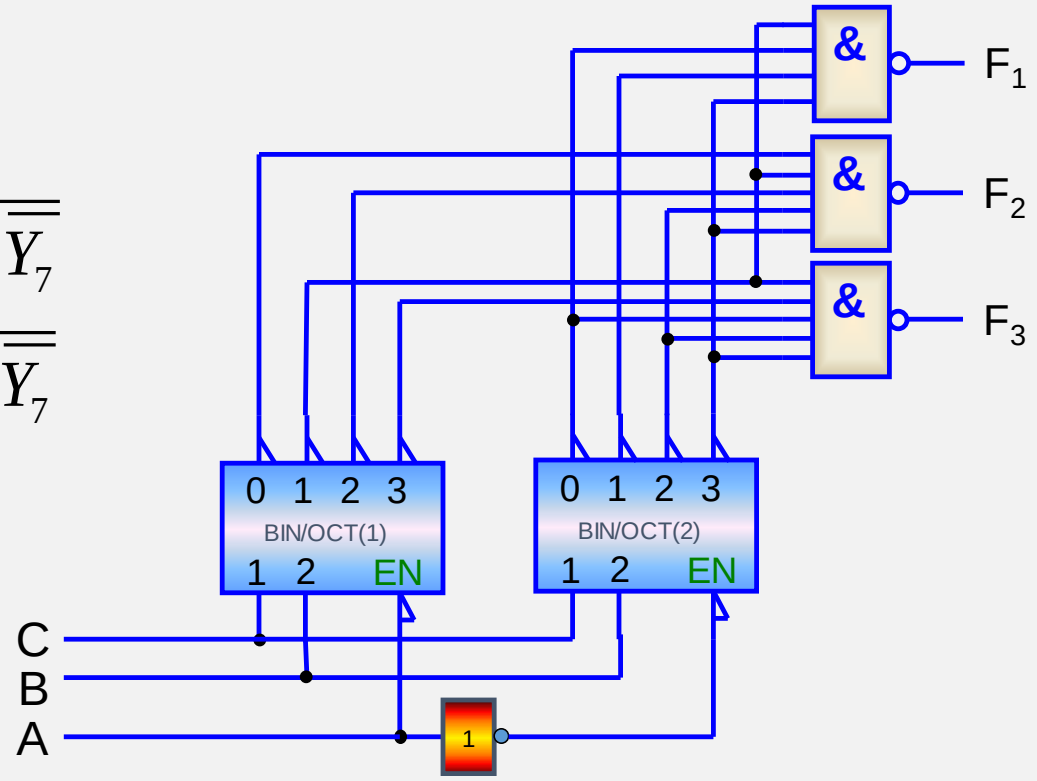
$$F_3 = \overline{A}C + BC + A\overline{C} = \overline{\overline{m_1} \cdot \overline{m_3} \cdot \overline{m_4} \cdot \overline{m_6} \cdot \overline{m_7}} = \overline{\overline{Y_1} \cdot \overline{Y_3} \cdot \overline{Y_4} \cdot \overline{Y_6} \cdot \overline{Y_7}}$$

4.10 基于基本组合逻辑功能部件的组合逻辑设计

$$F_1 = \overline{\overline{Y_1} \cdot \overline{Y_4} \cdot \overline{Y_5} \cdot \overline{Y_7}}$$

$$F_2 = \overline{\overline{Y_0} \cdot \overline{Y_1} \cdot \overline{Y_2} \cdot \overline{Y_6} \cdot \overline{Y_7}}$$

$$F_3 = \overline{\overline{Y_1} \cdot \overline{Y_3} \cdot \overline{Y_4} \cdot \overline{Y_6} \cdot \overline{Y_7}}$$



4.11 一位全加器FA设计


```
  1 1
+ 1 1
  1 0
-------
1 1 0
```

加数X_i	加数Y_i	低位进位C_i	和数S_i	进位C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S_i = X_i \oplus Y_i \oplus C_i$$

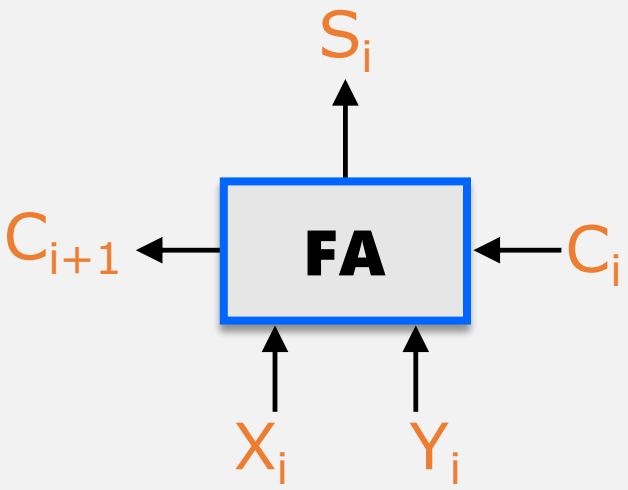
$$C_{i+1} = X_i Y_i + (X_i \oplus Y_i) C_i$$

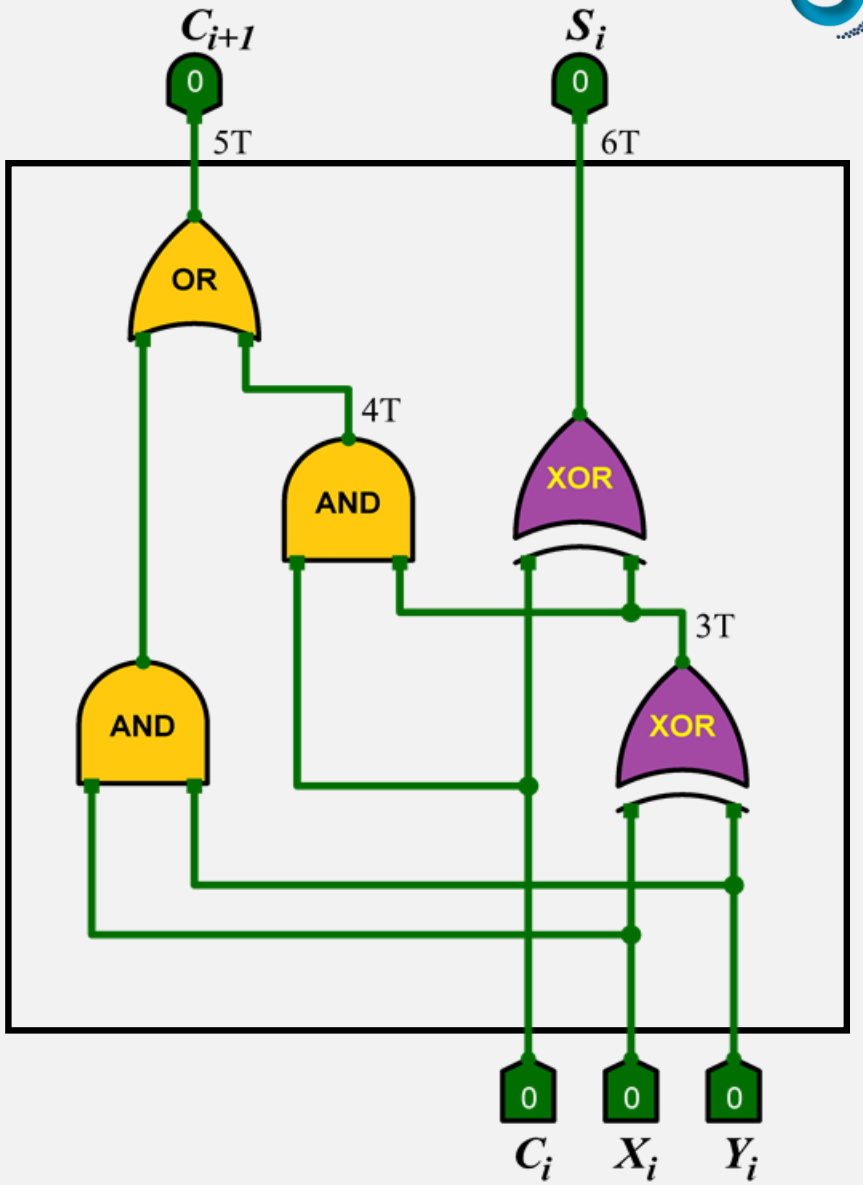
$$C_{i+1} = X_i Y_i + (X_i + Y_i) C_i$$

4.11 一位全加器FA设计

$$S_i = X_i \oplus Y_i \oplus C_i$$

$$C_{i+1} = X_i Y_i + (X_i \oplus Y_i) C_i$$





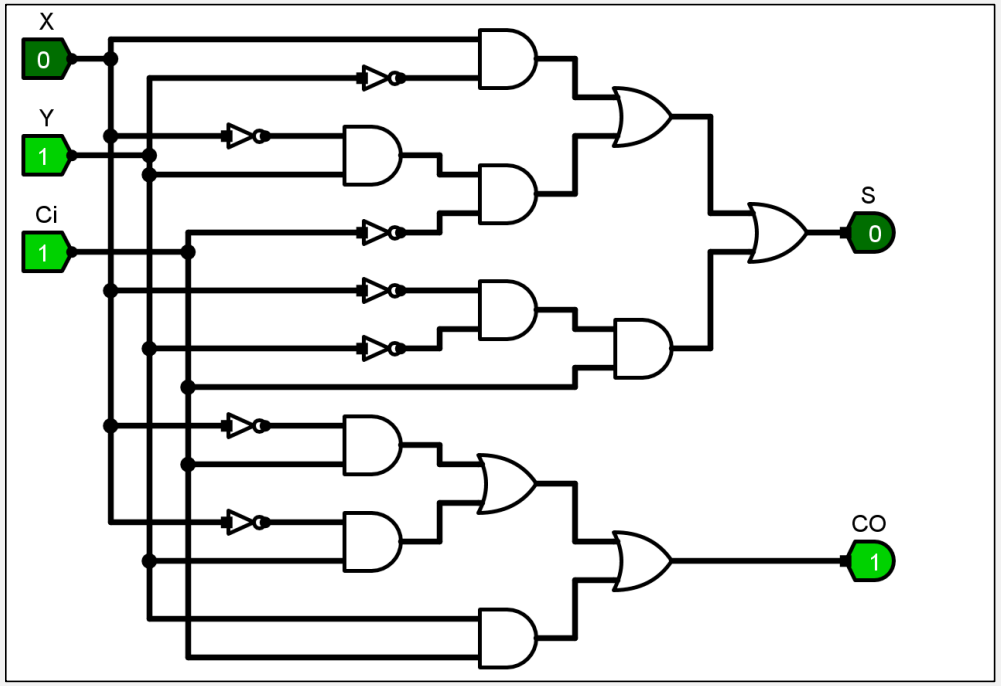
4.11 一位全减器的设计

加数X_i	加数Yi	低位进位C_i	和数S_i	进位C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

被减数X_i	减数Yi	低位借位C_i	差S_i	借位C_{i+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

4.11 一位全减器的设计

被减数X_i	减数Y_i	低位借位C_i	差S_i	借位C_{i+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



$$S_i = \overline{X}\overline{Y}C + \overline{X}Y\overline{C} + X\overline{Y}\overline{C} + XYC$$

$$= \overline{X}\overline{Y}C + \overline{X}Y\overline{C} + X\overline{Y}$$

$$C_{i+1} = \overline{X}\overline{Y}C + \overline{X}Y\overline{C} + \overline{X}YC + XYC$$

$$= \overline{X}Y + YC + \overline{X}C$$

本节内容完成