EE224 : Project Report Processor

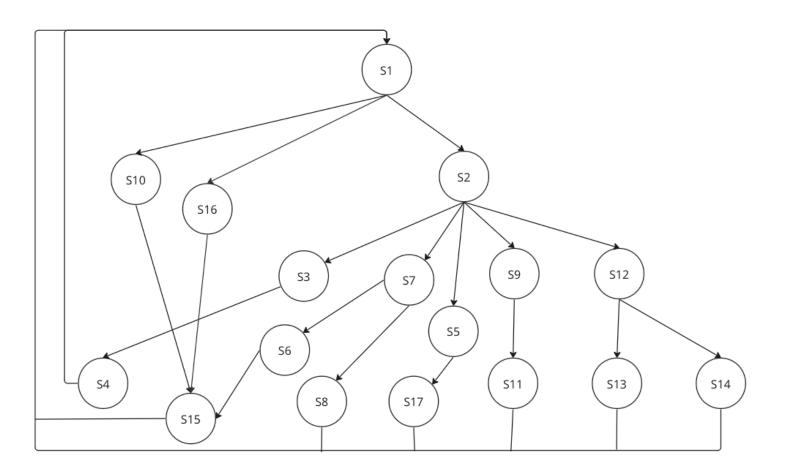
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State Diagram



State Descriptions

S1: Fetch

S2: Operand Read

S3: Execute

S4: Update

S5: Immediate Addition (T1)

S6: Memory Read

S7: Immediate Addition (T2)

S8: Memory Write

S9: Zero Evaluation

S10: LHI Shift

S11: Program Branch

S12: Store PC in Reg A

S13: Store Reg B in IP (Reg 7)

S14: Add Immediate to IP

S15: Store T3 in Reg A

S16: LLI Sign extension

S17: Store T3 in Reg B

Operation Flow

ADD, SUB, MUL, AND, ORA, IMP: S1 -> S2 -> S3 -> S4

ADI: S1 -> S2 -> S5 -> S17

LHI: S1 -> S10 -> S15

LLI: S1 -> S16 -> S15

LW: S1 -> S2 -> S7 -> S6 -> S15

SW: S1 -> S2 -> S7 -> S8

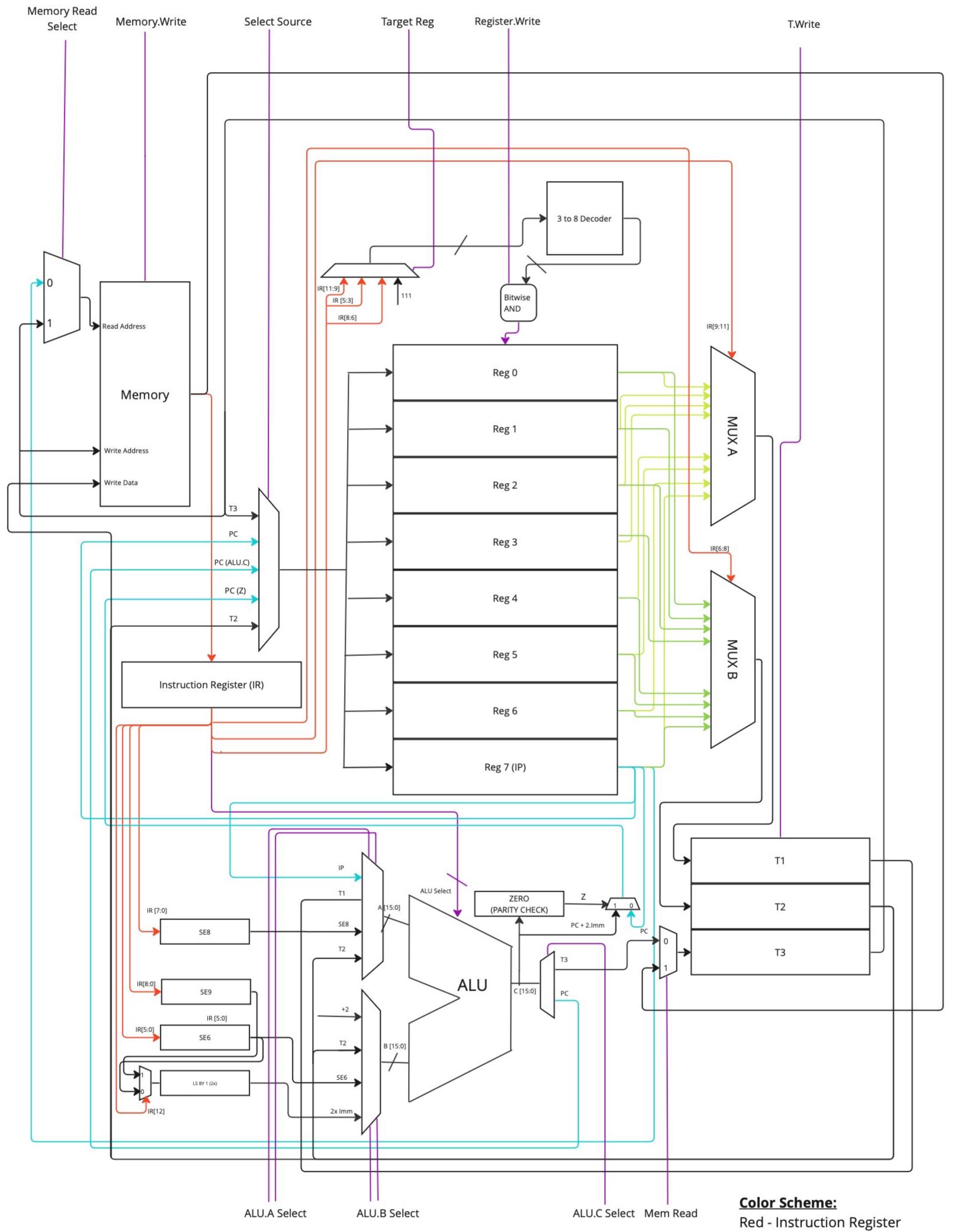
BEQ: S1 -> S2 -> S9 -> S11

JAL: S1 -> S2 -> S12 -> S13

JLR: S1 -> S2 -> S12 -> S14

Flowchart

			TD . DT D	1
Man_Data→IR	Mem_R Address TR-W TR-W	S1	$\begin{array}{c} \text{IP} \to \text{RF-D}_3 \\ \text{IR}_{9-n} \to \text{RF-A}_5 \end{array}$	Siz
$\begin{array}{c} TR_{q_{-1}} \longrightarrow RF_{-}A_{1} \\ TR_{6-8} \longrightarrow RF_{-}A_{2} \\ RF_{-}D_{2} \longrightarrow T, \\ RF_{-}D_{2} \longrightarrow T_{2} \end{array}$	T. 3 T. 3	S2	$IR_{6-8} \rightarrow RFA_2$ $IP\omega$ $RFD_2 \rightarrow IP$	SB
$T_{i} \rightarrow ALV_A$ $T_{i} \rightarrow ALV_B$ $ALV_C \rightarrow T_{i}$	ADD Ts.W	Sz	$IP \rightarrow ALU_A$ $IR_{0-5} \rightarrow SE_6 \rightarrow ALU_B$ $ALU_C \rightarrow IP$ IP_ω	Szų
$\begin{array}{c} T_3 \longrightarrow RF_D_3 \\ IR_{3-5} \longrightarrow RF_A_3 \end{array}$	RF_ω	S4	T ₃ → Men_Add Hen R Men_D → T ₃ T ₃ . W	S ₆
$\begin{array}{c} IR_{o-7} \longrightarrow SE_8 \\ SE_8 \longrightarrow AUUA \\ ALUC \longrightarrow T_3 \end{array}$	SHIFT To.W	Sıo	T3 → Men_ Data Men.w	S ₈
$T_1 \longrightarrow ALU_A$ $T_2 \longrightarrow ALU_B$ $ALU_C \longrightarrow Zero$ $Zero \longrightarrow Z$	SVB Z_W	S9	TZ ALV-A IROS -SEG-AUB ALV-C -> TS TE-W	57
IP → ALVLA IMM6→SE6→ALVB IF(z==1) AULC→IP ELSE IP→IP	ADD DPJW	Su	$\begin{array}{c} \mathbb{T} \longrightarrow RF_D_1 \\ \mathbb{IR}_{\mathfrak{q}_{-1 }} \longrightarrow RF_A_1 \end{array}$	S ₁₅
T ALULA IROS SEC AWB ALULC - T3	ADD Ts.W	S ₅	$ \begin{array}{ccc} T_3 & \longrightarrow RFD_2 \\ IR_{\xi} & \longrightarrow RFA_2 \end{array} $	S ₁₇
			$\begin{array}{c} \text{IR}_{6-7} \longrightarrow \text{SE}_8 \\ \text{SE}_8 \longrightarrow \text{T}_3 \end{array}$	Sic



Work Distribution

- 1. Ashwajit (22B1227)
- Controller
- Memory
- Debugging

2. Raunak (22B3955)

- Register File
- ALU
- Debugging

3. Suchet (22B1814)

- Top Level and Support Structures assembly
- Debugging