addi $1,$0,10

addi $2,$0,20

addi $3,$0,30

addi $5,$0,50

addi $6,$0,60

sw $5, 100($2)

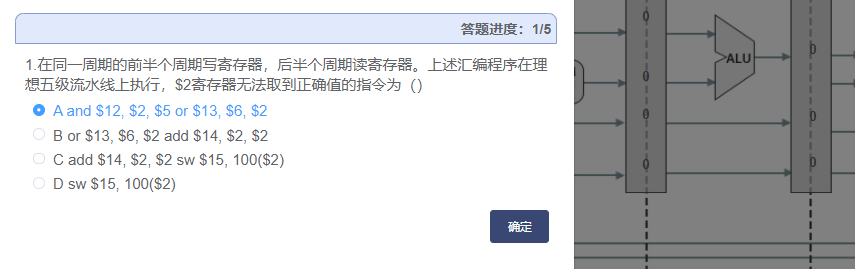
sub $2, $1, $3

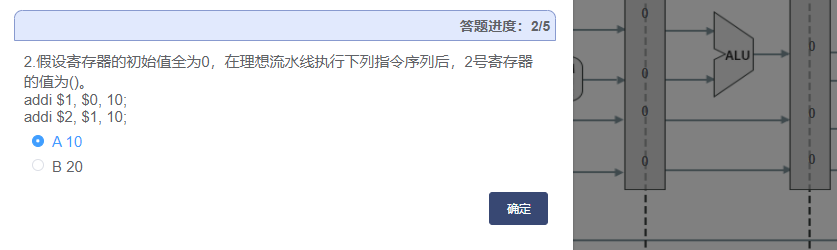
and $12, $2, $5

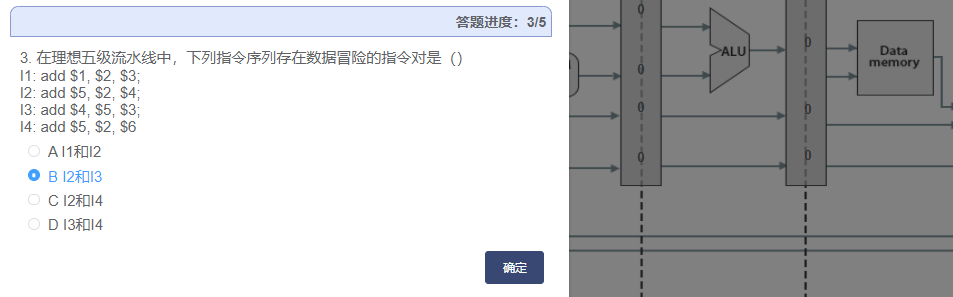
or $13, $6, $2

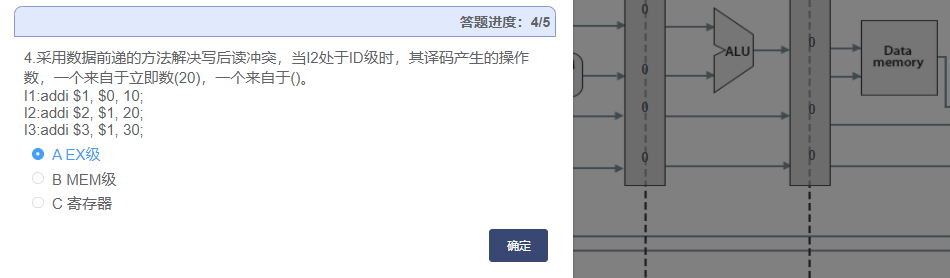
add $14, $2, $2

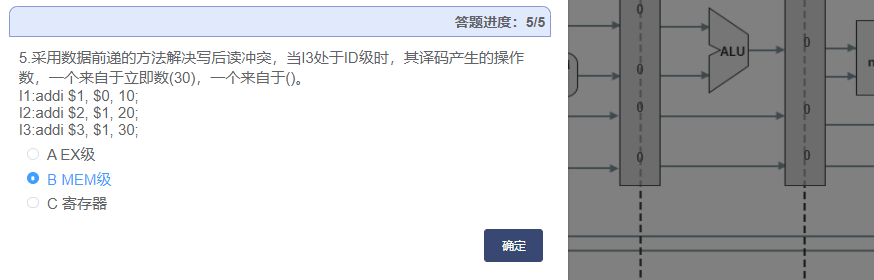
lw $15, 100($2)



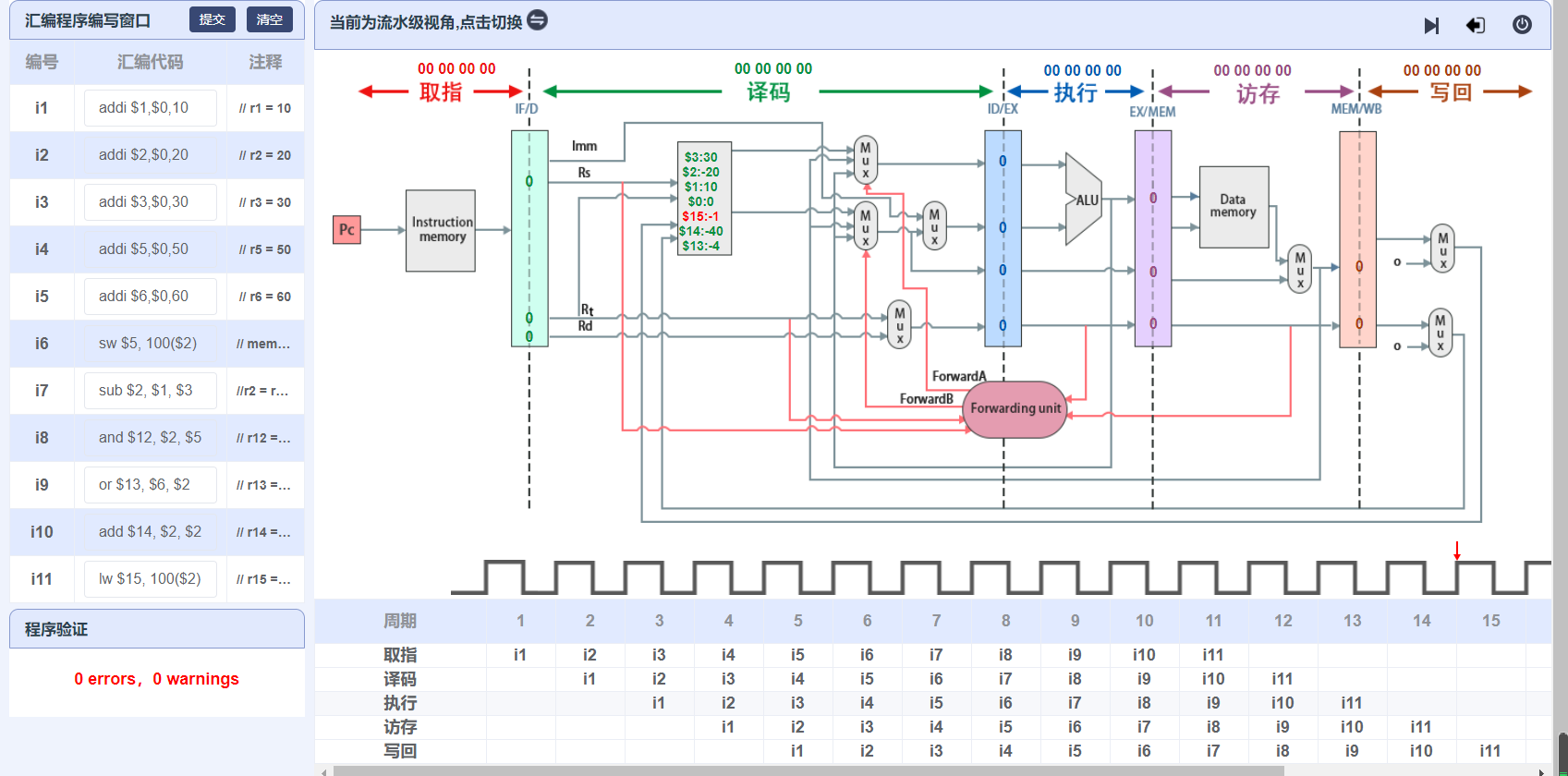








顺序：先写会，再访存，依次往前









addi $1,$0,10

addi $2,$0,20

addi $3,$0,30

sw $1, 20($1)

addi $5,$0,50

addi $6,$0,60

addi $7,$0,70

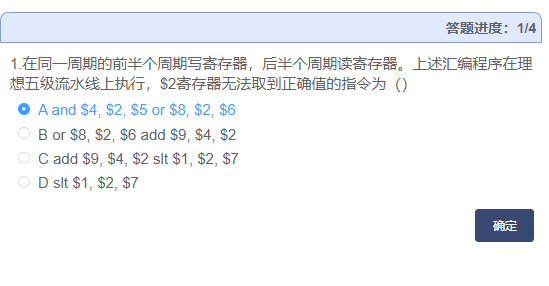
lw $2, 20($1)

and $4, $2, $5

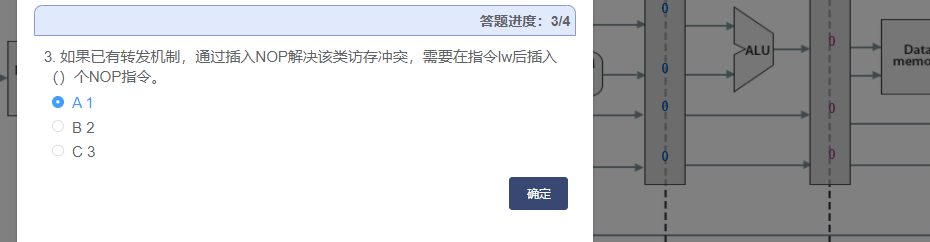
or $8, $2, $6

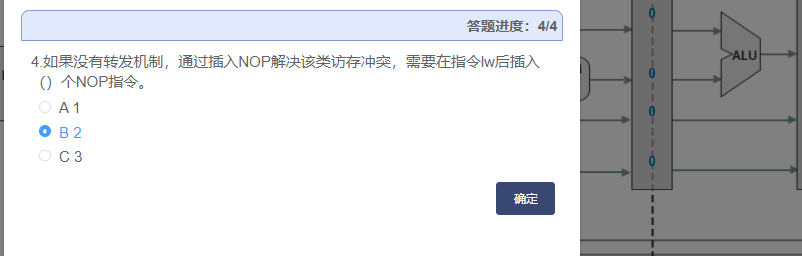
add $9, $4, $2

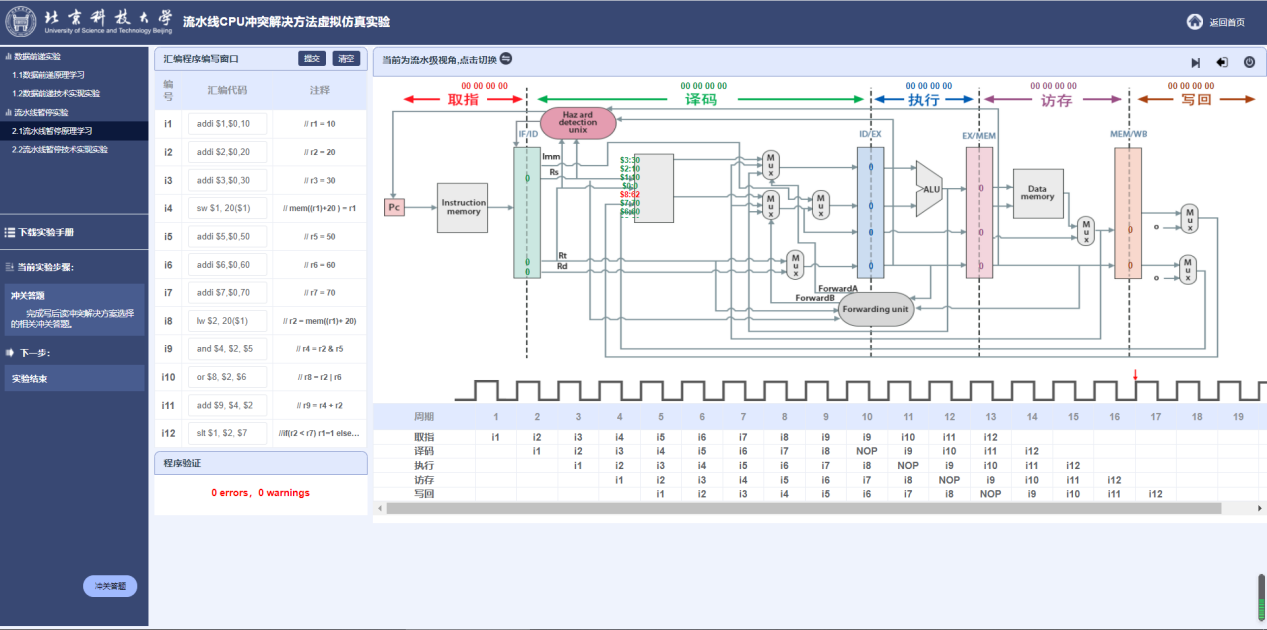
slt $1, $2, $7

















|  |  |
| --- | --- |
| ID | //待补充，完成对stall\_request的赋值  assign stall\_request = (load\_related\_1 || load\_related\_2); |
| RegReadProxy | //待补充，完成对load\_related\_1、load\_related\_2的赋值  assign load\_related\_1 = (ex\_load\_flag && read\_addr\_1==reg\_write\_addr\_from\_ex) || (mem\_load\_flag && read\_addr\_1==reg\_write\_addr\_from\_mem ) ;  assign load\_related\_2 = (ex\_load\_flag && read\_addr\_2==reg\_write\_addr\_from\_ex) || (mem\_load\_flag && read\_addr\_2==reg\_write\_addr\_from\_mem ) ; |
| PipelineDeliver | always @(posedge clk) begin  if (rst) begin  out <= 0;  end  else if (stall\_current\_stage && !stall\_next\_stage) begin  out<=0;  end  else if (!stall\_current\_stage) begin  out<=in;  end  //待补充，实现暂停功能  end |
|  |  |
|  |  |
|  |  |
|  |  |

