Question4

For a direct-mapped cache design with a 32-bit address

	Tag	Index	Offset
a.	31–10	9–5	4–0
b.	31–12	11–6	5–0

I. The chunks of memory handled by the cache are called cache lines. The size of these chunks is called the cache line size. Common cache line sizes are 32, 64 and 128 bytes. For example, a 64-kilobyte cache with 64-byte lines has 1024 cache lines
Tag- The higher order bits of the address
Index- bits that determine the lines possible location
Offset- which byte within the line

Cache lines = L
Cache line size = B
Address length = A (32 bits in our case)

Index bits = log2(L)
Offset bits = log2(B)
Tag bits = A - (index bits + offset bits)

a) Cache line size:
Block size=2^N
Where N= (number of offset bits)-2
N=5-2=3
Block size= 2^3 =8 bytes
Catch line size = 8 words

b) Cache line size:
Block size=2^N
Where N= (number of offset bits)-2
N=6-2=4
Block size= 2^4 =16 bytes
Catch line size = 16 words

II. How many entries does the cache have?
a) The index has 5 bits, and therefore the cache has 2^5 =**32 entries**
b) The index has 6 bits, and therefore the cache has 2^6 =**64 entries**

III. The ratio between total bits required for such a cache implementation over the data storage bits:

a) n= index =9-5+1=5
2 power m=number of words in the block=8
Total bits = 2power n * [2 power m* 32 + 31 -n - m]
Total bits =2 power 5*(8*32+31-5-3) = 8928

Storage bits = 2 power 5 * [2 power 5] bytes (offset 4-0, offset should be taken in 2 powers)
Storage bits = 2 power 5 * [2 power 5] *8bits =8192
Ratio= Total bits /Data bits=1.0898 =**1.10**

b) n= index =11-6+1=6
2 power m=number of words in the block=16

Total bits = 2power n * [2 power m* 32 + 31 -n - m]
Total bits =2power 6 * [16* 32 + 31 -6 - 4] =34112 bits

Storage bits = 2 power 6 * [2 power 6] bytes (offset 5-0, offset should be taken in 2 powers)
Storage bits = 2 power 6 * [2 power 5] *8bits =32768bits
Ratio= Total bits /Data bits=**1.04**