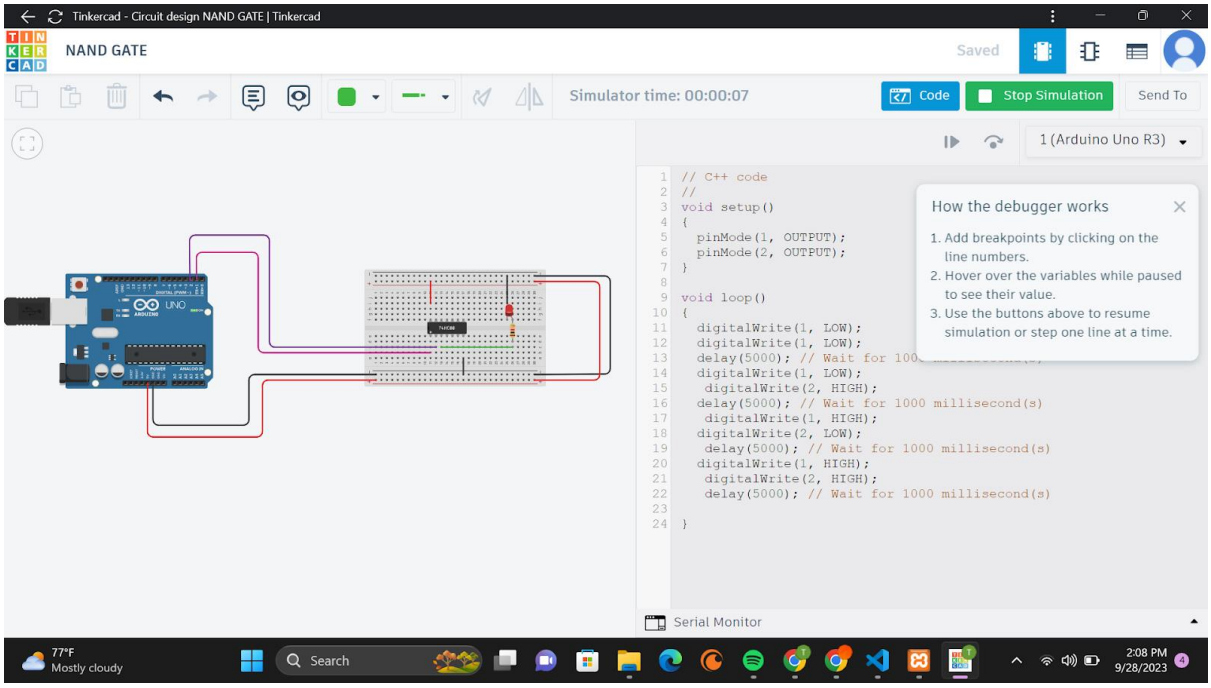
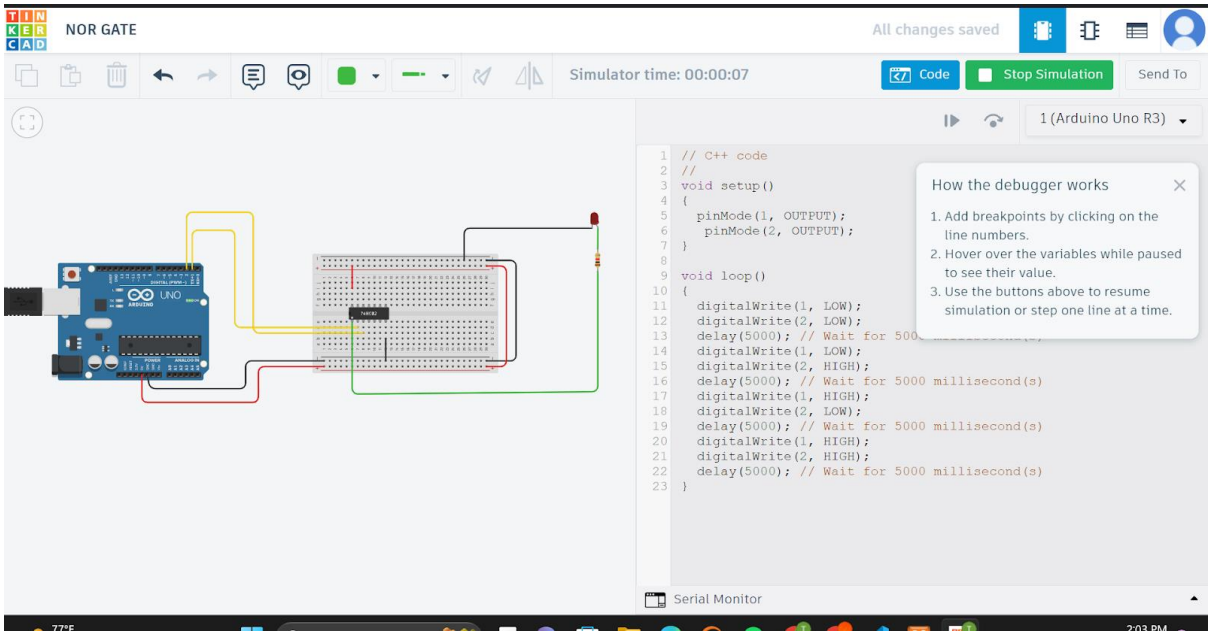
150467 LIZALOUREEN MAWIA KITHEKA

A) Simulation and implementation of logic gates using the basic and universal gate

NAND GATE



NOR GATE



NOR GATE TRUTH TABLE

A	B	(A+B)’
0	1	0
0	0	1
1	1	0
1	0	0

NAND GATE TRUTH TABLE

A	B	(AB)’
0	1	1
0	0	1
1	1	0
1	0	1

TRUTH TABLE FOR AB+A’B’

A	B	AB+A’B’
0	0	1
0	1	0
1	0	0
1	1	1

PART B: Gate level Minimization

Y = $\overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} + AB\overline{C}\overline{D} + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + A\overline{B}C$D

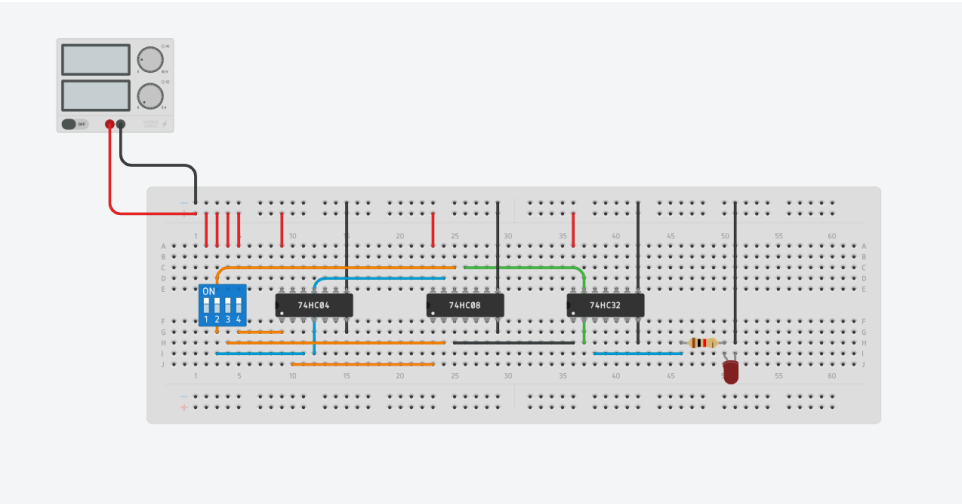
A	B	C	D	A’B’C D’	A’BCD ’	AB’CD ’	AB’CD	AB’C’ D’	AB’C’ D	AB’CD	Y

0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1
0	1	1	0	0	1	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1	0	0	1
1	0	1	1	0	0	0	0	0	1	0	1
1	0	1	0	0	0	0	1	0	0	1	1
1	1	0	1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	1	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	0	0

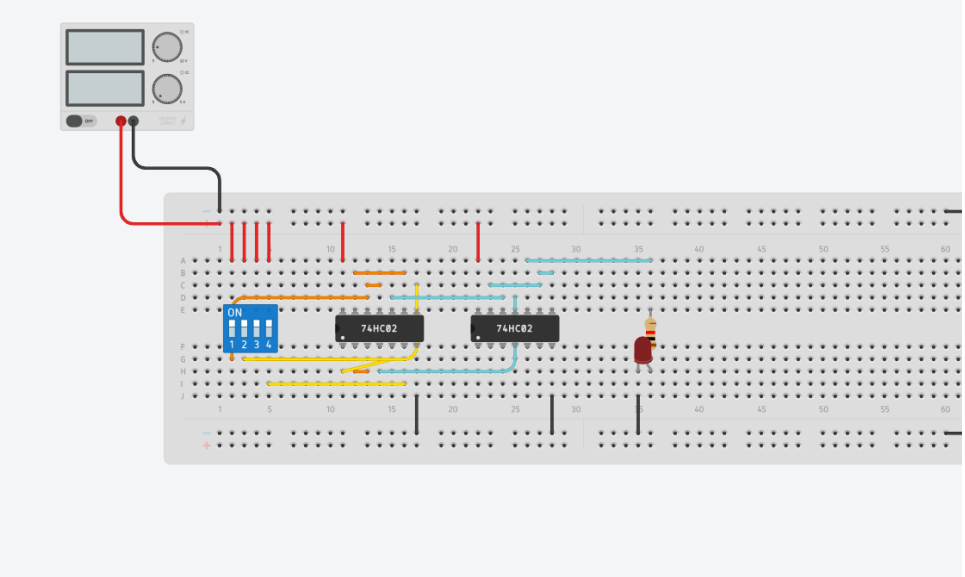
	00	01	11	10
00				1
01				1
11				1
10	1	1	1	1

= (m8+m9+m11+m10) + (m2+m6+m14+m10)

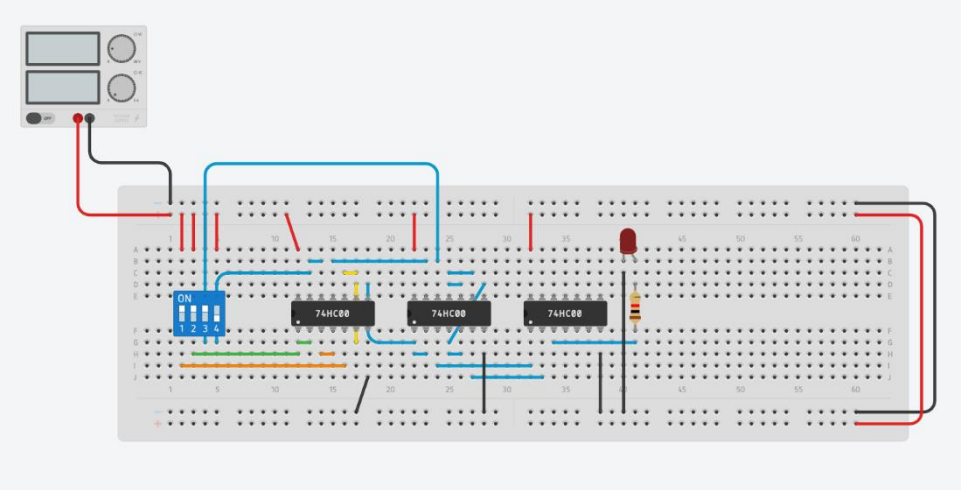
= AB’ + CD’



K-MAP using normal Gates.



K-MAP using NOR Gates.

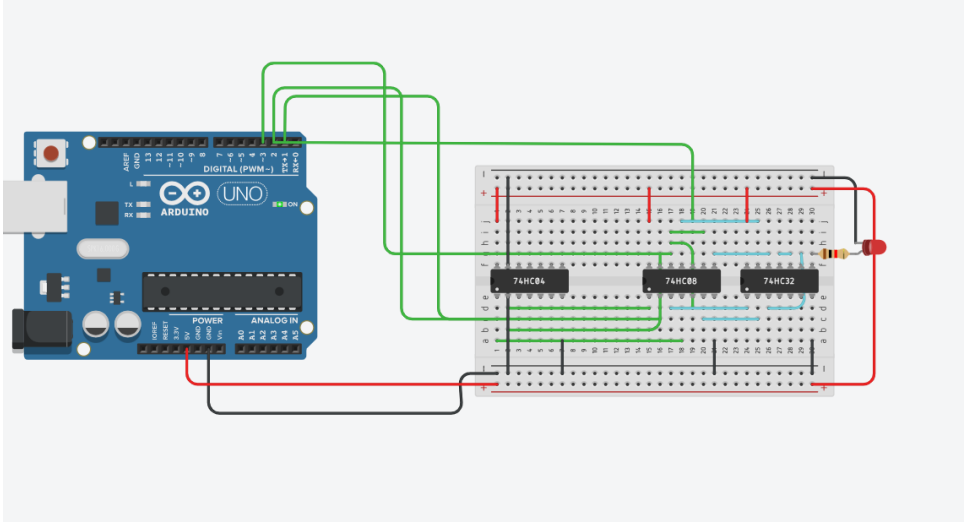


Question 2A)

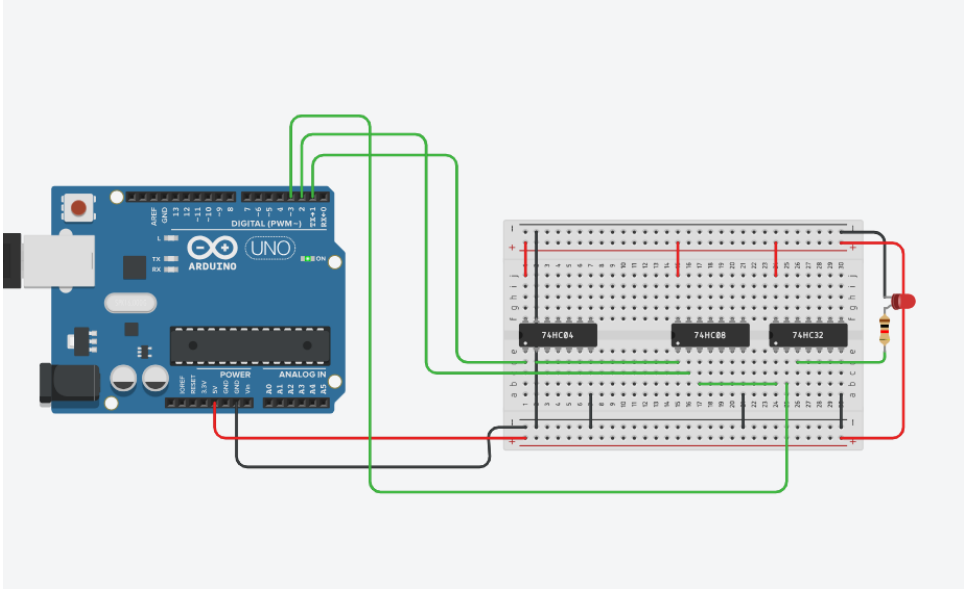
Y= A'C + A'B + AC + BC

A	B	C	A'C	A'B	AC	BC	Y	A'B+C
0	0	1	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	1	1	0	1	0	0	1	1
0	1	0	1	1	0	1	1	1
1	0	1	0	0	0	0	0	0
1	0	0	0	0	1	0	1	1

1	1	1	0	0	0	0	0	0
1	1	0	0	0	1	1	1	1



circuit: Y= A’C + A’B + AC + BC



BOTH CIRCUITS ARE IDENTICAL

F(w,x,y,z)= ∏(0,1,4,5,6,7,8,9)

	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	1	1	1	1

10	0	0	1	1

(m4+m5+m7+m6) + (m8+m9+m0+m1)

w'xy'z'+w'xy'z+w'xyz+w'xyz' = w'x +

Wx'y'z'+wx'y'z+w'x'y'z+w'y'x'z = x'y'

= (w'x+x'y')'

=(w'x)'(x'y')

=(w+x')(x+y);

Circuit for (w+x')(x+y)