PKU--LL201-处理器核

阶段一：ISA

- Instruction set: https://en.wikipedia.org/wiki/Instruction_set
  - An instruction set, or instruction set architecture (ISA), is the part of the computer architecture related to programming, including the native data types, instructions, registers, addressing modes, memory architecture, interrupt and exception handling, and external I/O.
  - Word: https://en.wikipedia.org/wiki/Word_(computer_architecture)
    - In computing, word is a term for the natural unit of data used by a particular processor design.
    - A word is a fixed-sized piece of data handled as a unit by the instruction set or the hardware of the processor.
    - The number of bits in a word (the word size, word width, or word length) is an important characteristic of any specific processor design or computer architecture.
  - Data type: https://en.wikipedia.org/wiki/Data_type
    - In computer science and computer programming, a data type or simply type is a classification identifying one of various types of data, such as real, integer or Boolean, that determines the possible values for that type; the operations that can be done on values of that type; the meaning of the data; and the way values of that type can be stored.
    - Primitive data type: https://en.wikipedia.org/wiki/Primitive_data_type
      - In computer science, primitive data type is either of the following:
        - a basic type is a data type provided by a programming language as a basic building block. Most languages allow more complicated composite types to be recursively constructed starting from basic types.
        - a built-in type is a data type for which the programming language provides built-in support.
      - In most programming languages, all basic data types are built-in.
      - In addition, many languages also provide a set of composite data types. Opinions vary as to whether a built-in type that is not basic should be considered "primitive".
  - Processor register: https://en.wikipedia.org/wiki/Processor_register
    - In computer architecture, a processor register is a small amount of storage available as part of a digital processor, such as a central processing unit (CPU).
    - Processor registers are normally at the top of the memory hierarchy, and provide the fastest way to access data.
    - The term normally refers only to the group of registers that are directly encoded as part of an instruction, as defined by the instruction set.
- X86：https://en.wikipedia.org/wiki/X86
  - x86 is a family of backward compatible instruction set architectures based on the Intel 8086 CPU and its Intel 8088 variant.
  - x86 registers:
    - General-purpose registers (GPRs) can store both data and addresses, i.e., they are combined data/address registers and rarely the register file is unified to include floating point as well.
    - Control register: https://en.wikipedia.org/wiki/Control_register
      - A control register is a processor register which changes or controls the general behavior of a CPU or other digital device. Common tasks performed by control registers include interrupt control, switching the addressing mode, paging control, and coprocessor control.
    - Status register：https://en.wikipedia.org/wiki/Status_register
      - A status register, flag register, or condition code register is a collection of status flag bits for a processor. An example is the FLAGS register of the x86 architecture. The flags might be part of a larger register, such as a program status word (PSW) register.
  - Operating modes:
    - Real mode：https://en.wikipedia.org/wiki/Real_mode
      - Real mode, also called real address mode, is an operating mode of all x86-compatible CPUs. Real mode is characterized by a 20-bit segmented memory address space (giving exactly 1 MiB of addressable memory) and unlimited direct software access to all addressable memory, I/O addresses and peripheral hardware.
      - Real mode provides no support for memory protection, multitasking, or code privilege levels.
    - Protected mode: https://en.wikipedia.org/wiki/Protected_mode
      - In computing, protected mode, also called protected virtual address mode, is an operational mode of x86-compatible central processing units (CPUs).
      - It allows system software to use features such as virtual memory, paging and safe multi-tasking designed to increase an operating system's control over application software.
    - Long mode: https://en.wikipedia.org/wiki/Long_mode
      - In the x86-64 computer architecture, long mode is the mode where a 64-bit operating system can access 64-bit instructions and registers.
      - 64-bit programs are run in a sub-mode called 64-bit mode, while 32-bit programs and 16-bit

protected mode programs are executed in a sub-mode called compatibility mode. Real mode or virtual 8086 mode programs cannot be natively run in long mode.
        - Unreal mode: https://en.wikipedia.org/wiki/Unreal_mode
            - In x86 computing, unreal mode, also big real mode, huge real mode, or flat real mode, is a variant of real mode, in which one or more data segment registers have been loaded with 32-bit addresses and limits.
        - Virtual 8086 mode: https://en.wikipedia.org/wiki/Virtual_8086_mode
            - In the 80386 microprocessor and later, virtual 8086 mode (also called virtual real mode, V86-mode or VM86) allows the execution of real mode applications that are incapable of running directly in protected mode while the processor is running a protected mode operating system.
- Processor supplementary capability: https://en.wikipedia.org/wiki/Processor_supplementary_capability
    - A processor supplementary capability is a feature that has been added to an existing central processing unit design after the initial introduction of that design to the marketplace.
    - CPUID：https://en.wikipedia.org/wiki/CPUID
        - The CPUID opcode is a processor supplementary instruction (its name derived from CPU IDentification) for the x86 architecture allowing software to discover details of the processor.
        - 三个命令：
            - cat /proc/cpuinfo
            - lscpu
            - cpuid
                - `sudo apt-get install cpuid`
                - `cpuid`
    - Model-specific register：https://en.wikipedia.org/wiki/Model-specific_register
        - A model-specific register (MSR) is any of various control registers in the x86 instruction set used for debugging, program execution tracing, computer performance monitoring, and toggling certain CPU features.
        - Reading and writing to these registers is handled by the rdmsr and wrmsr instructions, respectively.
        - TRY:
            - `sudo apt-get install msr-tools`
            - `sudo rdmsr 0x10`
                - `time stamp counter`
            - `sudo rdmsr 0x1b`
                - `apic base`
            - `sudo rdmsr 0xc0000080`
                - `EFER: extended feature enable register`

自学：

1. Instruction set: https://en.wikipedia.org/wiki/Instruction_set
2. Word: https://en.wikipedia.org/wiki/Word_(computer_architecture)
3. Data type: https://en.wikipedia.org/wiki/Data_type
4. Primitive data type: https://en.wikipedia.org/wiki/Primitive_data_type
5. Processor register: https://en.wikipedia.org/wiki/Processor_register
6. X86：https://en.wikipedia.org/wiki/X86
7. Control register: https://en.wikipedia.org/wiki/Control_register
8. Status register：https://en.wikipedia.org/wiki/Status_register
9. Real mode：https://en.wikipedia.org/wiki/Real_mode
10. Protected mode: https://en.wikipedia.org/wiki/Protected_mode
11. Long mode: https://en.wikipedia.org/wiki/Long_mode
12. Unreal mode: https://en.wikipedia.org/wiki/Unreal_mode
13. Virtual 8086 mode: https://en.wikipedia.org/wiki/Virtual_8086_mode
14. Processor supplementary capability: https://en.wikipedia.org/wiki/Processor_supplementary_capability
15. CPUID：https://en.wikipedia.org/wiki/CPUID
16. Model-specific register：https://en.wikipedia.org/wiki/Model-specific_register

See Also:

- List of instruction sets: https://en.wikipedia.org/wiki/List_of_instruction_sets
- Comparison of instruction set architectures：
    - https://en.wikipedia.org/wiki/Comparison_of_instruction_set_architectures
- Agner's CPU blog: Stop the instruction set war: http://www.agner.org/optimize/blog/read.php?i=25

阶段二：核心之外

- Coprocessor：https://en.wikipedia.org/wiki/Coprocessor
    - A coprocessor is a computer processor used to supplement the functions of the primary processor (the CPU).
    - Operations performed by the coprocessor may be floating point arithmetic, graphics, signal processing, string processing, encryption or I/O Interfacing with peripheral devices.
    - By offloading processor-intensive tasks from the main processor, coprocessors can accelerate system performance.

    - Coprocessors allow a line of computers to be customized, so that customers who do not need the extra performance don't need to pay for it.
- ASIC: https://en.wikipedia.org/wiki/Application-specific_integrated_circuit
    - An application-specific integrated circuit (ASIC) / e s k/, is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed to run in a digital voice recorder or a high-efficiency Bitcoin miner is an ASIC.
    - Floating point unit：https://en.wikipedia.org/wiki/Floating-point_unit
        - A floating-point unit (FPU, colloquially a math coprocessor) is a part of a computer system specially designed to carry out operations on floating point numbers.
        - MMX: https://en.wikipedia.org/wiki/MMX_(instruction_set)
            - MMX is a single instruction, multiple data (SIMD) instruction set designed by Intel, introduced in 1997 with its P5-based Pentium line of microprocessors, designated as "Pentium with MMX Technology".
            - MMX is a processor supplementary capability that is supported on recent IA-32 processors by Intel and other vendors.
            - MMX is officially a meaningless initialism trademarked by Intel; unofficially, the initials have been variously explained as standing for MultiMedia eXtension, Multiple Math eXtension, or Matrix Math eXtension.
    - SIMD: https://en.wikipedia.org/wiki/SIMD
        - Single instruction, multiple data (SIMD), is a class of parallel computers in Flynn's taxonomy.
        - It describes computers with multiple processing elements that perform the same operation on multiple data points simultaneously.
        - Thus, such machines exploit data level parallelism, but not concurrency: there are simultaneous (parallel) computations, but only a single process (instruction) at a given moment.
        - Data parallelism: https://en.wikipedia.org/wiki/Data_parallelism
            - Data parallelism is a form of parallelization of computing across multiple processors in parallel computing environments.
            - Data parallelism focuses on distributing the data across different parallel computing nodes.
            - It contrasts to task parallelism as another form of parallelism.
        - Vector processor: https://en.wikipedia.org/wiki/Vector_processor
            - In computing, a vector processor or array processor is a central processing unit (CPU) that implements an instruction set containing instructions that operate on one-dimensional arrays of data called vectors. (Compare scalar processors, whose instructions operate on single data items.)
            - SSE：https://en.wikipedia.org/wiki/Streaming_SIMD_Extensions
            - SSE2：https://en.wikipedia.org/wiki/SSE2
            - SSE3：https://en.wikipedia.org/wiki/SSE3
            - SSSE3：https://en.wikipedia.org/wiki/SSSE3
            - SSE4：https://en.wikipedia.org/wiki/SSE4
            - 3DNow!: https://en.wikipedia.org/wiki/3DNow!
        - SWAR: https://en.wikipedia.org/wiki/SWAR
            - SIMD within a register (SWAR) is a technique for performing parallel operations on data contained in a processor register. SIMD stands for single instruction, multiple data.
    - GPU: https://en.wikipedia.org/wiki/Graphics_processing_unit
        - A graphics processor unit (GPU), also occasionally called visual processor unit (VPU), is a specialized electronic circuit designed to rapidly manipulate and alter memory to accelerate the creation of images in a frame buffer intended for output to a display.
    - Network processor：https://en.wikipedia.org/wiki/Network_processor
        - A network processor is an integrated circuit which has a feature set specifically targeted at the networking application domain.
        - Network processors are typically software programmable devices and would have generic characteristics similar to general purpose central processing units that are commonly used in many different types of equipment and products.
    - Digital signal processor：https://en.wikipedia.org/wiki/Digital_signal_processor
        - A digital signal processor (DSP) is a specialized microprocessor (or a SIP block), with its architecture optimized for the operational needs of digital signal processing.
        - The goal of DSPs is usually to measure, filter and/or compress continuous real-world analog signals.
- Programmable logic device：https://en.wikipedia.org/wiki/Programmable_logic_device
    - A programmable logic device (PLD) is an electronic component used to build reconfigurable digital circuits. Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture. Before the PLD can be used in a circuit it must be programmed, that is, reconfigured.
    - Reconfigurable computing: https://en.wikipedia.org/wiki/Reconfigurable_computing
        - Reconfigurable computing is a computer architecture combining some of the flexibility of software with the high performance of hardware by processing with very flexible high speed computing fabrics like field-programmable gate arrays (FPGAs).
        - The principal difference when compared to using ordinary microprocessors is the ability to make substantial changes to the datapath itself in addition to the control flow.
    - Field-programmability: https://en.wikipedia.org/wiki/Field-programmability

        - An electronic device or embedded system is said to be field-programmable or in-place programmable if its firmware (stored in non-volatile memory, such as ROM) can be modified "in the field,"（在实地，在现场，在实际应用中） without disassembling the device or returning it to its manufacturer.
    - CPLD：https://en.wikipedia.org/wiki/Complex_programmable_logic_device
        - A complex programmable logic device (CPLD) is a programmable logic device with complexity between that of PALs and FPGAs, and architectural features of both.
    - FPGA：https://en.wikipedia.org/wiki/Field-programmable_gate_array
        - A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable".
        - Specific applications of FPGAs include digital signal processing, software-defined radio, ASIC prototyping, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, computer hardware emulation, radio astronomy, metal detection and a growing range of other areas.
- ASIP: https://en.wikipedia.org/wiki/Application-specific_instruction_set_processor
    - An application-specific instruction set processor (ASIP) is a component used in system-on-a-chip design. The instruction set of an ASIP is tailored to benefit a specific application. This specialization of the core provides a tradeoff between the flexibility of a general purpose CPU and the performance of an ASIC.
    - Some ASIPs have a configurable instruction set. Usually, these cores are divided into two parts: static logic which defines a minimum ISA (instruction-set architecture) and configurable logic which can be used to design new instructions. The configurable logic can be programmed either in the field in a similar fashion to an FPGA or during the chip synthesis.

自学：

1. Coprocessor：https://en.wikipedia.org/wiki/Coprocessor
2. ASIC: https://en.wikipedia.org/wiki/Application-specific_integrated_circuit
3. Floating point unit：https://en.wikipedia.org/wiki/Floating-point_unit
4. MMX: https://en.wikipedia.org/wiki/MMX_(instruction_set)
5. SIMD: https://en.wikipedia.org/wiki/SIMD
6. Data parallelism: https://en.wikipedia.org/wiki/Data_parallelism
7. Vector processor: https://en.wikipedia.org/wiki/Vector_processor
8. SSE：https://en.wikipedia.org/wiki/Streaming_SIMD_Extensions
9. SSE2：https://en.wikipedia.org/wiki/SSE2
10. SSE3：https://en.wikipedia.org/wiki/SSE3
11. SSSE3：https://en.wikipedia.org/wiki/SSSE3
12. SSE4：https://en.wikipedia.org/wiki/SSE4
13. 3DNow!: https://en.wikipedia.org/wiki/3DNow!
14. SWAR: https://en.wikipedia.org/wiki/SWAR
15. GPU: https://en.wikipedia.org/wiki/Graphics_processing_unit
16. Network processor：https://en.wikipedia.org/wiki/Network_processor
17. Digital signal processor：https://en.wikipedia.org/wiki/Digital_signal_processor
18. Programmable logic device：https://en.wikipedia.org/wiki/Programmable_logic_device
19. Reconfigurable computing: https://en.wikipedia.org/wiki/Reconfigurable_computing
20. Field-programmability: https://en.wikipedia.org/wiki/Field-programmability
21. CPLD：https://en.wikipedia.org/wiki/Complex_programmable_logic_device
22. FPGA：https://en.wikipedia.org/wiki/Field-programmable_gate_array
23. ASIP: https://en.wikipedia.org/wiki/Application-specific_instruction_set_processor

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阶段三：异常控制

- Interrupt vector table: https://en.wikipedia.org/wiki/Interrupt_vector_table
    - An interrupt vector table, a concept common across various processor architectures, is a table of interrupt vectors that associates an interrupt handler with an interrupt request in a machine specific way. A dispatch table is one method of implementing an interrupt vector table.
    - Interrupt Descriptor Table: https://en.wikipedia.org/wiki/Interrupt_descriptor_table
        - The Interrupt Descriptor Table (IDT) is a data structure used by the x86 architecture to implement an interrupt vector table. The IDT is used by the processor to determine the correct response to interrupts and exceptions.
        - Use of the IDT is triggered by three types of events: hardware interrupts, software interrupts, and processor exceptions, which together are referred to as "interrupts".
        - All INT_NUM between 0x0 and 0x1F, inclusive, are reserved for exceptions; INT_NUM bigger than 0x1F are used for interrupt routines.
        - Note：idtr是寄存器名称，即中断描述符表寄存器；汇编指令是lidt，即加载中断描述符表
- Interrupt handler: https://en.wikipedia.org/wiki/Interrupt_handler
    - In computer systems programming, an interrupt handler, also known as an interrupt service routine or ISR, is a callback function in microcontroller firmware, an operating system or a device driver, whose execution is triggered by the reception of an interrupt.
    - In general, interrupts and their handlers are used to handle high-priority conditions that require the interruption of the current code the processor is executing.

- Exception handling: https://en.wikipedia.org/wiki/Exception_handling
  - Exception handling is the process of responding to the occurrence, during computation, of exceptions – anomalous or exceptional conditions requiring special processing – often changing the normal flow of program execution.
  - It is provided by specialized programming language constructs or computer hardware mechanisms.

自学：

1. Interrupt vector table: https://en.wikipedia.org/wiki/Interrupt_vector_table
2. Interrupt Descriptor Table: https://en.wikipedia.org/wiki/Interrupt_descriptor_table
3. Interrupt handler: https://en.wikipedia.org/wiki/Interrupt_handler
4. Exception handling: https://en.wikipedia.org/wiki/Exception_handling

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阶段四：多核时代

- Parallel computing: https://en.wikipedia.org/wiki/Parallel_computing
  - Parallel computing is a form of computation in which many calculations are carried out simultaneously, operating on the principle that large problems can often be divided into smaller ones, which are then solved at the same time.
  - There are several different forms of parallel computing: bit-level, instruction level, data, and task parallelism.
  - Task parallelism: https://en.wikipedia.org/wiki/Task_parallelism
    - Task parallelism (also known as function parallelism and control parallelism) is a form of parallelization of computer code across multiple processors in parallel computing environments.
    - Task parallelism focuses on distributing tasks – concretely performed by processes or threads – across different parallel computing nodes.
    - It contrasts to data parallelism as another form of parallelism.
  - Scalable parallelism: https://en.wikipedia.org/wiki/Scalable_parallelism
    - Software is said to exhibit scalable parallelism if it can make use of additional processors to solve larger problems, i.e. this term refers to software for which Gustafson's law holds.
    - Gustafson's law: https://en.wikipedia.org/wiki/Gustafson%27s_law
      - Gustafson's Law (also known as Gustafson–Barsis' law) is a law in computer science which says that computations involving arbitrarily large data sets can be efficiently parallelized.
  - Parallel slowdown: https://en.wikipedia.org/wiki/Parallel_slowdown
    - Parallel slowdown is a phenomenon in parallel computing where parallelization of a parallel algorithm beyond a certain point causes the program to run slower (take more time to run to completion).
  - Embarrassingly parallel: https://en.wikipedia.org/wiki/Embarrassingly_parallel
    - 不易并行
    - In parallel computing, an embarrassingly parallel workload, or embarrassingly parallel problem, is one for which little or no effort is required to separate the problem into a number of parallel tasks. This is often the case where there exists no dependency (or communication) between those parallel tasks.
- Multiprocessing：https://en.wikipedia.org/wiki/Multiprocessing
  - Multiprocessing is the use of two or more central processing units (CPUs) within a single computer system.
  - The term also refers to the ability of a system to support more than one processor and/or the ability to allocate tasks between them.
  - There are many variations on this basic theme, and the definition of multiprocessing can vary with context, mostly as a function of how CPUs are defined (multiple cores on one die, multiple dies in one package, multiple packages in one system unit, etc.).
  - Multi-core processor: https://en.wikipedia.org/wiki/Multi-core_processor
    - A multi-core processor is a single computing component with two or more independent actual processing units (called "cores"), which are the units that read and execute program instructions.
  - SMP：https://en.wikipedia.org/wiki/Symmetric_multiprocessing
    - Symmetric multiprocessing (SMP) involves a symmetric multiprocessor system hardware and software architecture where two or more identical processors connect to a single, shared main memory, have full access to all I/O devices, and are controlled by a single operating system instance that treats all processors equally, reserving none for special purposes.
    - Most multiprocessor systems today use an SMP architecture.
  - AMP: https://en.wikipedia.org/wiki/Asymmetric_multiprocessing
    - Asymmetric multiprocessing (AMP) was a software stopgap for handling multiple CPUs before symmetric multiprocessing (SMP) was available.
    - It has also been used to provide less expensive options on systems where SMP was available.
    - In an asymmetric multiprocessing system, not all CPUs are treated equally; for example, a system might only allow (either at the hardware or operating system level) one CPU to execute operating system code or might only allow one CPU to perform I/O operations. Other AMP systems would allow any CPU to execute operating system code and perform I/O operations, so that they were symmetric with regard to processor roles, but attached some or all peripherals to particular CPUs, so that they were asymmetric with regard to peripheral attachment.

    - Heterogeneous computing: https://en.wikipedia.org/wiki/Heterogeneous_computing
        - Heterogeneous computing refers to systems that use more than one kind of processor.
        - These are systems that gain performance not just by adding the same type of processors, but by adding dissimilar processors, usually incorporating specialized processing capabilities to handle particular tasks.
- Load balancing: https://en.wikipedia.org/wiki/Load_balancing_(computing)
    - In computing, load balancing distributes workloads across multiple computing resources, such as computers, a computer cluster, network links, central processing units or disk drives. Load balancing aims to optimize resource use, maximize throughput, minimize response time, and avoid overload of any single resource.
    - Processor affinity：https://en.wikipedia.org/wiki/Processor_affinity
        - Processor affinity, or CPU pinning enables the binding and unbinding of a process or a thread to a central processing unit (CPU) or a range of CPUs, so that the process or thread will execute only on the designated CPU or CPUs rather than any CPU.
        - On Linux, the CPU affinity of a process can be altered with the taskset(1) program and the sched_setaffinity(2) system call. The affinity of a thread can be altered with one of the library functions: pthread_setaffinity_np(3) or pthread_attr_setaffinity_np(3).
- Mpstat: https://en.wikipedia.org/wiki/Mpstat
    - mpstat is a computer command-line software used in unix-type operating systems to report (on the screen) processor related statistics. It is used in computer monitoring in order to diagnose problems or to build statistics about a computer's CPU usage.
        - `sudo apt-get install sysstat`
        - `mpstat`

自学：

1. Parallel computing: https://en.wikipedia.org/wiki/Parallel_computing
2. Task parallelism: https://en.wikipedia.org/wiki/Task_parallelism
3. Scalable parallelism: https://en.wikipedia.org/wiki/Scalable_parallelism
4. Parallel slowdown: https://en.wikipedia.org/wiki/Parallel_slowdown
5. Embarrassingly parallel: https://en.wikipedia.org/wiki/Embarrassingly_parallel
6. Multiprocessing：https://en.wikipedia.org/wiki/Multiprocessing
7. Multi-core processor: https://en.wikipedia.org/wiki/Multi-core_processor
8. SMP：https://en.wikipedia.org/wiki/Symmetric_multiprocessing
9. AMP: https://en.wikipedia.org/wiki/Asymmetric_multiprocessing
10. Heterogeneous computing: https://en.wikipedia.org/wiki/Heterogeneous_computing
11. Load balancing: https://en.wikipedia.org/wiki/Load_balancing_(computing)
12. Processor affinity：https://en.wikipedia.org/wiki/Processor_affinity
13. Mpstat: https://en.wikipedia.org/wiki/Mpstat

其它建议内容

- Intel 80386 Reference Programmer's Manual:
    - http://pdos.csail.mit.edu/6.828/2005/readings/i386/toc.htm
- NX bit：https://en.wikipedia.org/wiki/NX_bit
    - The NX bit, which stands for No-eXecute, is a technology used in CPUs to segregate areas of memory for use by either storage of processor instructions (code) or for storage of data, a feature normally only found in Harvard architecture processors. However, the NX bit is being increasingly used in conventional von Neumann architecture processors, for security reasons.
- Trap: https://en.wikipedia.org/wiki/Trap_(computing)
    - In computing and operating systems, a trap, also known as an exception or a fault, is typically a type of synchronous interrupt typically caused by an exceptional condition (e.g., breakpoint, division by zero, invalid memory access).
- Addressing mode: https://en.wikipedia.org/wiki/Addressing_mode
    - Addressing modes are an aspect of the instruction set architecture in most central processing unit (CPU) designs. The various addressing modes that are defined in a given instruction set architecture define how machine language instructions in that architecture identify the operand(s) of each instruction. An addressing mode specifies how to calculate the effective memory address of an operand by using information held in registers and/or constants contained within a machine instruction or elsewhere.
- Orthogonal instruction set：https://en.wikipedia.org/wiki/Orthogonal_instruction_set
    - In computer engineering, an orthogonal instruction set is an instruction set architecture where all instruction types can use all addressing modes.
    - It is "orthogonal" in the sense that the instruction type and the addressing mode vary independently.
    - An orthogonal instruction set does not impose a limitation that requires a certain instruction to use a specific register.