Vivado从此开始（To Learn Vivado From Here）

Vivado
从此开始
To Learn Vivado From Here
高亚军 编著
· 内容翔实全面：涵盖Vivado所有基本功能
· 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
· 描述图文并茂：给出具体操作步骤，易于快速动手实践
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本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

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XILINX

ALL PROGRAMMABLE™

TCL, Vivado One World
Part 2

Lauren Gao

Some Items Should Be Cared

- How to get large fanout net
- How to get timing report through large fanout net
- How to confirm BUFG available

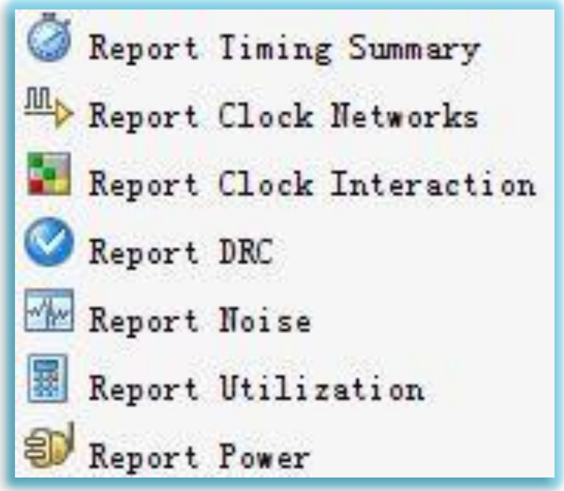
Agenda

- TCL background from Vivado view
- Edit synthesized netlist with TCL in Vivado
- **Customize various reports with TCL in Vivado**
- Interact with Vivado by TCL

Various Reports in Vivado

- **Various reports generated by Vivado GUI**
  - Report timing summary: `report_timing_summary`
  - Report clock interaction: `report_clock_interaction`
  - Report utilization: `report_utilization`
  - Report Power: `report_power`
- **Other useful reports generated by Vivado TCL**
  - Report clocks: `report_clocks`
  - Report clock utilization: `report_clock_utilization`
  - Report timing for customerized path: `report_timing`
  - Report high fanout nets: `report_high_fanout_nets`
  - Report control sets: `report_control_sets`
  - Report IP status: `report_ip_status`
  - Report power optimizations: `report_power_opt`
  - Report design analysis: `report_design_analysis`
  - Report cross domain clocks: `report_cdc`

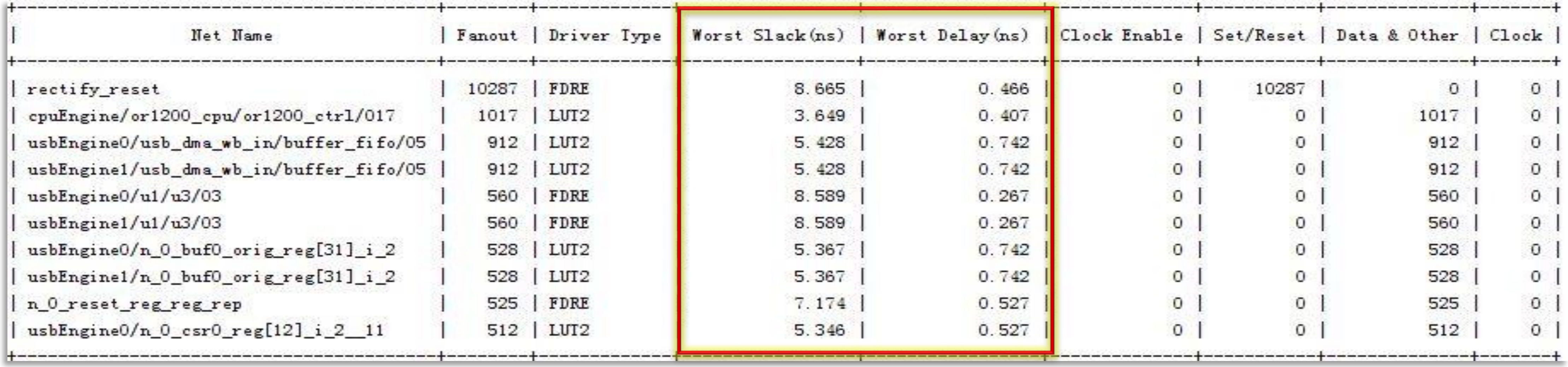
Vivado 2014.3



They are very useful for design analysis!

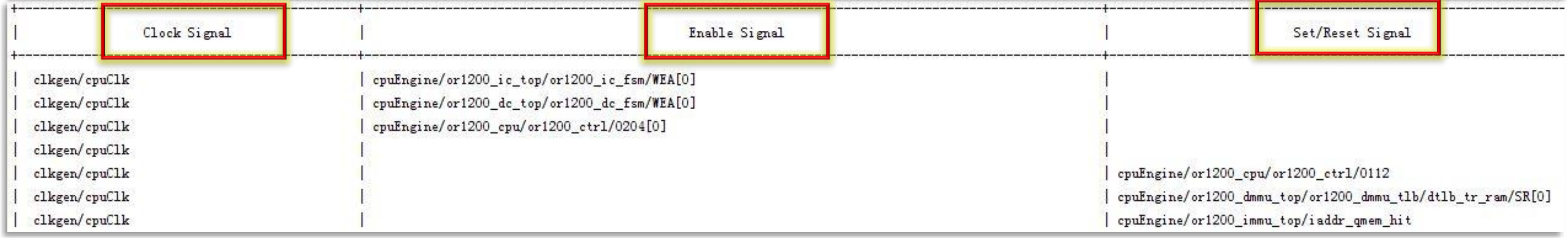
Report High Fanout Nets and Control Sets

```
report_high_fanout_nets -min_fanout 500 -timing -load_types
```



```
+------------------------------------------+--------+-------------+----------------+----------------+--------------+-----------+--------------+-------+
|                 Net Name                 | Fanout | Driver Type | Worst Slack(ns) | Worst Delay(ns) | Clock Enable | Set/Reset | Data & Other | Clock |
+------------------------------------------+--------+-------------+----------------+----------------+--------------+-----------+--------------+-------+
| rectify_reset                            |  10287 | FDRE        |          8.665 |          0.466 |            0 |     10287 |            0 |     0 |
| cpuEngine/or1200_cpu/or1200_ctrl/017     |   1017 | LUT2        |          3.649 |          0.407 |            0 |         0 |         1017 |     0 |
| usbEngine0/usb_dma_wb_in/buffer_fifo/05  |    912 | LUT2        |          5.428 |          0.742 |            0 |         0 |          912 |     0 |
| usbEngine1/usb_dma_wb_in/buffer_fifo/05  |    912 | LUT2        |          5.428 |          0.742 |            0 |         0 |          912 |     0 |
| usbEngine0/u1/u3/03                      |    560 | FDRE        |          8.589 |          0.267 |            0 |         0 |          560 |     0 |
| usbEngine1/u1/u3/03                      |    560 | FDRE        |          8.589 |          0.267 |            0 |         0 |          560 |     0 |
| usbEngine0/n_0_buf0_orig_reg[31]_i_2     |    528 | LUT2        |          5.367 |          0.742 |            0 |         0 |          528 |     0 |
| usbEngine1/n_0_buf0_orig_reg[31]_i_2     |    528 | LUT2        |          5.367 |          0.742 |            0 |         0 |          528 |     0 |
| n_0_reset_reg_reg_rep                    |    525 | FDRE        |          7.174 |          0.527 |            0 |         0 |          525 |     0 |
| usbEngine0/n_0_csr0_reg[12]_i_2__11      |    512 | LUT2        |          5.346 |          0.527 |            0 |         0 |          512 |     0 |
+------------------------------------------+--------+-------------+----------------+----------------+--------------+-----------+--------------+-------+
```

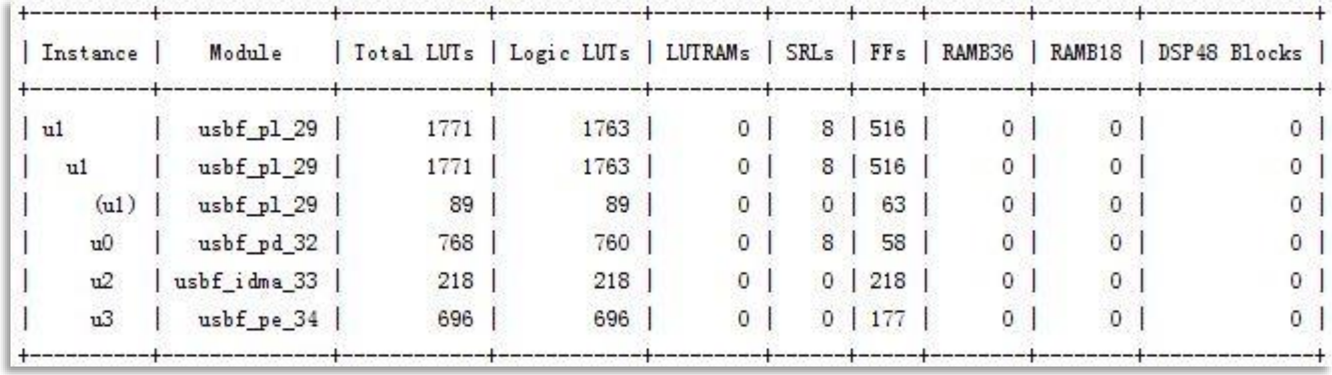
```
report_control_sets -verbose -sort_by {clk set}
```



```
+----------------------------------+------------------------------------------------------------+-----------------------------------------------------------------
|          Clock Signal            |                      Enable Signal                         |                      Set/Reset Signal
+----------------------------------+------------------------------------------------------------+-----------------------------------------------------------------
|  clkgen/cpuClk                   | cpuEngine/or1200_ic_top/or1200_ic_fsm/WEA[0]               |
|  clkgen/cpuClk                   | cpuEngine/or1200_dc_top/or1200_dc_fsm/WEA[0]               |
|  clkgen/cpuClk                   | cpuEngine/or1200_cpu/or1200_ctrl/0204[0]                   |
|  clkgen/cpuClk                   |                                                            |
|  clkgen/cpuClk                   |                                                            | cpuEngine/or1200_cpu/or1200_ctrl/0112
|  clkgen/cpuClk                   |                                                            | cpuEngine/or1200_dmmu_top/or1200_dmmu_tlb/dtlb_tr_ram/SR[0]
|  clkgen/cpuClk                   |                                                            | cpuEngine/or1200_immu_top/iaddr_qmem_hit
```

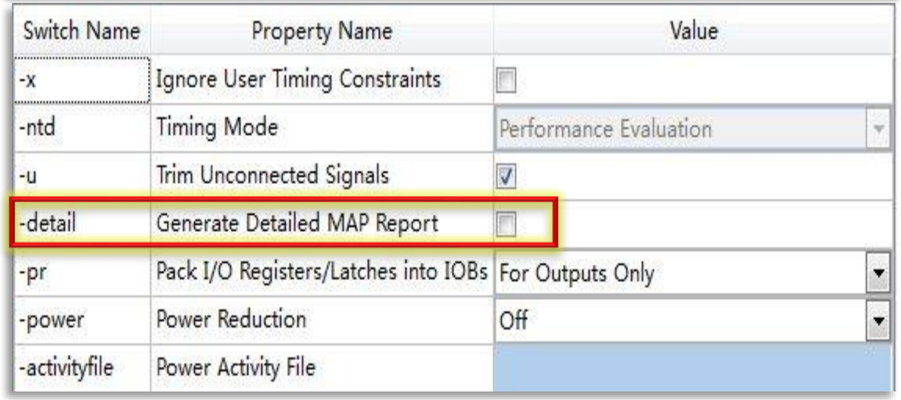
Customizable Utilization Reports

```
report_utilization -hierarchical -cells [get_cells usbEngine0/u1]
```



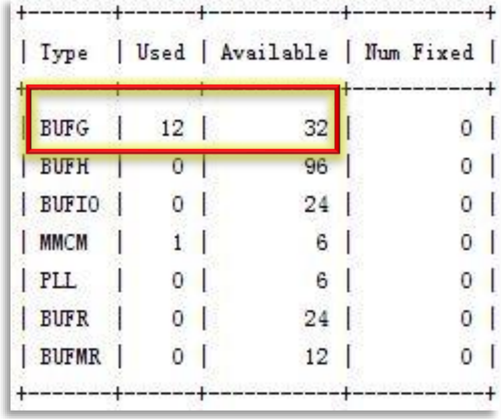
```
+----------+-------------+------------+------------+---------+------+-----+--------+--------+--------------+
| Instance |    Module   | Total LUTs | Logic LUTs | LUTRAMs | SRLs | FFs | RAMB36 | RAMB18 | DSP48 Blocks |
+----------+-------------+------------+------------+---------+------+-----+--------+--------+--------------+
| u1       |  usbf_pl_29 |       1771 |       1763 |       0 |    8 | 516 |      0 |      0 |            0 |
|   u1     |  usbf_pl_29 |       1771 |       1763 |       0 |    8 | 516 |      0 |      0 |            0 |
|     (u1) |  usbf_pl_29 |         89 |         89 |       0 |    0 |  63 |      0 |      0 |            0 |
|     u0   |  usbf_pd_32 |        768 |        760 |       0 |    8 |  58 |      0 |      0 |            0 |
|     u2   | usbf_idma_33 |       218 |        218 |       0 |    0 | 218 |      0 |      0 |            0 |
|     u3   |  usbf_pe_34 |        696 |        696 |       0 |    0 | 177 |      0 |      0 |            0 |
+----------+-------------+------------+------------+---------+------+-----+--------+--------+--------------+
```

ISE



Switch Name	Property Name	Value
-x	Ignore User Timing Constraints	□
-ntd	Timing Mode	Performance Evaluation
-u	Trim Unconnected Signals	☑
-detail	Generate Detailed MAP Report	□
-pr	Pack I/O Registers/Latches into IOBs	For Outputs Only
-power	Power Reduction	Off
-activityfile	Power Activity File	

```
report_clock_utilization
```



```
+-------+------+-----------+-----------+
| Type  | Used | Available | Num Fixed |
+-------+------+-----------+-----------+
| BUFG  |   12 |        32 |         0 |
| BUFH  |    0 |        96 |         0 |
| BUFIO |    0 |        24 |         0 |
| MMCM  |    1 |         6 |         0 |
| PLL   |    0 |         6 |         0 |
| BUFR  |    0 |        24 |         0 |
| BUFMR |    0 |        12 |         0 |
+-------+------+-----------+-----------+
```

- In ISE, generating module resource utilization only with ‘Generate Detailed Map Report’ checked in MAP property panel
- In ISE, clock utilization is only available in resource utilization and cannot be generated separately
- In Vivado, you can generate prolific and customizable reports with TCL

Customizable Timing Reports

```
# Description: -through: net pin or cell
# Use -through to get timing path and report timing
proc thr_timing_rpt {ListOfEmt} {
  puts [format {%-40s %-40s %-20s %-20s %7s} "Start Point" "End point" "Launch Clock" "Capture Clock" "Slack"]
  puts [string repeat "-" 140]
  set path [list]
  set class_type [list net cell pin]
  foreach thr_opt $ListOfEmt {
    set class [get_property CLASS $thr_opt]
    if {[lsearch $class_type $class]==-1} {
      puts "Error: -through opt must be net, cell or pin!"
      return 1
    }
    set path_i [get_timing_paths -through $thr_opt -nworst 100 -unique_pins]
    lappend path $path_i
  }
  foreach mypath $path {
    set startpoint [get_property STARTPOINT_PIN $mypath]
    set startclock [get_property STARTPOINT_CLOCK $mypath]
    set endpoint [get_property ENDPOINT_PIN $mypath]
    set endclock [get_property ENDPOINT_CLOCK $mypath]
    set slack [get_property SLACK $mypath]
    puts [format {%-40s %-40s %-20s %-20s %7s} $startpoint $endpoint $startclock $endclock $slack]
  }
}
```

➢ **More useful options in report_timing and get_timing_paths**

- -from
- -to
- -through
- -delay_type
- -max_paths
- -nworst
- -unique_pins
- -sort_by
- -slack_lesser_than

Agenda

- TCL background from Vivado view
- Edit synthesized netlist with TCL in Vivado
- Customize various reports with TCL in Vivado
- **Interact with Vivado by TCL**

Pack I/O Registers into IOB

- In ISE, ‘Pack I/O registers into IOBs’ is available in map property. There are four options: For Inputs Only, For Outputs Only, For Inputs and Outputs, Off
- In Vivado, it is more flexible with TCL
  - Pack input registers into IOBs for specified ports

```
set_property IOB true [all_fanout -flat -endpoints_only -only_cells [get_ports lb_sel_pin]]
set_property IOB true [get_ports lb_sel_pin]
```

  - Pack all input registers into IOBs

```
set_property IOB true [all_fanout -flat -endpoints_only -only_cells [all_inputs]]
set_property IOB true [all_inputs]
```

  - Pack output registers into IOBs for specified ports

```
set_property IOB true [all_fanin -only_cells -startpoints_only -flat [get_ports led_pins[0]]]
set_property IOB true [get_ports led_pins[0]]
```

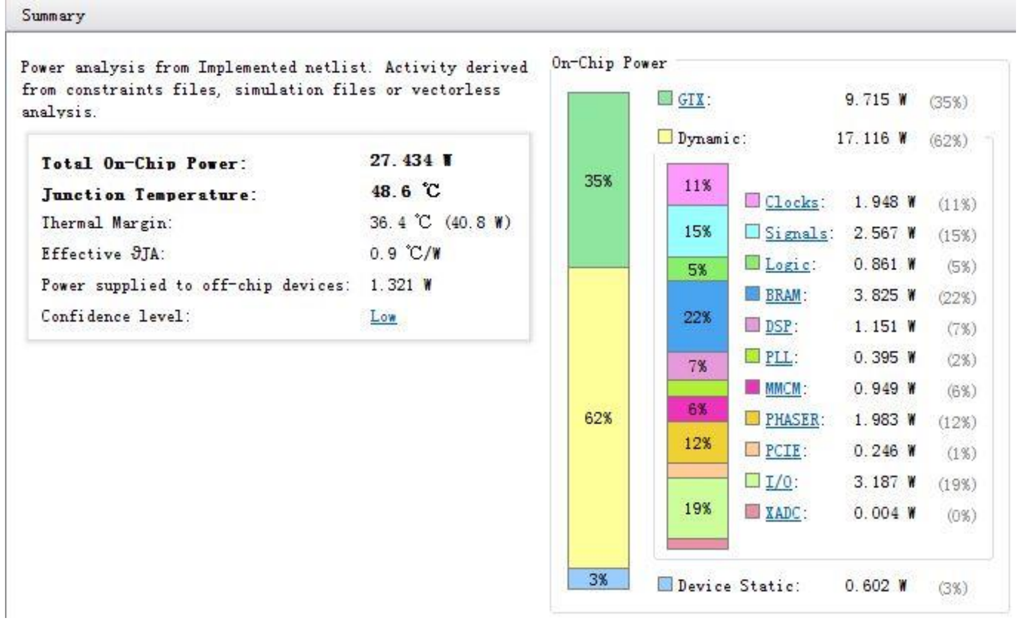
  - Pack all output registers into IOBs

```
set_property IOB true [all_fanin -flat -startpoints_only -only_cells [all_outputs]]
set_property IOB true [all_outputs]
```

set_property

Set Power Optimization

- Estimate power at any stage after synthesis
- Vector and vector less modes are available
- Power optimization
  - Maximize power optimization
  - Minimize its impact on timing
- Set power opt except BRAM in critical path
  - `set_power_opt -exclude_cells [get_cells alu/store_ram]`
- Set power opt for specified clock region
  - `set_power_opt -clocks [get_clocks rx_clk]`
- Set power opt for specified type cells
  - `set_power_opt -cell_types {bram reg}`



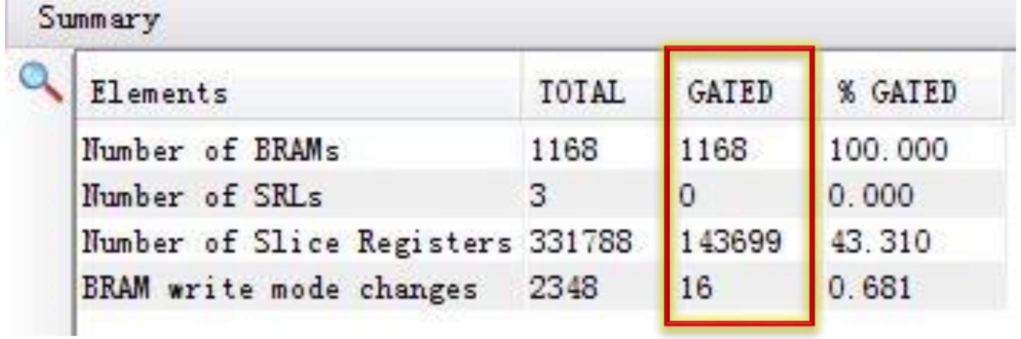
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**27.434 W**
Junction Temperature:	**48.6 ℃**
Thermal Margin:	36.4 ℃ (40.8 W)
Effective ϑJA:	0.9 ℃/W
Power supplied to off-chip devices:	1.321 W
Confidence level:	Low

On-Chip Power

GTX:	9.715 W	(35%)
Dynamic:	17.116 W	(62%)
Clocks:	1.948 W	(11%)
Signals:	2.567 W	(15%)
Logic:	0.861 W	(5%)
BRAM:	3.825 W	(22%)
DSP:	1.151 W	(7%)
PLL:	0.395 W	(2%)
MMCM:	0.949 W	(6%)
PHASER:	1.983 W	(12%)
PCIE:	0.246 W	(1%)
I/O:	3.187 W	(19%)
XADC:	0.004 W	(0%)
Device Static:	0.602 W	(3%)

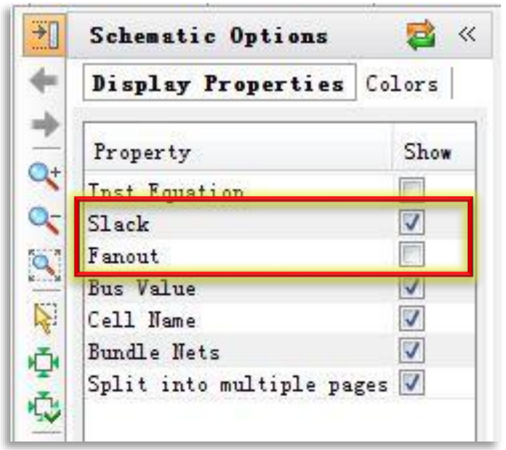


Summary

Elements	TOTAL	GATED	% GATED
Number of BRAMs	1168	1168	100.000
Number of SRLs	3	0	0.000
Number of Slice Registers	331788	143699	43.310
BRAM write mode changes	2348	16	0.681

Work with Vivado Schematic View

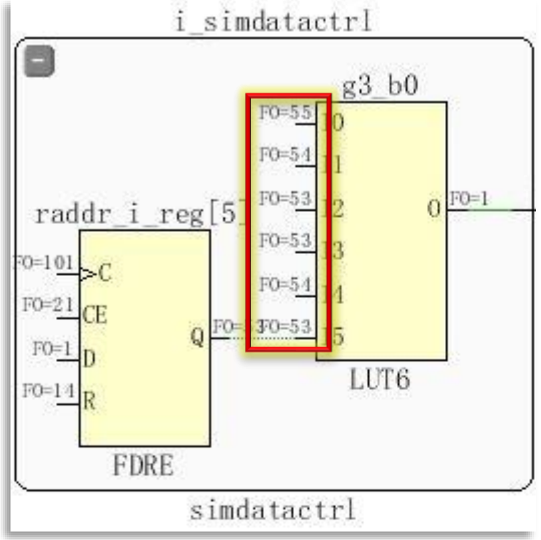
- Gets the objects currently selected in the Vivado IDE
  - `get_selected_objects`
- Selects the specified object in the appropriate open views in the GUI mode
  - `select_objects`
- Unselects the specified object or objects that were previously selected
  - `unselect_objects`
- Hot-key
  - `F4: Generate schematic; F6: Show hierarchy; F7: Go to source; F12: Unselect all`

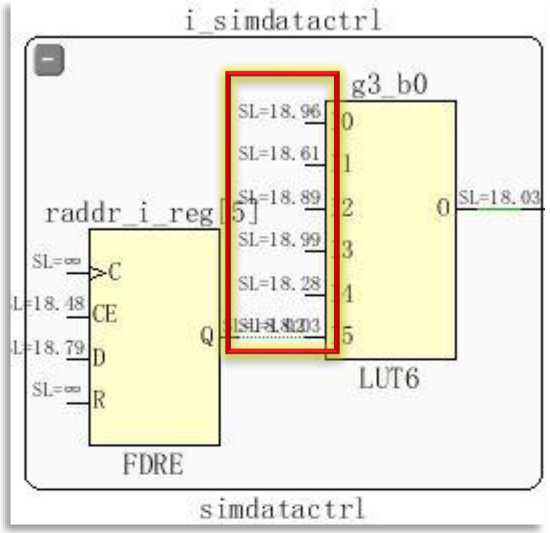


Schematic Options

Display Properties | Colors

Property	Show
Inst Equation	☐
Slack	☑
Fanout	☐
Bus Value	☑
Cell Name	☑
Bundle Nets	☑
Split into multiple pages	☑





Summary

- **TCL make Vivado more POWERFUL**
  - You can do what ISE cannot do
- **TCL make Vivado more FLEXIBLE**
  - You can do better what ISE can do
- **TCL make Vivado more INTERACTIVE**
  - You can switch between GUI and TCL smoothly