Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

UltraFast Design
Basic Introduction

Lauren Gao

What is UltraFast?

- **Documented Design Methodology to Improve Designer Productivity**
  - Methodology Recommendations
  - Best practices
  - Checklist

- **Customer Benefits**
  - Faster time to market
  - Better QoR & runtimes
  - Less time with their favorite FAE

UltraFAST™
Design Methodology
for Vivado Design Suite

The smarter way for:

- ✓ **PCB planning**
- ✓ **HDL Coding**
- ✓ **Design Closure**
  - XDC Constraints
  - Design Analysis
  - Timing Closure

v1.0

UltraFast collection of best-practices

- **Created by FAEs/SAEs from all over the world**
  - Collection of best practices
  - Things to avoid
  - Knowledge is provided in the form of UG949, Checklists and scripts.

- **"It's good to learn from your mistakes"**

- **"It's much better to learn from other people**

UltraFAST™

Design Methodology Guide for the Vivado Design Suite

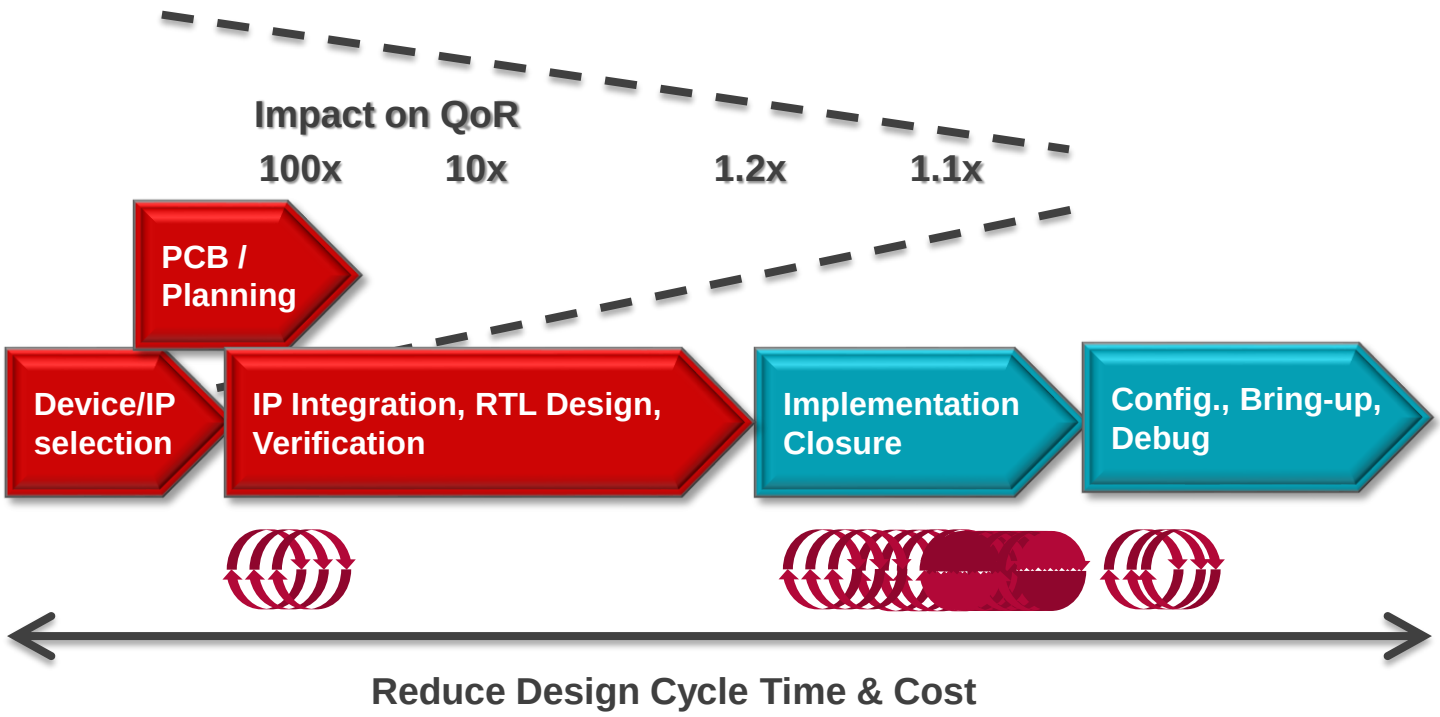
UltraFast Methodology: Why Now?

- **Device Density has been increasing exponentially**
  - FPGAs are as large as ASICs were a few years ago
  - Complexity of designs are increasing significantly
  - FPGAs are the center of the system, not just "glue-logic"
  - Proper frontend and backend methodology is essential for project success

- **Vivado**
  - Enables easy validation of constraints
  - Powerful timing analysis
  - Full featured DRC checks
  - Superior design analysis capabilities
  - Tcl access to complete design database
  - ASIC-class FPGA tool, designed to handle these large FPGAs

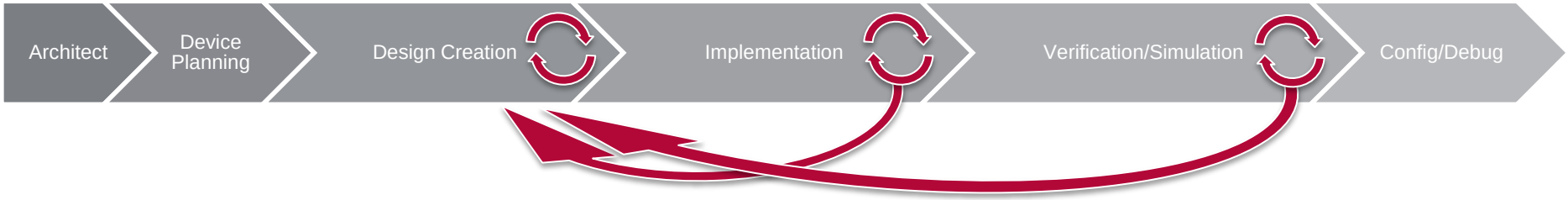
Overall Strategy for UltraFAST Design:
Earlier Iterations

- Upfront analysis
- Design closure at each step

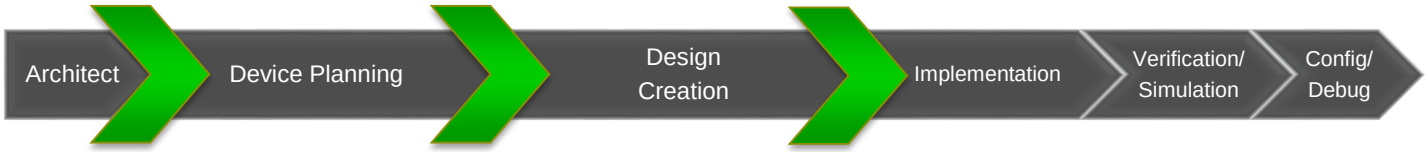


Customer Advantage

- **Normal Development Cycle**
  - Longer debug cycle
  - Non-deterministic debug



- **UltraFast Design Methodology Development Cycle**
  - Shorter debug cycle
  - More deterministic debug



Process Review Steps

UltraFast Checklists