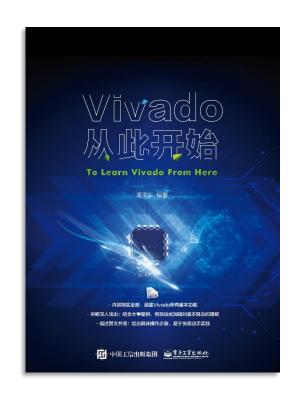
Vivado从此开始(To Learn Vivado From Here)



本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用



作者: 高亚军 (Xilinx战略应用高级工程师)

- · 2012年2月,出版《基于FPGA的数字信号处理(第1版)》
- · 2012年9月,发布网络视频课程《Vivado入门与提高》
- · 2015年7月,出版《基于FPGA的数字信号处理(第2版)》
- 2016年7月,发布网络视频课程《跟Xilinx SAE学HLS》
- ◆ 内容翔实全面:涵盖Vivado所有基本功能
- ◆ 讲解深入浅出:结合大量案例,帮助读者加强对基本概念的理解
- ◆ 描述图文并茂: 给出具体操作步骤, 易于快速动手实践



Using Design Rule Checks in Vivado

Lauren Gao

DRC Methodology

- ➤ Always run DRC early in the flow
- > Run DRC after each major design step
 - After Elaborate
 - After Synthesis
 - After Implementation
- > Fix Critical Warnings and Errors before proceeding to next step

Rule Decks

Elaborated Design



Synthesized Design

```
All Rules (4530)

Provided Pro
```

Implemented Design

```
All Rule (4531)

Placer (125)

Pin Planning (70)

My DRC System (1)

My Implementation (31)

My Floorplan (9)

My Partial Reconfiguration (1)

My Clocking (2)

My Memory (38)

My Physical Configuration (2859)

Posting (1)

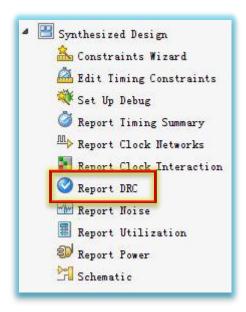
NOTE: Configuration (2859)
```

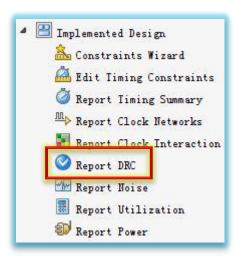
Invoking Methodology Check

Design Stages	methodology_checks		timing chocks
	RTL	XDC	timing_checks
Elaborated Design	√	√	
Synthesized Design		√	√
Implemented Design		√	√



Tcl: report_drc





DEMO

Summary

- ➤ Always run DRC early in the flow
- > Run DRC after each major design step
- > Fix Critical Warnings and Errors before proceeding to next step