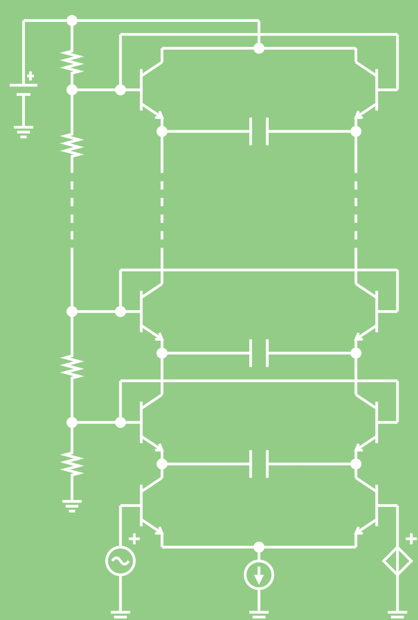
Department of Signal Processing and Acoustics

Virtual Analog Modeling of Nonlinear Musical Circuits

Stefano D'Angelo



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Virtual Analog Modeling of Nonlinear Musical Circuits

Stefano D'Angelo

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Abstract

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Abstract

Recent advances in semiconductor technology eventually allowed for affordable and pragmatic implementations of sound processing algorithms based on physical laws, leading to considerable interest towards research in this area and vast amounts of literature being published in the last two decades.

As of today, despite the efforts invested by the academic community and the music technology industry, new or better mathematical and computational tools are called for to efficiently cope with a relatively large subset of the investigated problem domain. This is especially true of those analog devices that inherently need to be studied by lumped nonlinear models. This research is, in this sense, directed towards both general techniques and specific problems.

The first part of this thesis presents a generalization of the *wave digital filter* (WDF) theory to enable interconnections among subnetworks using different polarity and sign conventions. It proposes two new non-energic two-port WDF adaptors, as well as an extension to the definitions of absorbed instantaneous and steady-state pseudopower. This technique eventually removes the need to remodel subcircuits exhibiting asymmetrical behavior. Its correctness is also verified in a case study. Furthermore, a novel, general, and non-iterative delay-free loop implementation method for nonlinear filters is presented that preserves their linear response around a chosen operating point and that requires minimal topology modifications and no transformation of nonlinearities.

In the second part of this work, five nonlinear analog devices are analyzed in depth, namely the common-cathode triode stage, two guitar distortion circuits, the Buchla lowpass gate, and a generalized version of the Moog ladder filter. For each of them, new real-time simulators are defined that accurately reproduce their behavior in the digital domain. The first three devices are modeled by means of WDFs with a special emphasis on faithful emulation of their distortion characteristics, while the last two are described by novelly-derived systems in Kirchhoff variables with focus on retaining the linear response of the circuits. The entirety of the proposed algorithms is suitable for real-time execution on computers, mobile electronic devices, and embedded DSP systems.

Keywords Acoustic signal processing, digital filters, digital signal processing, circuit simulation, nonlinear systems, real-time systems

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Preface

This work is the main result of three intense years of study and research carried out at the Laboratory of Acoustics and Audio Signal Processing. It is impossible for me to even vaguely express what this time meant for me in a couple of lines, so I rather refrain and apologize with the reader. I take, anyway, the opportunity to thank the people who accompained me in this journey.

My gratitude certainly goes to my supervisor, Prof. Vesa Välimäki, for the invaluable guidance and support he provided me. I am sure that this thesis would have never seen the light without his help. I am also deeply grateful to the other three coauthors of the publications, Jyri Pakarinen, Rafael Cauduro Dias de Paiva, and Julian Parker, to whom I not only acknowledge indisputable technical skills, but also high human qualities.

This thesis has been made possible by the financial support provided by the Centre for International Mobility (CIMO), the Research Foundation of the Helsinki University of Technology, the Graduate School in Electronics, Telecommunications and Automation (GETA), and the Aalto ELEC Doctoral School. Thanks also to Luis de Jussilainen Costa for having helped in improving the language of this thesis.

I want to express immense gratitude, and this is by no means a hyperbole, to Symeon Delikaris-Manias, Archontis Politis, Thanassis Gotsopoulos, Rosario Fina, and Elisa Di Fiore, for their endless support and for making me feel at home more than three thousand kilometers away from where I grew up. I also dedicate special and heartfelt thanks to Henna Tahvanainen, Essi Kärkkäinen, Xrysa Panayiotopoulou, Alessandro Altoè, Roberta Zaetta, Kimmo Söderholm, and Vassiliki Pitsa, who "contributed significant material", in their own ways and probably without even noticing, for me to see this world as much less of a miserable place.

In the end, I want to thank all of the people I met at the Department of Signal Processing and Acoustics, especially for tolerating my evident eccentricity, and the many friends I made while living in Helsinki.

Agropoli, Italy, October 15, 2014,

Stefano D'Angelo

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I J. Parker and S. D'Angelo. A Digital Model of the Buchla Lowpass-Gate. In *Proc. 16th Intl. Conf. Digital Audio Effects (DAFx-13)*, pp. 278–285, Maynooth, Ireland, September 2013.

II S. D'Angelo and V. Välimäki. Wave-Digital Polarity and Current Inverters and Their Application to Virtual Analog Audio Processing. In *Proc. Intl. Conf. Acoustics, Speech, and Signal Process. (ICASSP 2012)*, pp. 469–472, Kyoto, Japan, March 2012.

III S. D'Angelo, J. Pakarinen, and V. Välimäki. New Family of Wave-Digital Triode Models. *IEEE Trans. Audio, Speech, and Lang. Process.*, vol. 21, no. 2, pp. 313–321, February 2013.

IV R. C. D. de Paiva, S. D'Angelo, J. Pakarinen, and V. Välimäki. Emulation of Operational Amplifiers and Diodes in Audio Distortion Circuits. *IEEE Trans. Circ. Systems–II: Express Briefs*, vol. 59, no. 10, pp. 688–692, October 2012.

V S. D'Angelo and V. Välimäki. Generalized Moog Ladder Filter: Part I – Linear Analysis and Parameterization. *IEEE Trans. Audio, Speech, and Lang. Process.*, vol. 22, no. 12, pp. 1825–1832, December 2014.

VI S. D'Angelo and V. Välimäki. Generalized Moog Ladder Filter: Part II – Explicit Nonlinear Model through a Novel Delay-Free Loop Implementation Method. *IEEE Trans. Audio, Speech, and Lang. Process.*, vol. 22, no. 12, pp. 1873–1883, December 2014.

Author's Contribution

Publication I: "A Digital Model of the Buchla Lowpass-Gate"

The author and co-author planned this study. The author analyzed, simulated, modeled, and developed digital approximations of the control circuit. He also wrote Subsection 3.1.

Publication II: "Wave-Digital Polarity and Current Inverters and Their Application to Virtual Analog Audio Processing"

The author and co-author planned this study. The author derived the formulations for inverter components and absorbed pseudopower definitions; designed, implemented, and evaluated the case study; and wrote the paper.

Publication III: "New Family of Wave-Digital Triode Models"

The author planned this study in collaboration with the co-authors. The author designed, derived, implemented, and evaluated both the WDF tube model and the case study simulator. He also wrote Sections III, V, and VI.

Publication IV: "Emulation of Operational Amplifiers and Diodes in Audio Distortion Circuits"

The author derived WDF models for single and antiparallel diodes and wrote Section III.

Publication V: "Generalized Moog Ladder Filter: Part I – Linear Analysis and Parameterization"

The author and co-author planned this study. The author derived and analyzed the circuit model; designed, derived, implemented, and evaluated the digital model; and wrote the entire paper.

Publication VI: "Generalized Moog Ladder Filter: Part II – Explicit Nonlinear Model through a Novel Delay-Free Loop Implementation Method"

The author and co-author planned this study. The author designed and derived the delay-free loop implementation technique. He also designed, derived, implemented, and evaluated the digital model, and wrote the entire paper.

List of Symbols

a	WD incident wave
b	WD reflected wave
f_{s}	Sample rate
$\mathbf{i}$	SS nonlinear mapping output vector
I	Electrical current
$\mathbf{J}$	MNA current excitation vector
n	Discrete-time variable
R_0	WD port resistance
s	Laplace variable
$S(s)$	WD port reflectance
t	Continuous-time variable
$\mathbf{u}$	SS input vector
$\mathbf{v}$	SS nonlinear mapping input vector
V	Electrical voltage
$\mathbf{V}_{\mathrm{n}}$	MNA vector of ungrounded node voltages
$\mathbf{x}$	SS state vector
$\mathbf{y}$	SS output vector
$\mathbf{Y}$	MNA nodal admittance matrix
$Z(s)$	WD port impedance

List of Abbreviations

ASTAP	Advanced Statistical Analysis Program
BCT	Binary connection tree
BJT	Bipolar junction transistor
CANCER	Computer Analysis of Nonlinear Circuits, Excluding Radiation
DAE	Differential algebraic equation
DC	Direct current
DSP	Digital signal processing
LDR	Light-dependent resistor
LED	Light-emitting diode
LTI	Linear time-invariant
MIMO	Multiple-input multiple-output
MNA	Modified nodal analysis
PHS	Port-Hamiltonian system
Q	Quality
RT	Real-time
SISO	Single-input single-output
SPICE	Simulation Program with Integrated Circuit Emphasis
SS	State-space
TDF-II	Transposed-direct-form-II
VA	Virtual analog
WD	Wave-digital
WDF	Wave digital filter

1. Introduction

Analog electrical devices have been extensively utilized for music production in the past century to the point that still today they are in many cases preferred to their digital counterparts, also, if not particularly, by professional users. Such a phenomenon stands in sharp contrast with the opposite trend that characterized the vast majority of electrical engineering applications and that led to improved flexibility, performance, and reliability, as well as reduced costs in these areas. While it is possible to speculate that this may be partly due to aesthetical fashion or even subjective psychological factors bearing no relation to factual reality, nevertheless the vastness of current scientific research devoted to the topic suffices to show how accurate reproduction of the so-called *analog feel* of the original devices through software algorithms often presents major challenges.

Such attempts to emulate whole or part of analog devices, as well as the specific techniques developed for this particular purpose, are usually referred to as *virtual analog* (VA) *modeling* [1, 2, 3, 4]. Research has been conducted on countless circuits, including synthesizer oscillators [5, 6, 7] and filters [8, 9, 10, 11], electronic musical instrument circuitry [12, 13, 14], whole guitar amplifiers [15, 16] and parts of them [17, 18, 19, 20, 21], equalizers [22, 23], ring modulators [24, 25, 26], analog echo/delay [27, 28], modulation [29, 30, 31], distortion [32, 33, 15, 34], compressor/limiter [35, 36, 37, 38], plate [39, 40] and spring reverb [41, 42, 43] effects, and other vintage devices [44, 45, 46]. As an example, Figure 1.1 shows a photograph of a well-known analog synthesizer and a user interface screenshot of a VA emulator of the device.

Several more or less generic modeling and implementation methods have also emerged, which can be somewhat fuzzily classified as either being *black-box*, when they do not rely on knowledge of the internal work-

(a) (b)

Figure 1.1. (a) Photograph of the original Minimoog Voyager synthesizer (image in the public domain) and (b) screenshot of the user interface of the Bristol Moog Voyager MIDI-controlled VA emulator[1] (image copyright by Nick Copeland, used with permission).

ings of the emulated system and thus only consider input-output relationships, or *white-box*, when the specularly opposite principle is employed. The term *gray-box* is sometimes used to qualify those methods that mix the two approaches [47, 15]. Among the proposed techniques belonging to the former category, it is worth mentioning amplitude-dependent convolution methods [48, 49, 50], Volterra/Wiener/Hammerstein models [51, 52, 53, 54], neural networks [55, 56, 57], differential decomposition [58], even mirror Fourier nonlinear filters [59], and Legendre nonlinear filters [60]. The latter class includes numerical methods for solving differential equations [8, 61, 24, 33], the port-Hamiltonian approach introduced in [62], techniques based on the *state-space* (SS) formalism, such as the K-method [63] and derivatives [64, 65, 19], *wave digital filters* (WDFs) [66, 67, 68, 69], and delay-free loop implementation techniques [70, 71, 72, 73].

This thesis concentrates on the emulation of dynamic nonlinear circuits, which constitute a wide class of analog devices known to be particularly difficult to emulate by digital means in *real-time* (RT) through white-box methods. Both generic implementation techniques and specific circuits are studied in order to stimulate, on one hand, the research for focused and minimally demanding theoretical solutions to specific practical problems, and, on the other, the verification and evaluation of the effectiveness of methodological approaches in concrete scenarios.

The six publications discussed in this thesis can be grouped in three sets. The first includes Publication I, which digitizes a separable dynamic nonlinear circuit, that is a circuit that can be modeled by static nonlinear parts and dynamic linear parts showing negligible interdependency

[1]Bristol project website: `http://bristol.sourceforge.net`.

effects. Publications II, III, and IV form the second group. They utilize WDFs to model nonseparable dynamic nonlinear circuits with WDF-compatible topologies. Furthermore, Publication II extends the WDF theory to enable interconnections among subnetworks employing heterogeneous polarity and sign conventions. The last group is represented by Publications V and VI, which present, analyze, and provide digital implementations for a generalized version of the Moog ladder filter [74, 75]. Publication VI also introduces a generic delay-free loop implementation technique for dynamic nonlinear filters.

This thesis is organized as follows. Section 2 presents and performs a comparative analysis of the main white-box modeling and implementation techniques. Section 3 classifies dynamic nonlinear circuits and investigates the applicability of specific modeling and implementation methods. Section 4 summarizes the main scientific contributions of each publication. Section 5 concludes and points out possible future research directions.

2. Modeling and implementation techniques

Before delving into the technical aspects of the various VA modeling and implementation methods, it is worthwhile to examine the typical usage context of the original analog devices in order to obtain a clearer picture of the problem domain. This should also help to clarify the requirements that those techniques are meant to satisfy, and, conversely, which limitations can be tolerated.

In the most general terms, the devices of interest feature one or more signal inputs and one or more signal outputs. The input signals are generated by user-controlled gear, e.g., microphones, electronic musical instruments, synthesizers, samplers, record players, or other such sound processing equipment, while the output signals are reproduced, recorded, or fed into other similar devices. The user is often allowed to control functional parameters through different kinds of human-machine interfaces, e.g., panel-mount buttons and knobs, and external controllers. Figure 2.1 shows the input/output and control interface of a fictitious example device.

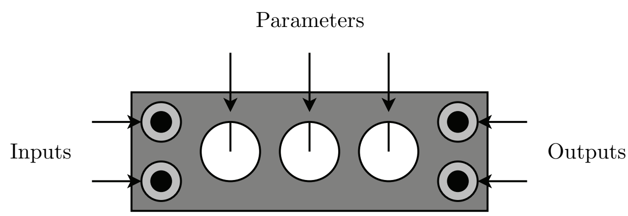

Figure 2.1. Input/output and control interface of a fictitious analog sound processing device.

Furthermore, with a few notable exceptions, the analog circuits being discussed are meant to exhibit minimal electrical coupling w.r.t. other interconnected devices, so that they can be regarded as isolated functional *modules* processing unidirectional signal streams. While it is still possible for the user to connect them so that external feedback loops are formed, such topologies are not considered to be relevant in this work, since they are not commonly encountered and may lead to unpredictable results or even to hardware damage. Figure 2.2 shows an example working setup topology.

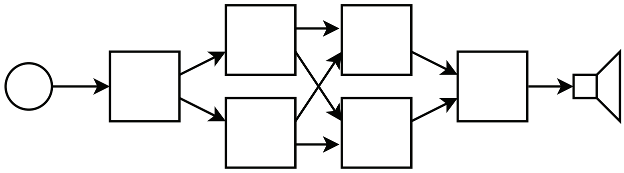

Figure 2.2. Example setup topology of interconnected analog sound processing devices. The circle represents a sound source, the boxes represent the devices of interest, and arrows the unidirectional signal streams.

The vast majority of analog circuits shows (quasi-)instantaneous input-output relationships, therefore making it necessary for digital emulation algorithms to guarantee that the execution time for any valid input amounts to less than the time duration of the same input and that the output relative to any valid input is produced within a predefined timeframe, that is they must operate in RT. This consideration restricts the class of suitable algorithms to those that do not exceed linear time complexity, which means they are bounded to a maximum finite number of operations per input sample, and that never perform potentially blocking operations. The undesirable artificial delay introduced by the digital emulation w.r.t. the original system is usually referred to as *latency*, and it can be conceptualized as the sum of two distinct components: a *buffering latency*, caused by the computational architecture of arguably all general-purpose *digital signal processing* (DSP) systems that this thesis targets, and an *algorithmic latency*, that is inherently due to the emulation algorithm itself.

Moreover, in analogy with the original devices, it is definitely desirable to let the user modify parameters affecting the generated sound while the emulator is running. Trade-offs need to be made in balancing the flexibility of the algorithms against the usage of available computing resources, and, in our case, it seems sensible to draw this line at excluding non-trivial structural changes in the data flow through parametric controls, which could be interpreted as corresponding to on-the-fly circuit modifications in the analog domain. Furthermore, parameter changes may be limited, for efficiency reasons, to happen asynchronously or at a control rate that is a fraction of the audio signal rate. In more general terms, low computational cost and memory usage are, in any case, especially attractive properties, since they also enable simultaneous execution and interconnection of multiple instances of virtual devices, which is customary in audio processing environments, digital audio workstations, and digital effect processors.

The development of emulation algorithms often proves to be a challenging endeavor, since large-signal models of dynamic nonlinear circuits usually correspond to systems of nonlinear *differential algebraic equations* (DAEs) for which no explicit analytical solution is known [76]. While general-purpose numerical methods may be employed, their computational complexity generally exceeds the constraints of RT emulation [77, 78]. Moreover, it is not uncommon for these equations to be *stiff*, that is they contain terms that can lead to rapid variations in the solution. For numerical solving methods to converge, in these cases, step sizes are required to be extremely small, which further increases the computational load. It comes as no surprise that different VA-specific approaches have been proposed which often pursue more sensible goals, in this specific application context, such as the maximization of perceptible, rather than absolute, accuracy and the preservation of stability conditions of the original systems in the digital domain.

This basic requirements analysis is already sufficient to obtain a framework, which Table 2.1 summarizes in a compact visual representation, against which it is possible to evaluate and compare the different VA techniques. Each column indicates criteria which are absolutely critical ("Must"), highly desirable in most application contexts ("Should"), or potentially desirable in a more restricted class of use cases ("May") for the generated algorithms to meet. The applicability of the various VA methods to specific problems, however, depends both on the peculiarities of their derivations and on the desired properties of the resulting algorithms. Therefore, the rest of this section contains an introduction to general-purpose circuit simulation algorithms, expanding on their unsuitability for VA emulation, brief descriptions of various VA methods; and a final discussion regarding such VA methods.

2.1 General-purpose circuit simulation algorithms

The history of general-purpose simulators of analog circuits spans back to at least the 1970s, when programs such as ASTAP (*Advanced Statistical Analysis Program*) [79], CANCER (*Computer Analysis of Nonlinear Circuits, Excluding Radiation*) [80, 81], and SPICE (*Simulation Program*

Must	Should	May
• Exhibit RT performance • Be bounded to a maximum finite number of operations per input sample • Never perform blocking operations	• Minimize algorithmic latency • Allow for low-rate/asynchronous parametric control • Minimize CPU and memory usage • Maximize perceptible accuracy • Preserve the stability of the original system	• Allow for audio-rate parametric control • Maximize absolute accuracy within band limits

Table 2.1. Properties that the algorithms generated through VA methods must, should, or may exhibit.

with Integrated Circuit Emphasis) [82, 83, 84] were developed. The second version of the last of these programs set a de facto standard in circuit simulation, to the point that, still today, its algorithms represent the cornerstone upon which the vast majority of simulators is based. This section discusses the nonlinear time-domain transient analysis algorithm implemented in SPICE2 [83], but similar considerations apply to all general-purpose circuit simulators.

The SPICE2 simulator internally describes circuits based on *modified nodal analysis* (MNA) [85, 76], which represents circuit equations as

$$\left(\begin{array}{c|c} \mathbf{Y} & \mathbf{B} \\ \hline \mathbf{C} & \mathbf{D} \end{array}\right) \left(\begin{array}{c} \mathbf{V}_{\mathrm{n}} \\ \hline \mathbf{I}_{\mathrm{b}} \end{array}\right) = \left(\begin{array}{c} \mathbf{J} \\ \hline \mathbf{E} \end{array}\right), \tag{2.1}$$

where $\mathbf{Y}$ is a reduced form of the nodal admittance matrix, $\mathbf{V}_{\mathrm{n}}$ is the vector of ungrounded node voltages, $\mathbf{J}$ is the current excitation vector, and $\mathbf{B}$, $\mathbf{C}$, $\mathbf{D}$, $\mathbf{I}_{\mathrm{b}}$, and $\mathbf{E}$ are used to accommodate voltage- and current-defined branches. This equation can be easily derived from a circuit diagram by first considering Kirchhoff's current-law equations, then substituting currents with node voltages according to branch-constitutive equations, and finally adding defining equations for elements with no admittance description.

If the simulated circuit is linear and static, determining node voltages at any time instant is easily accomplished by solving such a system of linear equations. In the general case, when dynamic nonlinear circuits are to be simulated, this arrangement is obviously insufficient. Therefore SPICE2 employs numerical root-finding and integration methods operating on linearized, discrete-time, and, generally, nonuniformly-sampled, snapshots of the MNA matrix equation (2.1).

2.1.1 Nonlinear DC analysis

The *direct current* (DC) analysis of linear dynamic circuits is relatively straightforward, since it consists of treating dynamic components—capacitors and inductors—as either voltage or current sources implementing their initial conditions and then solving the corresponding static MNA matrix equation.

In the dynamic nonlinear case, a numerical solution can be obtained iteratively by substituting each nonlinear component in the circuit with an equivalent linear subcircuit that approximates its behavior around the currently-chosen operating point. The algorithm works by making a first guess about the operating point around which a first solution is obtained, then using this solution to choose a new operating point, and repeating this process until the dissimilarity between two successive solutions lies within some predefined tolerance bounds. In particular, SPICE2 utilizes a modified version of the Newton-Raphson method to compute the following operating point from the previous solution.

2.1.2 Nonlinear transient analysis

The transient analysis algorithm computes the time-domain response of the circuit over a specified time interval by dividing it into discrete time points, then applying a numerical integration scheme to transform differential model equations into equivalent algebraic equations, and finally determining the instantaneous time-point solution using nonlinear DC analysis. The initial conditions can be either supplied by the user or automatically determined by the simulator employing DC operating-point analysis.

It is well known that implicit integration methods show better stability than explicit ones [86, 87], yet they require iterative methods for their evaluation. SPICE2 employs an implicit trapezoidal integration scheme with variable integration time step to accommodate stiff systems thus operating on nonuniformly-sampled signals. The algorithm that determines the distance between successive time points estimates the local truncation error and examines the convergence, or lack of thereof, of the solving algorithm at a particular time point, thus potentially decreasing this distance in case of nonconvergence. Hence, it is possible for the simulator to evaluate a time-point solution several times before producing the relative output.

Figure 2.3 visually summarizes the nonlinear transient analysis algorithm of SPICE2 with a flowchart representation.

2.1.3 Discussion

SPICE and other general-purpose circuit simulators are extremely valuable tools for circuit design and analysis. They are capable of simulating with considerable accuracy wide classes of circuits, including those that contain integrated circuits, analog and/or digital, and they often offer further analysis tools that are not described in this thesis. Furthermore, they are relatively modular and easy to use, in that they usually allow

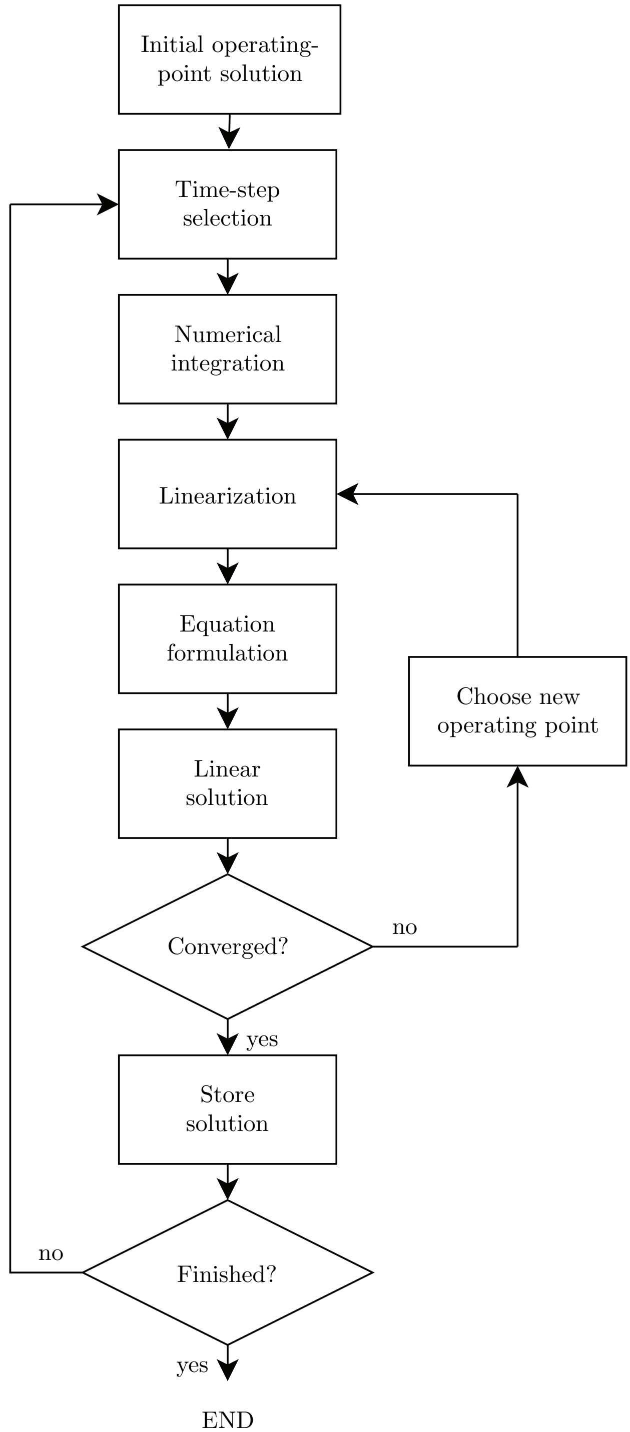

Figure 2.3. Flowchart representation of the nonliear transient analysis algorithm of SPICE2

the user to define a circuit by simply providing a *netlist* of interconnected components, which are either selected from a predefined library or defined themselves as netlists of their parts. Hence, the user may modify a circuit by simply editing its netlist. For these reasons, SPICE simulations have been used as references in Publications I, II, IV, and VI.

Nevertheless, the SPICE algorithm cannot be used for RT VA emulation, perhaps with the exception of small linear circuits for which other techniques are better suited. While its dependency on nonuniform sampling can be dealt with by introducing variable-rate interpolators at the inputs and decimators at the outputs, albeit introducing some amount of extra algorithmic latency, the computational cost of the iterative nonlinear DC analysis algorithm and, even more importantly, the time complexity of the time-step control algorithm make it unsuitable for RT operation.

2.2 Virtual analog methods

The various white-box VA methods that have been developed so far take different approaches to the problem of circuit simulation for the resulting algorithms to be suitable for RT execution at the expense of accuracy, modularity, stability, and/or generality. Some of these techniques tend to specialize on specific classes of circuits, for which they usually lead to algorithms with excellent computational properties, while encountering great difficulties in other cases. Other methods can be considered relatively generic, yet often incurring in performance penalties or other limitations that have to be taken into account.

This section explores both groups, compares individual techniques, and infers general properties about both the techniques themselves and the problem domain in order to suggest possible future research directions.

2.2.1 Port-Hamiltonian approach

This technique has been recently introduced by Falaize-Skrzek and Hélie [62] and is based on *port-Hamiltonian systems* (PHSs) theory [88, 89, 90], by which a circuit can be represented by the PHS equation

$$\left(\begin{array}{c} \frac{\mathrm{d}\mathbf{x}}{\mathrm{d}t} \\ \hline \mathbf{w} \\ \hline \mathbf{y} \end{array}\right) = \left(\begin{array}{c|c|c} \mathbf{J_x} & -\mathbf{K} & \mathbf{G_x} \\ \hline \mathbf{K}^T & \mathbf{J_w} & \mathbf{G_w} \\ \hline \mathbf{G_x}^T & \mathbf{G_w}^T & \mathbf{J_y} \end{array}\right) \left(\begin{array}{c} \nabla\mathcal{H}(\mathbf{x}) \\ \hline \mathbf{z}(\mathbf{w}) \\ \hline \mathbf{u} \end{array}\right). \tag{2.2}$$

The involved quantities can be chosen in a variety of different ways according to some constraints that guarantee power balance, that is, the passivity of the resulting system excluding external energy sources. The paper [62] builds a dictionary of standard components—resistors, capacitors, inductors, diodes, and transistors—in such a way that the two vectors in (2.2) contain voltage and current quantities and the matrix results in a combination of circuit topology relationships and constitutive laws of the circuit elements.

The temporal discretization of differential quantities is performed employing a finite-difference scheme that preserves stability, yet leading, in the general case, to implicit relationships. The proposed simulation algorithm involves a fixed number of iterations of the Newton-Raphson method to tackle this issue. This VA technique is then applied to digitize the CryBaby wah circuit with remarkable accuracy and RT performance [62].

However, the process by which (2.2) is derived from the circuit schematic is not univocally defined, which makes the translation of a given circuit into the PHS formalism a nontrivial process. It is also unclear whether and to what extent the application of the Newton-Raphson algorithm may affect the stability of the simulated system, even though the method derivation seems to give good guarantees in this sense. Furthermore, the computational cost of the resulting algorithms exceeds the one obtained through other VA methods and is more-than-linearly proportional to the number of components in the circuit. On the other hand, it is interesting to notice how such a technique that does not leverage on nonuniform sampling and does not require high sampling rates seems to be able to cope with stiff systems.

2.2.2 State-space methods

These methods are based on the SS formalism in representing dynamic nonlinear systems [63, 64, 19] as

$$\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}t} = \mathbf{Ax} + \mathbf{Bu} + \mathbf{Ci}, \tag{2.3}$$

$$\mathbf{i} = f(\mathbf{v}), \tag{2.4}$$

$$\mathbf{v} = \mathbf{Dx} + \mathbf{Eu} + \mathbf{Fi}, \tag{2.5}$$

$$\mathbf{y} = \mathbf{Lx} + \mathbf{Mu} + \mathbf{Ni}, \tag{2.6}$$

where $\mathbf{x}$ is the state vector, $\mathbf{u}$ is the input vector, $\mathbf{y}$ is the output vector, $f()$ is a *multiple-input multiple-output* (MIMO) nonlinear mapping, $\mathbf{v}$ is the input vector to such function, $\mathbf{i}$ is its output, t is the time variable, and the remaining symbols represent matrices that characterize the linear behavior of the system. In other words, a circuit is described as a strongly coupled system consisting of a dynamic linear part and a static nonlinear part.

Different discretization schemes can be applied to these equations, of which the most commonly used are the backward Euler method [63] and the trapezoidal rule [64, 19, 36], given their low computational cost and their applicability to stiff problems [91]. Such approaches, however, result in implicit equations that can be iteratively solved or otherwise approximated.

K-method

The so-called K-method to implement equations (2.3) to (2.5) is described in [63]. Applying the backward Euler method to discretize $\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}t}$ leads to

$$\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}t} \approx f_\mathrm{s}\left(\mathbf{x}[n] - \mathbf{x}[n-1]\right), \tag{2.7}$$

where n is the discrete-time variable and f_s is the sample rate. Substituting this quantity in (2.3) gives

$$\mathbf{x}[n] \approx \mathbf{H}\left(f_\mathrm{s}\mathbf{x}[n-1] + \mathbf{B}\mathbf{u}[n] + \mathbf{C}\mathbf{i}[n]\right), \tag{2.8}$$

where $\mathbf{H} = \left(f_\mathrm{s}\mathbf{I} - \mathbf{A}\right)^{-1}$. If such matrix inversion is possible, then (2.8) serves as an explicit state update formula. Combining (2.4), (2.5), and (2.8), it can be stated that

$$0 = f\left(\mathbf{p}[n] + \mathbf{K}\mathbf{i}[n]\right) - \mathbf{i}[n], \tag{2.9}$$

where $\mathbf{K} = \mathbf{DHC} + \mathbf{F}$ and $\mathbf{p}[n] = f_\mathrm{s}\mathbf{DHx}[n-1] + \left(\mathbf{DHB} + \mathbf{E}\right)\mathbf{u}[n]$. This static nonlinear mapping from $\mathbf{p}[n]$ to $\mathbf{i}[n]$ isolates the implicitly-defined part of the system which, if it is functional, can be either implemented by an iterative root-finding algorithm or by a precomputed lookup table. The paper [63] also shows how similar results can be obtained using other discretization schemes and evaluates the overall method by deriving a Chua's circuit emulator.

A modified version of the K-method is introduced in [64], which instead expresses the implicit relationships in terms of a static nonlinear mapping from $\mathbf{p}[n]$ to $\mathbf{v}[n]$, which poses different conditions on $f()$ for the derived nonlinear mapping to result functional, and which is claimed to achieve faster convergence in the case of electronic circuits.

DK-method

The K-method forms the basis upon which other more circuit-simulation-oriented techniques have been developed. One such technique, known as DK-method, is introduced in [64], which essentially proposes two improvements, namely automatic derivation of the SS equations (2.3) to (2.6) from circuit schematics and better numerical convergence through discretization of circuit elements before the formulation of the SS equations.

In particular, first an intermediate method is described, called NK-method, which only contemplates the former improvement by employing an ad-hoc form of MNA [85] that expresses a circuit as

$$\mathbf{G}\nu = \mathbf{M}_1\mathbf{x} + \mathbf{M}_2\mathbf{u} + \mathbf{M}_3\mathbf{i}, \tag{2.10}$$

where $\mathbf{G}$ essentially corresponds to the augmented node admittance matrix as found in equation (2.1) and ν is the vector of unknowns. Therefore K-method coefficients can be derived by inverting $\mathbf{G}$.

Such an arrangement leads to ill-conditioned problems in the case of some circuits containing reactive elements in series, hence the need for the latter improvement [64]. In this case, dynamic components are replaced by equivalent discrete-time companion circuits using the trapezoidal rule, thus obtaining the state update equation

$$\mathbf{x}[n] \approx \mathbf{G_e}\mathbf{v_e}[n] + \mathbf{S}\mathbf{x}[n-1], \tag{2.11}$$

where both $\mathbf{G_e}$ and $\mathbf{S}$ are linear combinations of component-specific values. With a similar approach to that applied in the derivation of the K-method, a nonlinear mapping is derived that isolates the implicitly-defined part of the system as

$$0 = \mathbf{p}[n] + \mathbf{F}f\left(\mathbf{v}[n]\right) - \mathbf{v}[n], \tag{2.12}$$

where $\mathbf{p}[n] = \mathbf{D}\mathbf{x}[n-1] + \mathbf{E}\mathbf{u}[n]$. As in the case of the K-method, this result is essentially independent of the type of discretization chosen. The paper then evaluates nonlinear solvers and eventually opts for precomputed lookup tables with interpolation to circumvent convergence problems. The DK-method is then applied to derive emulators of a diode clipper circuit [64], a common-emitter *bipolar junction transistor* (BJT) amplifier, and a common-cathode triode preamplifier [65].

Dempwolf's method

Another variant of the K-method was presented by Dempwolf *et al.* in [19]. In this case, the SS equations (2.3) to (2.6) are directly discretized by the trapezoidal rule, thus obtaining the state update equation

$$\mathbf{x}[n] \approx (2f_\mathrm{s}\mathbf{I} - \mathbf{A})^{-1} \\ \{(2f_\mathrm{s}\mathbf{I} + \mathbf{A})\,\mathbf{x}[n-1] + \mathbf{B}\,[\mathbf{u}[n] + \mathbf{u}[n-1]] + \mathbf{C}\,[\mathbf{i}[n] + \mathbf{i}[n-1]]\}\,, \tag{2.13}$$

and the linear part of the system can be expressed in terms of a new state variable

$$\mathbf{x_c}[n] \triangleq \frac{1}{2f_\mathrm{s}}\left[(2f_\mathrm{s}\mathbf{I} + \mathbf{A})\,\mathbf{x}[n] + \mathbf{B}\mathbf{u}[n] + \mathbf{C}\mathbf{i}[n]\right], \tag{2.14}$$

leading to

$$\mathbf{x_c}[n] \approx \bar{\mathbf{A}}\mathbf{x_c}[n-1] + \bar{\mathbf{B}}\mathbf{u}[n] + \bar{\mathbf{C}}\mathbf{i}[n], \tag{2.15}$$

$$\mathbf{v} = \bar{\mathbf{D}}\mathbf{x_c}[n] + \bar{\mathbf{E}}\mathbf{u}[n] + \bar{\mathbf{F}}\mathbf{i}[n], \tag{2.16}$$

$$\mathbf{y} = \bar{\mathbf{L}}\mathbf{x_c}[n] + \bar{\mathbf{M}}\mathbf{u}[n] + \bar{\mathbf{N}}\mathbf{i}[n], \tag{2.17}$$

where the various matrices can be computed as long as $2f_\mathrm{s}\mathbf{I} - \mathbf{A}$ is invertible.

This approach is less suitable for automatic formulation of SS equations from circuit schematics, but it generates smaller matrices than the DK-method, a property that the paper exploits to avoid matrix inversion in computing coefficients for a parametric emulator of the JCM900 preamplifier circuit, thus allowing for some RT-safe parametric control of the linear part of the system. This method has also been applied in [36] to discretize an analog guitar compressor.

Discussion

The SS formalism fully describes the behavior of any dynamic nonlinear system, and such generality is reflected by the various VA techniques based on it. This desirable property, however, comes with a price in terms of computational effort that the VA methods described here try to reduce in order to honour the RT restrictions.

The most relevant trade-offs involve RT parametrization on one side and computational resources on the other. Indeed, in the general case, matrix inversions and iterative root-finding algorithms would be needed to solve discrete-time SS systems, while in practice they are often replaced by precomputed lookup tables, thus usually trading lower computational effort and/or better numerical stability with increased memory usage. However, such an approach is, in general, only viable as long as the number of RT parameters is small and their values are confined to predetermined ranges.

2.2.3 Wave digital filters

The WDF theory was introduced by Fettweis in 1971 [66] and later vastly extended and adapted to various application contexts, to the point that an overview touching on most major subtopics would be overly lengthy. Therefore, this subsection only discusses the basic principles and properties related to RT audio circuit emulation. Readers interested in a comprehensive introduction to the topic are encouraged to refer to more exhaustive resources [67, 68, 69, 92].

WDFs can be thought of as digital equivalents of either analog circuit components or specific topological interconnections, and they operate on wave variables, which are quantities obtained through linear geometric transformations of directly observable Kirchoff variables. The most common variety is represented by voltage wave variables, which are obtained as

$$\begin{pmatrix} a \\ b \end{pmatrix} = \begin{pmatrix} 1 & R_0 \\ 1 & -R_0 \end{pmatrix} \begin{pmatrix} V \\ I \end{pmatrix}, \tag{2.18}$$

where a is the incoming wave variable or *incident wave*, b is the outgoing wave variable or *reflected wave*, V and I represent, respectively, voltage and current quantities of the Kirchoff variable pair, and R_0 is a resistance parameter that relates Kirchoff variables via Ohm's law.

Normally, each Kirchoff variable pair refers to an electrical port in a multiport network, that is to a pair of terminals where the ingoing current to one terminal is always identical to the outgoing current from the other. Such a pair can be always obtained from the wave variables by reversing (2.18). In this formulation R_0 is not required to correspond to any physically meaningful quantity, therefore it is used as an additional degree of freedom to simplify calculations.

The translation of *linear time-invariant* (LTI) components to the *wave-digital* (WD) domain can be easily accomplished by examining the so-called *reflectance* of a port, that is the transfer function from the incoming to the outgoing wave variable. In the Laplace domain

$$S(s) = \frac{\mathcal{L}\{b(t)\}}{\mathcal{L}\{a(t)\}} = \frac{Z(s) - R_0}{Z(s) + R_0}, \tag{2.19}$$

where $S(s)$ is the port reflectance and $Z(s)$ is the port impedance. At this point components can be discretized, most often by means of the bilinear transform, and R_0 can be chosen as a constant value that eliminates potential instantaneous dependencies between $b[n]$ and $a[n]$. Any WD port that exhibits this property, that is a lack of instantaneous reflections, is called *reflection-free*.

The interconnections among components can themselves be modeled in the WD domain as N-port scattering junctions, often referred to as *adaptors*. In this case, their constitutive relations can be simply transformed into the WD domain using (2.18), and then it is possible to solve for b_i, where i denotes the port index, often still obtaining one degree of freedom to choose R_0 for one of the WD ports so that it stays reflection-free. It follows that it is possible to build N-port adaptors with one reflection-free port by interconnecting three-port adaptors with one reflection-free port each in a tree-like structure called *binary connection tree* (BCT). This property holds true for, at least, series and parallel connection adaptors.

A typical WD network then results in a BCT where the leaf elements are digital filters representing single analog components, the branches are formed by interconnected adaptors, and the root element is connected to a reflection-free port thus being able to implement an instantaneous reflection without generating delay-free loops in the network. This last property is often exploited to implement nonlinear devices, since, in the general case, their discretization necessarily leads to instantaneous input-output dependencies. Furthermore, port resistance values are constants, thus offline-computable. These values propagate from the leaves to the root of the BCT.

Extensions

The basic form of the WDF theory presented so far possesses a number of highly desirable properties, in particular the preservation of passivity in common adaptors and in the digital equivalents of LTI analog components, excellent numerical properties [67], and a resulting computational cost that grows linearly with the number of leaf elements [93]. However, this formulation also exhibits serious limitations, mainly in its inability to properly accommodate time-varying impedances, implicit relationships in the root element, and the presence of multiple nonlinear elements, as well as in the difficulty in modeling non-multiport devices, such as vacuum tubes with grids, transistors, and integrated circuits. The same also holds true for certain types of interconnections, like the bridged-T [94, 95], Y, and Δ kinds, thus limiting the variety of supported circuit topologies. Here, some pragmatic solutions that have been proposed to cope with each of these problems are briefly discussed.

The most straightforward way to implement time-varying impedances simply consists of updating port resistance values, and potentially other "quasi-constants", at runtime whenever a parameter change occurs. Such an approach can be regarded as being analogous to changing the coefficients of a generic IIR filter during its operation, and thus no passivity, stability, or accuracy guarantees can be stated in the general case. A more sensible approach is described in [96], where a methodology is presented to derive WD structures that are consistent with the physics of time-varying impedances and transmission lines, but still without guaranteeing passivity or stability. A third method consists of employing power-wave, rather than voltage-wave, variables, which leads to different adaptor structures and element formulations that are, however, still interconnectable with voltage WD subnetworks through specific adaptors. In [97] it is shown that power wave adaptors inherently remain stable with time-varying port resistance values, but [67] claims that they lead to slightly higher computational costs and worse numerical properties. Finally, it is worth noticing that the time-varying generalization of allpass filters presented in [98] is based on power-normalized WDFs.

The simultaneous presence of multiple nonlinear circuit elements in WD networks and/or the occurrence of implicit relationships in the root element have also been addressed in different ways. The most simplistic approach is to strategically break delay-free loops by inserting fictitious unit delays (see Subsection 2.2.4), as in [99, 18, 100, 21], which may create instabilities and result in inaccuracies, but these problems can be mitigated by oversampling [99, 18, 100]. Another more sound possibility is represented by the implementation of all nonlinearities in a single multiport root element with multiple BCTs attached to it [101]. This method is successfully applied in Publication III, but the process is nontrivial since it inevitably has to rely on topological information to derive the multiport root element thus compromising modularity. Finally, recent studies analyze the use of fixed-point iteration schemes in this context [95, 102].

Similar difficulties affect the translation in the WD domain of non-multiport analog components, where possible solutions are represented by performing device-specific approximations, in which some feedback effects are neglected or predictively estimated, and/or by incorporating part of the circuit topology into leaf/root element logic, as discussed in [99, 18, 100, 5], as well as in Publications III and IV.

Finally, fully modular adaptors for certain types of topological patterns could not be derived without introducing delay-free loops [94, 103, 95]. Pragmatic approaches tend to trade modularity for easily computable structures, and fortunately automated methods exist that generate computable ad-hoc WD structures globally implementing the internal branches of a BCT for a wide class of circuit topologies [94]. On the other hand, a generic and fully modular approach was recently proposed that employs a quickly-converging fixed-point iteration scheme [95].

Polarity and current inverters

Publication II presents an extension of WDF theory to support different polarity and sign conventions in the same WD network. Essentially, while equation (2.18) does not impose restrictions on voltage and current directions, it is customary to always adopt the passive sign convention and, if polarity is defined, to choose voltages to point from the minus pole to the plus pole, as indicated in [67]. Such a rigid arrangement solves this ambiguity, but, for practical interconnection purposes, it forces the remodeling of N-port elements and subnetworks showing asymmetrical behavior up to 2^N times. Even worse, in case different sign conventions need to be employed, this upper bound grows up to 2^{2N}.

In order to avoid these issues, two simple two-port WD adaptors are introduced, namely a polarity and a current inverter, and they are shown to suffice in matching WD subnetworks operating with different polarity or sign conventions, to be *nonenergic*, thus never determining instabilities, and to never introduce instantaneous reflections, hence never causing computability problems. Figure 2.4 illustrates their signal-flow diagrams and WD representations. A somewhat direct relationship is found between the sign of port resistance values and sign conventions, in analogy with electrical circuit analysis, and the original definitions of WD passivity measures are extended to include the active sign convention case.

The approach is validated by adding a polarity inverter to the WDF guitar amplifier model presented in [99] between the plate circuit and the rest of the WD network. This modification corrects a polarity mismatch in the original model by which it operated as if the power supply had its positive terminal connected to ground, thus resulting in dramatic improvements in matching the output of SPICE simulations.

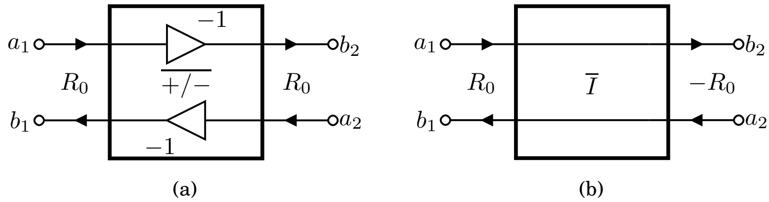

Figure 2.4. Signal-flow diagram and WD representation of (a) polarity and (b) current inverter adaptors.

2.2.4 Delay-free loop implementation techinques

Numerical integration and implementation of implicit equations represent two of the main issues in deriving RT-safe discretizations of dynamic nonlinear systems. While iterative approaches or other kinds of expensive and/or inflexible approximations seem to be needed in the general case, the same does not necessarily hold true in particular cases in which explicit approaches yield significant benefits. This subsection briefly describes such limited-scope techniques that emerged in VA research.

Classical explicit and semi-implicit numerical integration methods
While classical explicit numerical integration methods can be regarded as being quintessential to the discretization of LTI systems, their application in dynamic nonlinear systems can also sometimes lead to viable explicit discretizations that do not require excessive oversampling [8, 104], and the same is theoretically true for semi-implicit methods. Obviously, these methods are only concerned with numerical integration, thus other approaches are still needed to cope with implicit instantaneous relationships.

Fictitious delay units
The most obvious method to implement delay-free loops in a discrete-time filter consists of simply inserting one fictitious delay unit in each delay-free feedback branch [63, 105]. Despite its apparent naivety and its lack of stability guarantees, such an approach is undoubtedly attractive in that it has minimal impact on the filter structure and computational cost, and it has been therefore employed in several cases [8, 99, 21, 38]. Its accuracy and stability improve as the ratios between the band of the signals to be delayed and the sample rate diminish, and therefore it may be especially suitable when oversampling [99, 38]. It is also worth noticing that this method is also applicable when utilizing implicit discretizations of

continuous-time variables, since they are automatically transformed into explicit expressions. On the other hand, the frequency response of the filter is necessarily affected by such modifications, which often leads to undesirable and nonobvious parameter coupling effects [106, 107, 8, 104].

Härmä's method and derivatives

A method to implement recursive linear filters containing delay-free loops is presented in [70]. Given a filter

$$Y(z) = X(z) + P(z)Y(z), \tag{2.20}$$

where $P(z) = p_0 + \sum_i p_i z^{-i}$, it can be shown that

$$y[n] = \frac{x[n] + q[n]}{1 - p_0} \tag{2.21}$$

by applying the following procedure:

1. $q[n]$ is computed as the output of the feedback filter $P(z)$ fed by a null sample,
2. $y[n]$ is computed by (2.21),
3. $y[n]$ is used to update the state of $P(z)$.

This effectively corresponds to replacing the delay-free feedback branch with an equivalent, yet computable, feedforward term.

This technique was applied to frequency-warped recursive filters [70, 108] and was later extended to the MIMO case [109]. Nonlinear variants of the same technique are presented in [71, 72, 73], in which the nonlinear part is dealt with in a similar fashion to the K-method (see Section 2.2.2), thus still requiring iterative approaches and/or other approximations.

Nonlinear noniterative approach

Publication VI derives a novel technique for transforming an implicitly-defined discrete-time *single-input single-output* (SISO) dynamic nonlinear system into an explicit equivalent that retains the original linear response around a predetermined operating point. In order to minimize modifications to the original filter topology and to obtain a general framework for studying the proposed approach, the aforementioned goal is accomplished by applying a fictitious delay unit to the feedback branch and introducing linear compensation filters at the input and in the feedforward and feedback branches, as shown in Publication VI, Fig. 2, thus covering all possible cases in a mathematical, rather than structural, sense.

The paper gives a formal description of this problem and shows that there are infinitely many valid choices of linear compensation filters. It investigates some classes of solutions characterized by the existence of explicit and relatively simple coefficient formulae and the presence of the minimum number of coefficients, in general terms and in each specific class, such that the feedback branch is not necessarily eliminated. Furthermore, the paper also derives a composition method by which the same technique can be recursively applied to implicit filters themselves containing other implicit filters.

This approach is shown to be interpretable as a wide generalization of Härmä's method and it represents, as of today, the only such method that does not differentiate between stateless and stateful components. While the derivation is limited to SISO systems, this method was successfully applied to a generalized version of the Moog ladder filter, described in Publication V, from which several outputs are simultaneously extracted, thus obtaining the first documented noniterative white-box digital model of such a system that exhibits perfect parameter decoupling. Further research is however needed to obtain efficient implementations of generic MIMO systems.

While this technique certainly excels in generality, modularity, and flexibility, some of its fundamental properties, such as stability and global accuracy, are yet to be explored. In general, each solution class will behave differently, in this sense. Furthermore, its mathematical derivation does not prescribe specific operation scheduling or realization of linear compensation filters, which further complicates the investigation of these matters even within a single solution class. These considerations, however, also indicate that, for each implicitly-defined system, several explicit analogous systems can be derived that generally have different properties. In practice, it seems reasonable to speculate that the proposed technique is most likely viable when the system of interest is characterized by a mapping operator $f()$, as defined in Publication VI, Section III, whose linearization around all possible operating points gives a sub-unity feedback amplitude gain at all frequencies, which is certainly not the case of stiff systems.

2.3 Summary and conclusions

This section has first described at least some of the goals of VA modeling by examining the functional behavior of analog systems to be emulated, thus deriving a framework against which it is possible to evaluate and compare the different VA techniques, which is visually summarized by Table 2.1. Then it briefly analyzed the SPICE2 transient analysis algorithm [83] in order to show how general-purpose circuit simulators are unsuitable for VA emulation. Finally, short descriptions of the most prominent white-box VA emulation techniques follow, outlining their strengths and weaknesses.

This last analysis outlines that on one side are those methods that enjoy high generality, such as the port-Hamiltonian approach described in [62] and those based on SS formalism [63, 64, 19], which are often also characterized by relatively high computational resource requirements and/or lack of parametrization flexibility. On the other side are delay-free loop implementation methods, such as Härmä's method [70] and the approach described in Publication VI, which are limited to specific classes of circuits, whose discretization is minimally demanding and potentially highly parametric. WDFs [67] can be located between these two extremes, in that they trade generality for relatively good stability and parameterization possibilities, excellent numerical accuracy, and low computational effort. Nevertheless, the method introduced in Publication VI opens new possibilities in achieving good accuracy and stability without sacrificing computational resources, but further research is needed in this area.

All the presented techniques fully respect RT constraints, as long as enough computational throughput is available, and introduce negligible amounts of algorithmic latency, if any. The port-Hamiltonian approach and SS-based methods generally show better stability, especially when audio-rate parametrization is desirable and possible, as well as higher accuracy. WDFs also allow for high fidelity VA emulation of supported circuit topologies, but special care needs to be taken in the parametric case. As of today, noniterative delay-free loop implementation methods tend to be most attractive when discretizing weakly-nonlinear and/or nonstiff circuits.

Moreover, these techniques are not mutually exclusive, meaning that it is certainly possible to use them in conjunction to digitize an analog circuit. Indeed, some attempts to hybridize different approaches have already been documented [110, 111], however this possibility still awaits more systematic exploration.

3. Application to dynamic nonlinear circuits

As already anticipated in Section 1, this thesis is also concerned with the emulation of specific dynamic nonlinear circuits in order to evaluate the applicability and suitability of various VA methods in concrete scenarios. It particularly concentrates on those systems that do not require highly-generic VA techniques, both for efficiency of the resulting algorithms, as discussed in Section 2, and to promote research towards minimally demanding VA methods. Moreover, non-generic VA approaches tend to generate filters that retain, to some extent, topological information of the original circuit in the digital domain, thus often being *modular*, in the sense that specific parts of the generated digital filter univocally correspond to specific parts of the analog circuit, and/or parts of the digital filter topology correspond to parts of the continuous-time model equations. This property does not only allow for better understanding of the internal workings of the original device through *divide-et-impera* approaches, but also greatly simplifies modification, reusability, and composition of the obtained results, leaving inessential implementation and optimization details to the programmer and to the compiler.

This section examines the circuits of interest by coarsely classifying them into three classes:

- *separable circuits*, characterized by negligible interdependencies between their dynamic linear and static nonlinear parts;

- *nonseparable, WDF-compatible circuits*, which allow precise and direct modeling of linear-nonlinear interdependencies through WDFs; and

- *nonseparable, non-WDF-compatible non-stiff circuits*, whose modeling and implementation does not require highly generic VA methods, but whose linear-nonlinear interdependencies are not easily translatable into the WD domain.

3.1 Separable circuits

In general, physical systems are characterized by mutual instantaneous interdependencies among their parts. However, some dynamic nonlinear circuits may be reasonably modeled as a set of separate subcircuits characterized by a unidirectional control flow, that is each subcircuit may control others as long as no feedback control loops are formed. This is often the case when operational-amplifier-based buffers or electrically isolating components, such as those depicted in Figure 3.1, are employed.

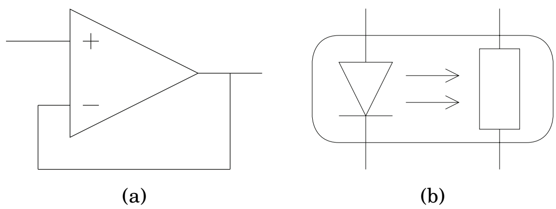

Figure 3.1. Examples of isolating circuit parts: (a) shows an operational-amplifier-based voltage follower and (b) represents a resistive opto-isolator device.

When the set of such subcircuits contains only dynamic linear and static nonlinear parts, the digitization of the whole circuit usually is particularly straightforward, since the former parts may be implemented through standard linear filtering techniques and the latter may remain unaltered in the digital domain. In some cases, the major practical difficulty is represented by the presence of implicit nonlinear equations in the large-signal model of one or more static nonlinear parts, which can be tackled by iterative methods, precomputed lookup tables, or other approximations [112].

The stability of the resulting global filter will correspond to the intersection of the stability regions of its linear parts, which will necessarily cover the global stability region of the original device in the time-invariant case when employing appropriate linear discretization techniques, e.g., the bilinear transform. In the time-varying case, appropriate linear digital filter topologies may still preserve the stability of the original device [113, 114, 115].

In some cases it is desirable to also retain some topological information of one or more linear parts into the digital domain, e.g., for later inserting weak nonlinearities or to apply simple localized modifications. The Buchla lowpass gate described hereafter represents a clear example of such a separable circuit.

3.1.1 Buchla lowpass gate

Publication I presents a digital model of the Buchla lowpass gate, a special lowpass filter circuit developed by Don Buchla in 1970 for the Buchla 200 series Electric Music Box modular synthesizer. It consists of two separable subcircuits:

- a dynamic linear audio-path subcircuit which can operate in three modes according to a three-pole switch setting that modifies its inner topology, ranging from a resonant lowpass configuration to a voltage-controlled amplifier mode of operation, and

- a dynamic nonlinear control-path subcircuit, which is shown to be itself separable into two more sequentially connected parts:

  1. a dynamic linear part that applies buffering and low-shelving to a control input signal and

  2. a static nonlinear part that controls the cut-off frequency of the audio path subcircuit through a resistive opto-isolator.

The digitization of these last two parts is conceptually straightforward, as it results in a series of a low-shelving filter and a static nonlinearity. This last component is, however, nontrivial to model in practice due to the simultaneous presence of a Zener diode and the *light-emitting diode* (LED) part of the opto-isolator. The paper develops an explicit approximation that instantaneously maps the output of the shelving filter to the current flowing through the LED to overcome this problem.

A continuous-time model of the audio-path subcircuit is derived that also takes into account the various switch settings in terms of values of specific circuit components, and then the resulting differential equations are transformed into a digital filter that retains their structure by replacing each part of the said equations with digital counterparts discretized through the bilinear transform and implemented in *transposed-direct-form-II* (TDF-II). This leads to a digital filter with delay-free loops that are implemented explicitly with a technique that is substantially equivalent to Härmä's method (see Section 2.2.4). It is also shown how this peculiar discretization allows adding nonlinear limiting effects to the resonance feedback path, thus mimicking analogous modifications that are often found in derivative versions of the circuit.

Finally, a simple, heuristic, unidirectional dynamic nonlinear model of the resistive opto-isolator is described, which maps the current through the LED in the control-path subcircuit to resistance values of the corresponding *light-dependent resistors* (LDRs) in the audio-path subcircuit.

3.2 Nonseparable WDF-compatible circuits

Despite their inability to generate explicit implementations of arbitrary topologies, WDFs were found suitable for modeling and digitizing a relatively wide class of nonseparable dynamic nonlinear circuits [116, 101, 18, 5]. As discussed in Section 2.2.3, one of the main limitations concerns the presence of multiple nonlinear elements when they are not easily groupable into a single, nonlinear root WD element. Therefore, a sensible criterion for considering whether the digitization of a given circuit could be pursued through a WD approach might correspond to establishing whether it is possible to partition the circuit into separate subcircuits characterized by unidirectional control flow and WDF-compatible topologies, as in the example depicted in Figure 3.2.

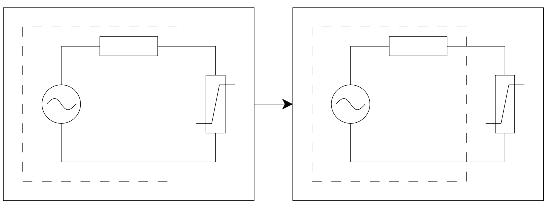

Figure 3.2. Two nonseparable WDF-compatible circuits, where the one on the left side controls that on the right side. The dashed boxes contain the Thévenin equivalents of the linear parts of each circuit.

The literature, however, reports several cases in which WDFs were successfully applied even if this partitioning scheme was not fully respected [99, 100, 5, 21]. In most of such cases, the original circuit is further partitioned by approximating some instantaneous interdependencies with the addition of fictitious delay units, according to the constraints discussed in

Section 2.2.4. The reader is encouraged to refer to [5] for a more systematic discussion on non-standard WD structures.

3.2.1 Common-cathode triode stage

The common-cathode triode stage, depicted in Publication II, Fig. 4, and Publication III, Fig. 2, represents one of the classical preamplifier subcircuits commonly found in tube audio amplifiers. While triodes are not multiport elements, thus being difficult to model in the WD domain, the first WDF-based implementation of such a circuit was proposed by Karjalainen and Pakarinen [99] which disregarded the so-called grid-current effect by assuming that no current flowed through the grid terminal. The triode element could then be implemented as a voltage-controlled nonlinear resistor. However, the controlling voltage still instantaneously depended on both the grid and the cathode voltages, which created a delay-free loop that was made explicit through a fictitious delay unit by considering that the cathode voltage changes slowly compared to the grid voltage. Publication II improves this design by also applying a WD polarity inverter element to correctly match polarity conventions, obtaining substantial improvements in accuracy, while [18] employs this same approach to model the whole output chain of a tube amplifier.

Later, a WD approach that also contemplated the grid-current effect was presented in [100], where the nonlinearity on the grid terminal is modeled by a diode element, whose voltage controls the nonlinear resistor implementing the plate-to-cathode relationship. In order to make this structure computable, a fictitious delay unit is inserted between the diode and the nonlinear resistor elements. In this case, the resulting BCT may be interpreted as consisting of a multiport root nonlinear element that roughly corresponds to the triode and of separate subbranches implementing the subcircuits connected to each terminal of the triode, as shown in Publication III, Fig. 3(b). In particular, such a composite three-port root element also contains some adaptors that limit its applicability to the restricted class of circuit topologies depicted in Publication III, Fig. 1.

Based on these considerations, Publication III essentially proposes a global approach to model the triode as a three-port root element that does not require fictitious delay units and employs a more realistic static triode model [117] than previous attempts [118]. Two algorithms are derived, one that includes the grid-current effect and another that does not, both sharing the same WD structure. Furthermore, their parametrization is independent of the peculiar interpolative formulation of the chosen triode model, as long as a few restrictions are enforced. The resulting digitizations of the original circuit are found to be less computationally demanding than the previous emulators, while swept-sine [119] and output aliasing [120] analyses reveal, respectively, that they produce richer and more regular harmonic responses and comparable or less aliasing in the output signals.

It should be noted that a similar circuit has been efficiently modeled with the DK-method [65], yet the proposed solution differs in that it is highly parametric, since no precomputed lookup table is required to achieve RT performance, and also more modular, but maybe not as computationally efficient. However, it is still possible to trade some or all of its parametricity and/or memory usage for lower CPU load, e.g., by choosing parameter values beforehand, solving the implicit nonlinear relationships offline, and employing lookup tables. In this case, the resulting performance should be comparable or even better than the corresponding DK-method-based solution, given that WDFs have lower complexity than SS-based methods [93].

3.2.2 Operational-amplifier-based guitar distortion circuits

Publication IV presents WD models of a noninverting and an inverting guitar distortion circuit, respectively illustrated in Fig. 4(a) and Fig. 4(b). The difficulty, in these cases, is represented by the presence of operational amplifiers, which are not multiport elements, and strongly saturating nonlinearities implemented by antiparallel diode pairs.

Firstly, a WD operational amplifier model is derived from a simplified static linear circuital model of such element, which is converted to the WD domain by presupposing a certain topological arrangement, in an analogous fashion to the triode case discussed in Publication III. This results in three separable subcircuits with a unidirectional control flow, as shown in Publication III, Fig. 1(d), which correspond to original subcircuits connected to the non-inverted input, the inverted input, and the feedback path between the inverted input and the output.

In both cases the nonlinearities are part of the feedback subcircuit, and thus it is naturally possible to implement them as one-port root elements. The exact explicit analytical expression implementing the WD model of a single diode is derived, leading to a relationship involving the Lambert $W()$ function [121, 122, 123]. An approximated WD antiparallel diode pair element is then derived by considering that, at any time instant, the forward current flowing through one of the diodes is substantially greater than the reverse current flowing through the other, which is therefore completely neglected.

The computational load of the resulting emulators is dominated by the Lambert $W()$ function evaluation, which can be conveniently performed by employing lookup tables without compromising parametrizability. Swept-sine analysis [119] revealed an excellent match between the output signals generated by the proposed emulators and analogous SPICE [82, 83, 84] simulation results.

As for the previous circuit, a previous model for a similar device has been proposed using the DK-method [64]. Again, the exact same considerations regarding modularity, paramterization, and computational load apply.

3.3 Nonseparable non-WDF-compatible non-stiff circuits

Even in the case of dynamic nonlinear circuits that are not separable and not easily representable as WDFs, an explicit discretization through delay-free loop implementation techniques, as presented in Section 2.2.4, may still be viable, particularly when model equations are not stiff. The Moog ladder filter [74, 75], a resonant lowpass filter with a peculiar ladder topology invented by Robert Moog in 1965 for his modular synthesizers, represents one concrete example of such a circuit. Its discretization has been addressed by several authors, but resulting in digital implementations that are computationally demanding [53], limited to the linear case [106, 107, 124], or cannot correctly reproduce its linear response [106, 107, 8, 104]. In particular, the approaches that were taken in all of the cited papers already employ a mixture of delay-free loop implementation techniques. This section summarizes the results obtained in Publications V and VI, which culminate in the definition of the first documented lightweight digital emulator of a generalized version of such a device that preserves its linear response without compromising its nonlinear behavior.

3.3.1 Generalized Moog ladder filter

Large-signal models of the original filter [8, 53, 104] show that it is functionally equivalent to a series of four nonlinear and implicitly-defined one-pole lowpass filters, usually referred to as *ladder stages*, and a global delay-free feedback branch that feeds part of the filter output, which corresponds to the output of the last stage, into the first stage. An equivalent circuital representation of such models is shown in Figure 3.3. Publication V studies a version of the filter circuit generalized to any number of ladder stages, depicted in Fig. 2 of the publication, and proposes a similar large-signal continuous-time model with a variable number of stages. A linear response analysis is performed to extend previous results [125, 126] to the generalized case and to identify exact analytical relationships between filter parameters, namely control current and feedback gain, and properties of the transfer function, such as cut-off frequency, Q (*Quality*) factor, and DC gain.

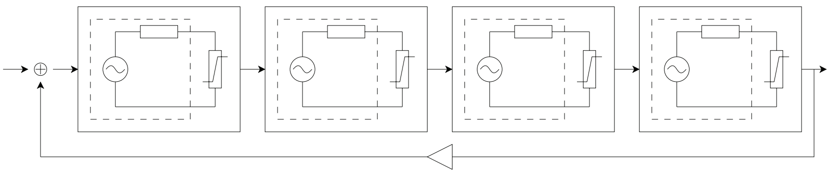

Figure 3.3. Circuital equivalent of the continuous-time large-signal model of the original Moog ladder filter.

The peculiar choice of the number of ladder stages in the original device is essential to obtain certain desirable parametric control properties, as in all other cases the cut-off frequency parameter becomes significantly coupled with global feedback gain setting. In order to achieve some form of consistency among different filter orders, a few alternative parametrization strategies for digital implementations are examined, based on an analysis of the deviation from the behavior when the feedback gain is null. In particular, three relative error measures are defined, namely a cut-off frequency error, when the filter is parametrized in terms of control current, or any other linearly-proportional quantity; a cut-off slope gain error, which quantifies the deviation of the position, i.e., gain, of the stop-band slope when the filter is controlled in terms of the resulting cut-off frequency; and a dc gain error, which is entirely due to the feedback gain. A few pragmatic considerations allow to suggest parametrizing the generalized filter in terms of resulting cut-off frequency and feedback gain without any extra gain compensation.

In the end, the paper presents a simple linear digital implementation of the generalized device, based on a series of biquad sections and a final first-order section, in case the filter order is odd. The filter is discretized using the bilinear transform with pre-warping around the global cut-off frequency. This results in the generated frequency responses to match theoretical results, except for frequency-warping effects at high frequencies, which could be however otherwise mitigated [127].

Publication VI describes another model of the same generalized circuit with any number of ladder stages that exhibits excellent linear response, stability, and parametrization properties, and that also emulates the nonlinear behavior of the device. The approach, in this case, consists of applying a delay-free loop implementation technique, introduced in the same paper and briefly discussed before in Section 2.2.4, which provides explicit structures for the implicitly-defined parts in such a way that their linear response is preserved around their natural operating point. The fourth-order variant of this implementation is compared with two previous emulators [8, 104], and it is found to be vastly superior in terms of parametrization and linear response, comparable in terms of nonlinear behavior, and only slightly heavier in terms of computational load. Furthermore, this model also allows for precise extraction of different frequency-response modes by mixing the outputs of individual ladder stages as described in [128].

3.4 Summary and conclusions

This section elaborated on the desirability of employing non-generic VA techniques to maximize efficiency and modularity, and then it coarsely classified circuits suitable to be modeled and implemented through such techniques in three classes and analyzed them with concrete examples from the publications.

The first class includes circuits that are separable into dynamic linear and static nonlinear parts with unidirectional control flow, which can be conveniently implemented through classical linear filtering techniques that guarantee good stability properties and static nonlinear blocks, as in the case of the digital model of the Buchla lowpass gate presented in Publication I.

The second class corresponds to those nonseparable circuits that can be modeled through WDFs, including the cases in which it is possible to partition them into multiple WDF-compatible circuits with either unidirectional signal flow or with mutual interdependencies that may be approximated through delay-free loop implementation techniques. The common-cathode triode stage presented in Publications II and III, with particular emphasis on the digital model proposed in the latter paper, and the emulators for the two operational-amplifier-based guitar distortion circuits described in Publication IV were reported as examples.

The third and last class consists of those circuits that are nonseparable, non-WDF-compatible, and non-stiff, which may still be implemented through delay-free loop implementation techniques. The digital models of a generalized version of the Moog ladder filter in Publications V and VI shows that such a circuit belongs to this group.

While it is difficult and inappropriate to extrapolate general properties from specific cases, it appears remarkable that classical DSP techniques and VA methods that do not enjoy high genericity can be pragmatically employed to digitize such a wide class of dynamic nonlinear circuits. It is also worth noticing that generic methodological improvements and innovations, such as the WDF polarity and sign inverters introduced in Publication II and the delay-free loop implementation technique presented in Publication VI, were essentially developed to solve modeling and implementation issues in specific cases, a fact that underlines the importance of problem-oriented research.

4. Summary of main results

Publication I. A Digital Model of the Buchla Lowpass-Gate

The control-path circuit of the device is partitioned into a dynamic linear part that filters the control input cascaded with a static nonlinear part that controls the LED part of a resistive opto-isolator, whose LDRs reside in the audio-path subcircuit and control its cut-off frequency. Firstly, the validity of such a separation is shown, resulting in the dynamic linear part being modeled as a classical low-shelving linear filter. The static nonlinear part is implemented by an explicit mapping, whose derivation involves the Lambert $W()$ function [121, 122, 123], datasheet information for the resistive opto-isolator, and results obtained through SPICE [82, 83, 84] simulations.

Publication II. Wave-Digital Polarity and Current Inverters and Their Application to Virtual Analog Audio Processing

A simple consideration on polarity and sign conventions in WDFs leads to the conclusion that N-port elements that exhibit asymmetrical behavior may need to be modeled up to 2^{2N} times to be compatible with normal WD structures. Therefore, an extension to the WDF theory is proposed in order to support any polarity and sign convention, and specific polarity and current inverters are defined to match WD subnetworks adopting different conventions. Extended definitions of instantaneous and steady-state pseudopower are given, and the introduced inverters are shown to be pseudopassive, pseudolossless, and nonenergic according to any convention, as well as never introducing delay-free loops. Negative port resistance values, which are normally excluded from classical WDF theory, are shown to be related to the active sign convention. These results are applied, as a case study, to the WD common-cathode triode stage emulator presented in [99], resulting in remarkable output-accuracy improvements.

Publication III. New Family of Wave-Digital Triode Models

A WD model of vacuum-tube triodes implemented as a three-port nonlinear root element is presented that does not require fictitious delay units. It is based on the triode model presented in [117], which more faithfully reproduces the saturating behavior of the original devices than the model [118] employed in previous WD implementations [99, 100]. The resulting algorithms, one that includes grid-current effect and the other that does not, impose a few restrictions in the parametrization scheme, thus allowing further experimentation in this sense. The derived model is applied to the common-cathode stage preamplifier circuit and compared with previous models [99, 100], leading to less computationally demanding emulators, richer and more regular harmonic responses, and comparable or less aliasing noise in the output signals.

Publication IV. Emulation of Operational Amplifiers and Diodes in Audio Distortion Circuits

The paper presents WD models of operational amplifiers and antiparallel diode pairs, which allow for WD modeling and implementation of two guitar distortion circuits. In particular, an exact, explicit, analytical WD model of a single diode is derived that involves one evaluation of the Lambert $W()$ function [121, 122, 123], while the WD model of an antiparallel diode pair is developed by considering that the forward current through one of the diodes makes the corresponding reverse current through the other diode negligible, thus resulting in one Lambert $W()$ function evaluation per time instant, which can be conveniently implemented through lookup tables without compromising parametrizability. The application of such models to the discretization of the aforementioned guitar distortion circuits results in efficient emulators whose output signals match corresponding SPICE [82, 83, 84] simulations with notable accuracy.

Publication V. Generalized Moog Ladder Filter: Part I – Linear Analysis and Parameterization

A version of the Moog ladder filter [74, 75] generalized to any number of ladder stages is presented and a continuous-time large-signal model is proposed. A linear response analysis extends previous results [125, 126] to the generalized case, and exact analytical expressions are derived that relate filter parameters to transfer function properties. Further study of parametric control issues allow establishing a parametrization strategy that is consistent for any number of ladder stages. An example linear digital model is then proposed that faithfully reproduces the linear response of the generalized circuit.

Publication VI. Generalized Moog Ladder Filter: Part II – Explicit Nonlinear Model through a Novel Delay-Free Loop Implementation Method

In order to define an accurate nonlinear emulator of the generalized Moog ladder filter introduced in Publication V, a novel and generic delay-free loop implementation technique is developed that preserves the linear response of the original filter around its natural operating point. This technique minimally affects the original implicitly-defined topologies through potentially infinite families of linear compensation filters characterized by simple analytical expressions for coefficient values. Minimally demanding compensation filters are identified, and a recursive composition method is proposed. This approach can be interpreted as a wide generalization of Härmä's method [70] that noniteratively supports nonlinear systems and does not differentiate between stateless and stateful components. It is then applied to the circuit of interest, obtaining the first documented noniterative white-box digital model of such a system that exhibits perfect parameter decoupling, precise extraction of different frequency modes [128], and excellent stability properties, and whose fourth-order variant compares favorably in terms of linear behavior to previous models [8, 104], while showing similar accuracy in nonlinear behavior, and only requiring a slight increase in computational requirements.

5. Conclusions and directions of future research

This work discussed the most prominent VA methods available to date, with a special emphasis on those that generate emulators characterized by high levels of parametrization and low computational requirements, as opposed to others that trade higher generality for lower algorithmic efficiency. This choice does not imply superiority of the former to the latter or viceversa, but it merely reflects the intention to stimulate investigations towards efficient, modular, and conceptually simple techniques, whether generic or specialized. In any case, research is likely to continue in both directions, at least in the near future, and potentially leading to convergent evolutions, also considering that, as outlined in Section 2.3, it is certainly possible to simultaneously employ more than one VA method in a complementary fashion. Furthermore, the importance of problem-oriented research was stressed in Section 3.4, since it may lead to methodological innovations or improvements of already existing techniques, as in the cases of Publications II and VI.

This last publication contains the most important contribution that this thesis presents, namely a novel, conceptually straightforward, computationally lightweight, and modular technique to implement nonlinear delay-free loops, which represent one of the major difficulties in VA modeling of dynamic nonlinear circuits, that preserves the linear response of the system around an arbitrary predetermined operating point. This technique is, however, limited to the SISO case and its applicability to a given circuit model has not yet been studied. The former limitation is somewhat relative, given that a recursive composition method is also documented, but a proper MIMO extension would most likely lead to more efficient structures. On the other hand, more research is definitely needed to determine its accuracy and stability properties.

Other than that, different important subtopics were touched on in this work. In particular, Publications III and IV indicate a potentially rewarding direction in WDF research, in that they define multiport WD models of non-multiport analog elements leveraging on *a priori* topological assumptions. While such an approach is not entirely new to WDF theory [101, 5], these two papers represent some of the first practical applications of this principle, which can be probably successfully employed for modeling other electronic components and circuit topologies. Moreover, Publications I and IV emphasized the identification and exploitation of subcircuit separability as a mean to simplify circuit modeling and lower computational requirements, as discussed throughout Section 3. This is, once again, all but a novel idea, and indeed its proven effectiveness definitely needs to be taken into account in future VA research.

Further theoretical and pragmatical aspects were also found to hold particular interest depending on the application context, such as analytical and approximate solutions of transcendental equations in Publications I and IV, parametric control analysis in Publication V, and reusability of known digital structures in Publications II and IV. Finally, all of the emulators presented in this work are reasonably accurate and certainly suitable for RT execution, yet it would be hard to believe that they could not be further improved.

In more general terms, important contributions to the field might come from various, and apparently uncorrelated or diverging, research directions. On one hand, there is no doubt that the development of novel VA modeling techniques and the improvement of already existing ones are still likely to bring noticeable benefits in the near future. However, parallel investigations into other topics might prove equally important. For example, the development of aliasing suppression methods for nonlinear filters should help relaxing oversampling requirements, insight into the physical and cognitive aspects of hearing might lead towards more meaningful parametrization possibilities, and also advances in the mathematical treatment of transcendental equations could improve or simplify the digitization of analog circuits. Furthermore, the importance of applied research should not be undervalued, since, as of today, there exist only few specialized tools for the VA researcher, and especially w.r.t. development of white-box models.

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