



# RYO Discrete TRL Boolean Logics

## NAND/AND

- 1 Gate one input 1 (normalised 1>2)
- 2 Gate one input 2 (normalised 2>3)
- 3 Gate one input 3
- 4 Gate one NAND Output
- 5 Gate one AND Output (normalised to Gate two input 1)
- 6 Gate two input 1 (inputs normalised 1>2)
- 7 Gate two input 2
- 8 Gate two NAND output
- 9 Gate two AND output

[Try dif input amplitudes, waveforms and frequency rates including audio into inputs!] Width: 4 hp

Name	AND	NAND																														
Alg. Expr.	$AB$	$\overline{AB}$																														
Symbol																																
Truth Table	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	B	A	X	0	0	0	0	1	0	1	0	0	1	1	1	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	B	A	X	0	0	1	0	1	1	1	0	1	1	1	0
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