An Analog Circuit Technique for Finding the Median

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Abstract

In this work, we present a novel analog technique to find the median of an odd number of inputs. A three-input median circuit, implemented in a 2μm CMOS process, demonstrates the efficaciousness of the technique.

1. Introduction

Median filtering is one of the key nonlinear operations used in digital signal and image processing [1-3]. In time or space, it consists of taking an odd number of neighboring points, and outputting the value which is in the middle when the points are sorted by value - i.e. the median of the points.

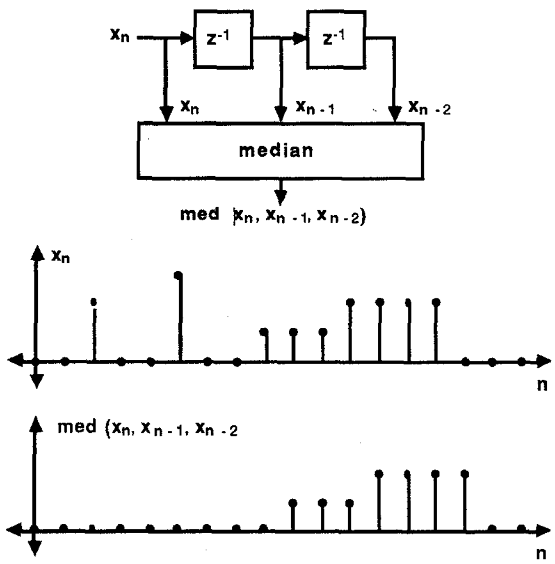

Figure 1. A temporal 3-point median filter, an example input, and the filter's response.

While simple in concept, median filters are nonlinear and have some extremely useful properties. Figure 1 shows a 3-point, temporal median filter, an example input signal and the filter's response. Note that the filter completely rejects isolated impulses while perfectly preserving step changes. This effect is impossible to achieve with a linear filter.

Figure 2, further demonstrates the usefulness of median filtering. In this case, a 3x3 spatial median filter is used to remove impulsive noise. It is clear that the median filter performs much better than the linear filter for this example.

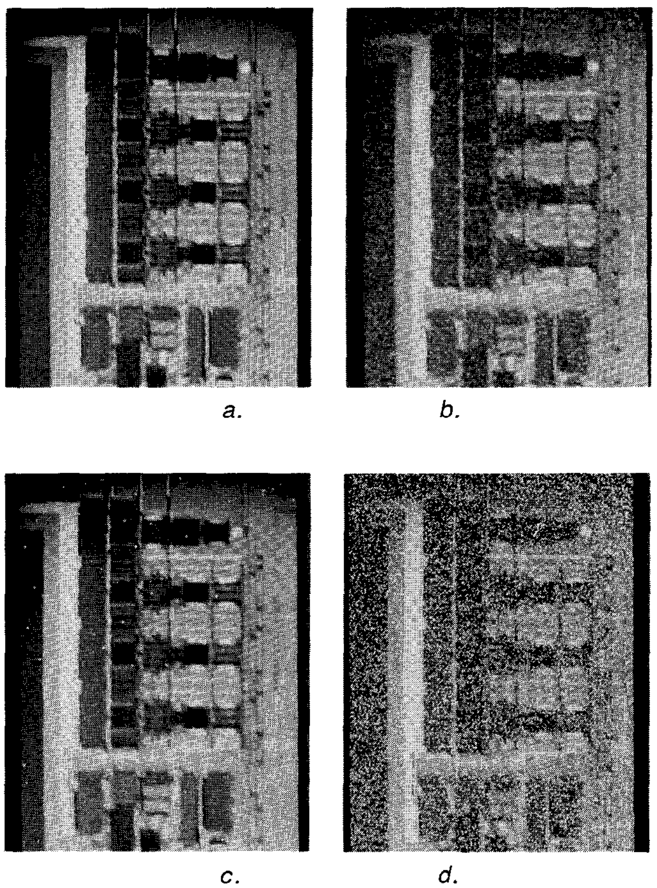

Figure 2. Median filter chip. (a) Original image; (b) Image corrupted by mixed impulses; (c) Output of a 3x3 median filter; (d) Output of a 3x3 moving average filter.

Generally, median filters are implemented in digital form and are considered computationally expensive. Thus their use has been limited to low data rate systems. In this work we will demonstrate a technique which uses simple analog circuits to find the median. These circuits can be made fast and small allowing for enormous data rates in parallel systems. Unlike previous implementations [1], the median technique we propose is a true continuous time system,

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suitable for such applications as pixel plane processing, and high speed communications systems.

2. Analog Computation of the Median of N Signals

Since median filters have existed for quite some time in digital form, a number of algorithms have been used in their implementation. However, these algorithms are generally based upon maintenance of a sorted list of the data points into which new points are inserted and old points deleted. Unfortunately, analog implementations are not amenable to these types of algorithms. Instead, we propose an algorithm which uses feedback to solve an equation, whose solution is the median. This type of algorithm was used by Lee and Kassam [2] in their description of *M*- filters. It will be shown that this technique yields efficient implementations in MOS and bipolar technologies.

We begin by assuming that there are N inputs, where N is an odd number, and we define a function $f(x)$ as:

$$f(x) = \begin{cases} +1 & \text{for } x > \varepsilon \\ \dfrac{x}{\varepsilon} & \text{for } |x| \le \varepsilon \\ -1 & \text{for } x < -\varepsilon \end{cases} \qquad (1)$$

which is shown in figure 3.

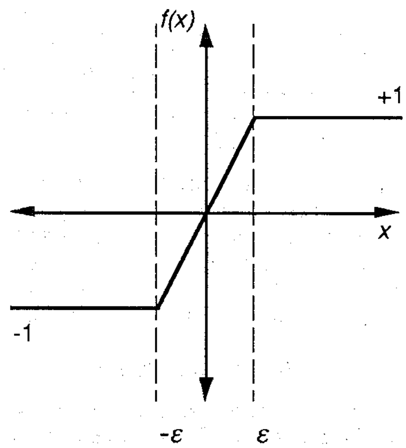

Figure 3. The limiting function, f(x), which is used in the median filter.

The median, M, is such that it solves the equation:

$$0 = \lim_{\varepsilon \to 0} \sum_{k=1}^{N} f(V_k - M) \qquad (2)$$

The circuits that we shall describe approximate this equation, using feedback to solve for M.

3. Circuits for Computing the Median

A block diagram of a circuit to simulate equation 2 is shown in figure 4. There is one limiting gm block for each input. These approximate the function given in equation 1. Since the outputs are differential currents, they are summed by wiring them together. Finally, there is an output amplifier which converts the summed differential current into a voltage which is output and fedback as an estimate of the median. While this may seem complex, these blocks can be quite trivial to implement, depending upon the accuracy required.

Figure 5 shows a bipolar circuit that we constructed to find the median of three points. The gm limiters are just the differential pairs which naturally limit at a differential input of about 3 kT/q. A current mirror is used to convert the summed differential currents into a voltage. This circuit may be thought of as simply an operational transconductance amplifier tied in unity gain mode, except that it has three pairs of inputs instead of just one. The accuracy of this circuit in finding the median is limited by several factors including the matching of the tail currents, the finite gain of the diff pairs in their active region, and the finite output impedance of the devices.

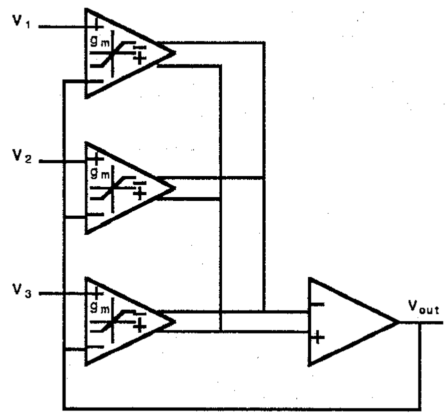

Figure 4. Block diagram of a three-input analog median circuit.

In many ways, building an analogous circuit in CMOS technologies is more challenging. The major difficult lies in the lack of sharpness in the transfer function of the MOS diff pair, restricting its usefulness to low accuracy applications. We solve this problem by adding an additional gain stage in front of the limiting diff pair.

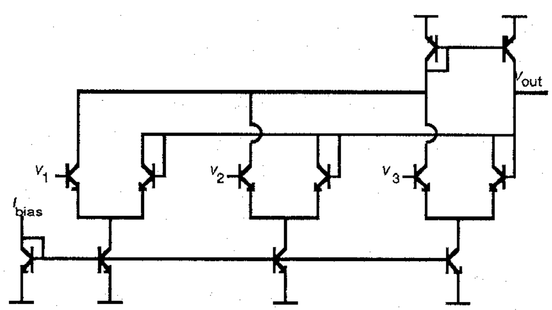

Figure 5. A simple three-input bipolar median circuit.

In order to demonstrate the viability of CMOS median circuits, we have designed a three-input median circuit on a 2μm CMOS process and fabricated it through the MOSIS foundry service. A schematic of the test circuit appears as figure 6. The limiting gm block is implemented with a folded differential preamp driving essentially resistive loads. This folding greatly increases the input common-mode range. Additionally, the output of the preamp is crudely clamped to ease the output impedance requirements of the main diff pair's tail current source. Thus the main diff pair sees only small common-mode and differential mode signals, improving the limiting characteristic considerably.

The currents are summed into a simple current mirror whose high impedance output creates the circuit's dominant pole. Other poles are created by the preamp. By limiting the gain, the driving point impedances are kept fairly low, reducing their effect on stability.

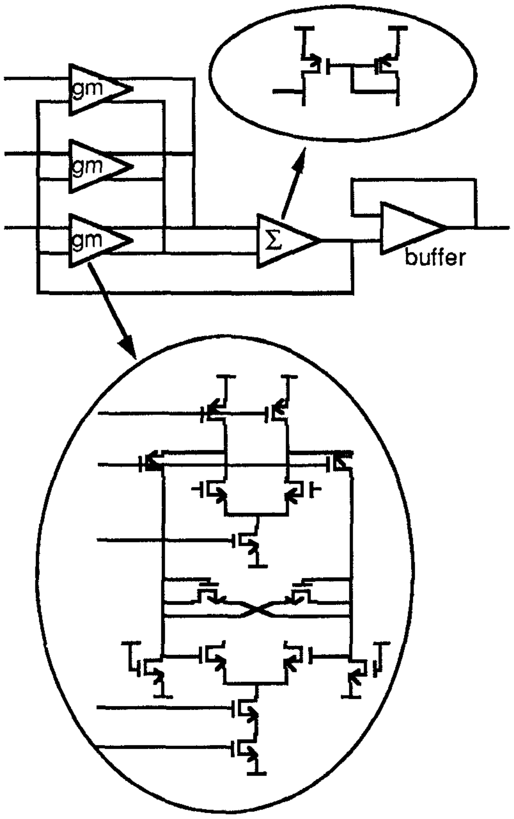

Figure 6. Simplified schematic of the CMOS three-point median test circuit.

4. Experimental Results

Laboratory measurements are summarized in table 1. All measurements were made using an in-circuit unity gain buffer. The circuit consistently produced an output that was a close estimate of the median of its inputs. Figures 7, 8, and 9 show the performance of the circuit. Figure 7 plots V1 versus Vout when the other two inputs are tied to opposite rails, demonstrating the large input/output range. Swapping the two rail tied inputs had an almost negligible effect on the curve, revealing that tail current source mismatch is not a significant source of error.

An extremely demanding test for this type of median circuit occurs when two inputs are the same and the third is swept from rail to rail. In this case the two matched inputs are servoed to half the limit current so as to balance the current from the third. Figure 8 graphs this experiment. As V1 is swept from 0 V to 5 V, the output is servoed to force plus half the limiting current to minus half the limiting current from the two matched input limiting gm stages. Since the output jumps 9.5 mV, we can conclude that the width of the limiting function to go from 25% to 75% is 9.5 mV.

A more direct measurement of the limiting function is given by figure 9. This is the same experiment, except with the free input varied over a very small range. Where the curve first starts to bend up is where the free input's corner is, or more specifically, around 0 mV differential input. Similarly, the top corner graph gives the other corner of the limit, which is around 35 mV differential input. Therefore, the total width of the limiting function is about 35 mV.

Technology	2 µm CMOS
Circuit Size	0.32 mm^2
Power Supply	5 V
Power Drain	5.6 mW
Input/Output Range	0.8 V to 4.5 V
Gain	.994 to .995 from each channel
Offset	±<10 mV each channel in unity gain
Max response to non-median input	±5 mV
Small Signal Bandwidth	1.4 MHz. / active input
Slew Rate	1.2 V / µs or 3.6 V / µs (dependent on state)

Table 1. Median test circuit measurements, including biasing and output buffers.

AC testing was complicated by the multiple inputs. Small signal bandwidth is a function of how many inputs are being driven, and whether or not the signal is clearly the median. Slew rate depends upon the current balance state which can be either 3 vs. 0 or 2 vs. 1. It is not clear how to evaluate cross channel effects at high frequency.

5. Discussion

In this work, we have shown that simple analog circuits can be used to find the median. Their compactness allows their use in parallel systems, such as pixel plane processing, yielding enormous effective computation rates. In addition, their analog nature allows them to be easily incorporated into systems where digital median filters are impractical, such as high speed communications equipment.

More generally, the technique described can be used to implement a large class of non-linear filters based on rank order. By adding current in the summation, we can force the circuit to servo on the min, max, or any rank input. There is a very large body of literature on non-linear filters, summarized in [3].

Finally, we must note that the filter we have created is really an M - filter, which approaches a median filter only in the limit. However, M - filters are interesting in and of themselves, being a compromise between linear and median filters, and this work suggests their simplicity in analog implementations.

6. Acknowledgements

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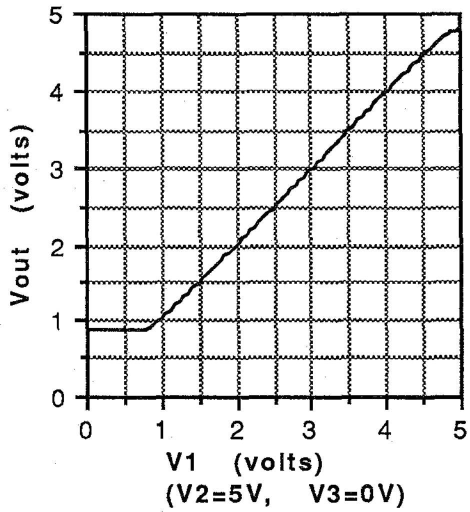

Figure 7. Median circuit output for V1 swept from 0V to 5V, V2 = 5V, and V3 = 0V.

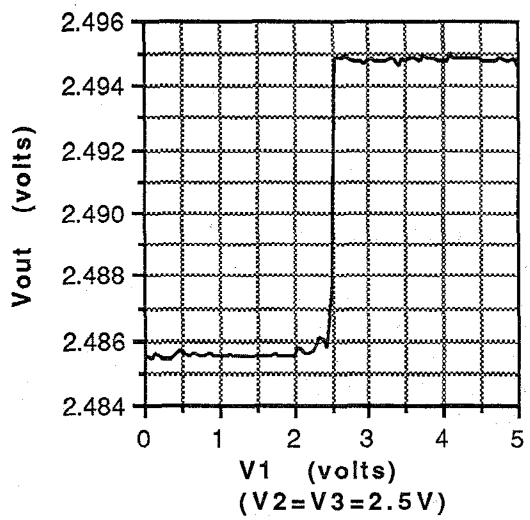

Figure 8. Median circuit output for V1 swept from 0V to 5V, V2 = 2.5V, and V3 = 2.5V.

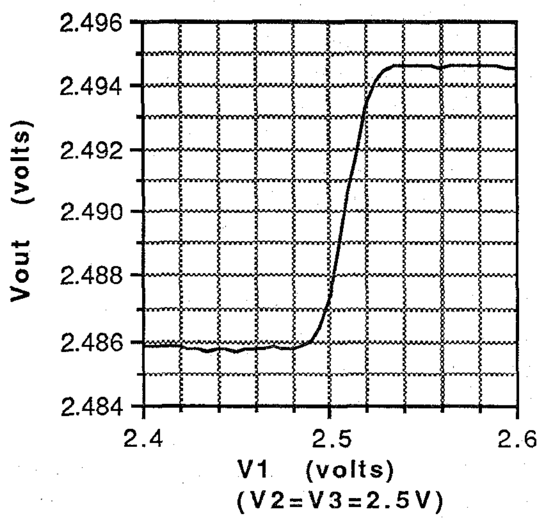

Figure 9. Median circuit output for V1 swept from 2.4V to 2.6V, V2 = 2.5V, and V3 = 2.5V.

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