TEXAS INSTRUMENTS
TPS61088
ZHCSDP8D – MAY 2015 – REVISED AUGUST 2021

TPS61088 10A 全集成同步升压转换器

1 特性

- 2.7V 至 12V 输入电压范围
- 4.5V 至 12.6V 输出电压范围
- 10A 开关电流
- 效率高达 91%（V_{IN} = 3.3V、V_{OUT} = 9V 且 I_{OUT} = 3 A 时）
- 在轻负载条件下，有 PFM 模式和强制 PWM 模式可供选择
- 关断期间，流入 VIN 引脚的电流为 1.0μA
- 可通过电阻编程的开关峰值电流限制
- 可调开关频率：200kHz 至 2.2MHz
- 可编程软启动
- 13.2V 输出过压保护
- 逐周期过流保护
- 热关断
- 20 引脚 4.50mm × 3.50mm VQFN 封装
- 使用 TPS61088 并借助 *WEBENCH Power Designer* 创建定制设计方案

2 应用

- 便携式刷卡机 (POS) 终端
- Bluetooth™ 扬声器
- 电子烟
- Thunderbolt 接口
- 快充移动电源

3 说明

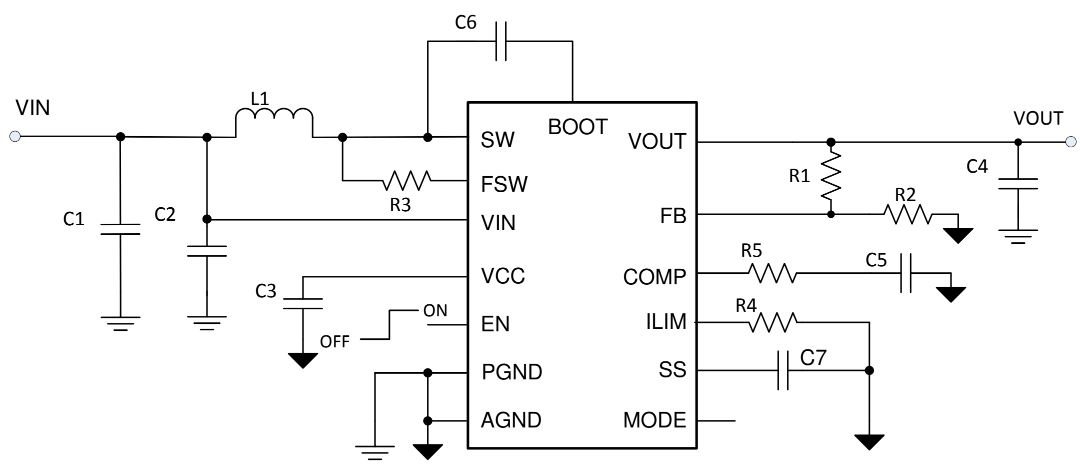
TPS61088 是一款高功率密度的全集成同步升压转换器，配有一个 11mΩ 功率开关和一个 13mΩ 整流器开关，可为便携式系统提供高效率的小尺寸解决方案。TPS61088 具有 2.7V 至 12V 的宽输入电压范围，可支持由单芯或两芯锂电池供电的应用。该器件具备 10A 开关电流能力，并且能够提供高达 12.6V 的输出电压。

TPS61088 采用自适应恒定关断时间峰值电流控制拓扑结构来调节输出电压。在中等到重负载条件下，TPS61088 在脉宽调制 (PWM) 模式下工作。在轻负载条件下，该器件可通过 MODE 引脚选择下列两种工作模式之一。一种是可提高效率的脉宽调制 (PFM) 模式；另一种是可避免因开关频率较低而引发应用问题的强制 PWM 模式。可通过外部电阻在 200kHz 至 2.2MHz 范围内调节 PWM 模式下的开关频率。TPS61088 还实现了可编程的软启动功能和可调节的开关峰值电流限制功能。此外，该器件还提供有 13.2V 输出过压保护、逐周期过流保护和热关断保护。

TPS61088 采用 20 引脚 4.50mm × 3.50mm VQFN 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS61088	VQFN (20)	4.50mm × 3.50mm



典型应用电路

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (February 2019) to Revision D (August 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式。........ 1

Changes from Revision B (September 2018) to Revision C (February 2019) — **Page**

- Corrected spelling of 'resister' to 'resistor' in the *Pin Functions* table........ 3
- Added caption to *Functional Block Diagram* as auto-number 图 7-1........ 10
- Added cross-reference hyperlink in the *Enable and Startup* section pointing to C7 reference in 图 8-1........ 10
- Inserted missing cross-reference hyperlink in *节 8.2.2.4* section pointing to 图 8-1 circuit in the *Typical Application* section........ 15

5 Pin Configuration and Functions

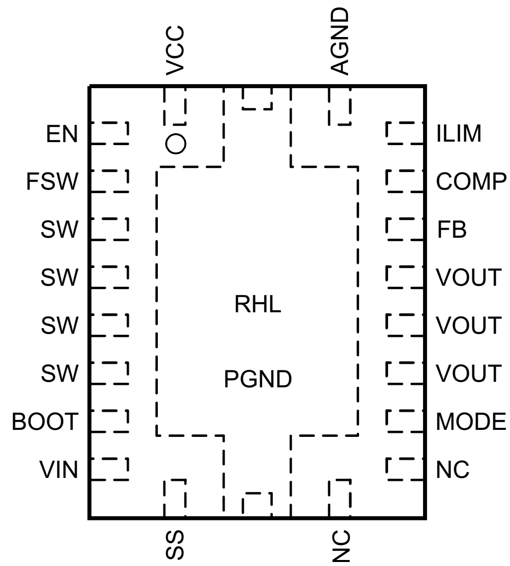

图 5-1. 20-Pin VQFN With Thermal Pad RHL Package(Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VCC	1	O	Output of the internal regulator. A ceramic capacitor of more than 1.0 µF is required between this pin and ground.
EN	2	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode.
FSW	3	I	The switching frequency is programmed by a resistor between this pin and the SW pin.
SW	4, 5, 6, 7	I	The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
BOOT	8	O	Power supply for high-side MOSFET gate driver. A ceramic capacitor of 0.1 µF must be connected between this pin and the SW pin.
VIN	9	I	IC power supply input
SS	10	O	Soft-start programming pin. An external capacitor sets the ramp rate of the reference voltage of the internal error amplifier during soft start.
NC	11, 12	—	No connection inside the device. Connect these two pins to the ground plane on the PCB for good thermal dissipation.
MODE	13	I	Operation mode selection pin for the device in light load condition. When this pin is connected to ground, the device works in PWM mode. When this pin is left floating, the device works in PFM mode.
VOUT	14, 15, 16	O	Boost converter output
FB	17	I	Voltage feedback. Connect to the center tape of a resistor divider to program the output voltage.
COMP	18	O	Output of the internal error amplifier, the loop compensation network must be connected between this pin and the AGND pin.
ILIM	19	O	Adjustable switch peak current limit. An external resistor must be connected between this pin and the AGND pin.
AGND	20	—	Signal ground of the IC
PGND	21	—	Power ground of the IC. It is connected to the source of the low-side MOSFET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
Voltage[(2)]	BOOT	–0.3	SW + 7	V
	VIN, SW, FSW, VOUT	–0.3	14.5	
	EN, VCC, SS, COMP, MODE	–0.3	7	
	ILIM, FB	–0.3	3.6	
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		12	V
V_{OUT}	Output voltage range	4.5		12.6	V
L	Inductance, effective value	0.47	2.2	10	µH
C_I	Input capacitance, effective value	10			µF
C_O	Output capacitance, effective value	6.8	47	1000	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS61088 RHL 20 PINS Standard	TPS61088 RHL 20 PINS EVM	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.8	29.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.8	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.7 V to 5.5 V and T_J = -40°C to 125°C. Typical values are at V_{IN} = 3.6 V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		12	V
V_{IN_UVLO}	Undervoltage lockout (UVLO) threshold	V_{IN} rising			2.7	V
		V_{IN} falling		2.4	2.5	V
V_{IN_HYS}	VIN UVLO hysteresis			200		mV
V_{CC_UVLO}	UVLO threshold	V_{CC} falling		2.1		V
I_Q	Operating quiescent current from the VIN pin	IC enabled, V_{EN} = 2 V, no load, R_{ILIM} = 100 kΩ, V_{FB} = 1.3 V, V_{OUT} = 12 V, T_J up to 85°C		1	3	μA
	Operating quiescent current from the VOUT pin			110	250	μA
I_{SD}	Shutdown current into the VIN pin	IC disabled, V_{EN} = 0 V, no load, no feedback resistor divider connected to the VOUT pin, T_J up to 85°C		1	3	μA
V_{CC}	VCC regulation	I_{VCC} = 5 mA, V_{IN} = 8 V		5.8		V
EN AND MODE INPUT						
V_{ENH}	EN high threshold voltage	V_{CC} = 6 V			1.2	V
V_{ENL}	EN low threshold voltage	V_{CC} = 6 V	0.4			V
R_{EN}	EN internal pull-down resistance	V_{CC} = 6 V		800		kΩ
V_{MODEH}	MODE high threshold voltage	V_{CC} = 6 V			4.0	V
V_{MODEL}	MODE low threshold voltage	V_{CC} = 6 V	1.5			V
R_{MODE}	MODE internal pull-up resistance	V_{CC} = 6 V		800		kΩ
OUTPUT						
V_{OUT}	Output voltage range		4.5		12.6	V
V_{REF}	Reference voltage at the FB pin	PWM mode	1.186	1.204	1.222	V
		PFM mode		1.212		
I_{LKG_FB}	FB pin leakage current	V_{FB} = 1.2 V			100	nA
I_{SS}	Soft-start charging current			5		μA
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} +200 mV, V_{COMP} = 1.5 V		20		μA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} – 200 mV, V_{COMP} = 1.5 V		20		μA
V_{CCLPH}	High clamp voltage at the COMP pin	V_{FB} = 1 V, R_{ILIM} = 100 kΩ		2.3		V
V_{CCLPL}	Low clamp voltage at the COMP pin	V_{FB} = 1.5 V, R_{ILIM} = 100 kΩ, MODE pin floating		1.4		
G_{EA}	Error amplifier transconductance	V_{COMP} = 1.5 V		190		μA/V
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	VCC = 6 V		13	18	mΩ
	Low-side MOSFET on-resistance	VCC = 6 V		11	16.5	mΩ
CURRENT LIMIT						
I_{LIM}	Peak switch current limit in PFM mode	R_{ILIM} = 100 kΩ, V_{CC} = 6 V, MODE pin floating	10.6	11.9	13	A
	Peak switch current limit in FPWM mode	R_{ILIM} = 100 kΩ, V_{CC} = 6 V, MODE pin short to ground	9.0	10.3	11.4	A
V_{ILIM}	Reference voltage at the ILIM pin			1.204		V
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	R_{FREQ} = 301 kΩ, V_{IN} = 3.6 V, V_{OUT} = 12 V		500		kHz
t_{ON_min}	Minimum on-time	R_{FREQ} = 301 kΩ, V_{IN} = 3.6 V, V_{OUT} = 12 V		90	180	ns

Minimum and maximum values are at V_{IN} = 2.7 V to 5.5 V and T_J = -40°C to 125°C. Typical values are at V_{IN} = 3.6 V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
V_{OVP}	Output overvoltage protection threshold	V_{OUT} rising	12.7	13.2	13.6	V
V_{OVP_HYS}	Output overvoltage protection hysteresis	V_{OUT} falling below V_{OVP}		0.25		V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

6.6 Typical Characteristics

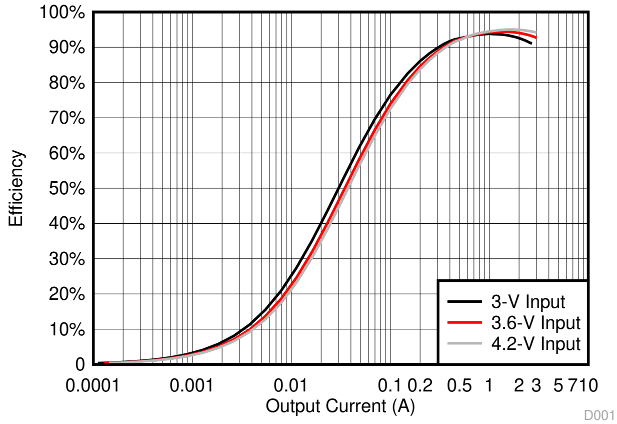

图 6-1. Efficiency vs Output Current, V_{OUT} = 9 V, FPWM

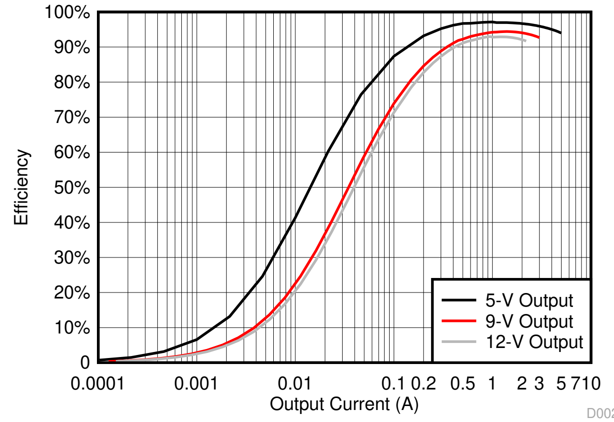

图 6-2. Efficiency vs Output Current, V_{IN} = 3.6 V, FPWM

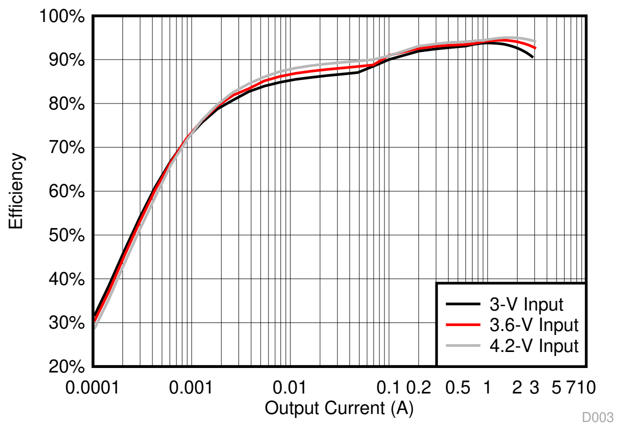

图 6-3. Efficiency vs Output Current, V_{OUT} = 9 V, PFM

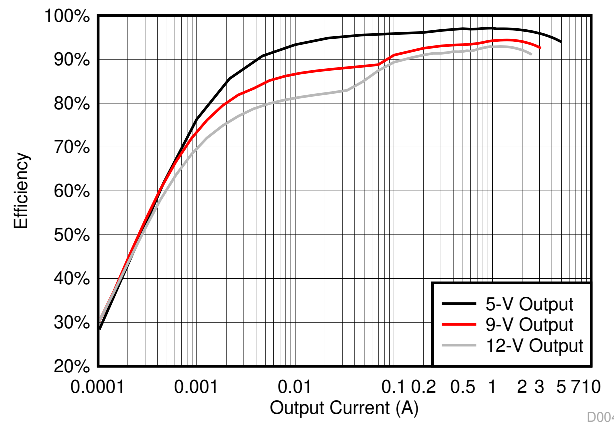

图 6-4. Efficiency vs Output Current, V_{IN} = 3.6 V, PFM

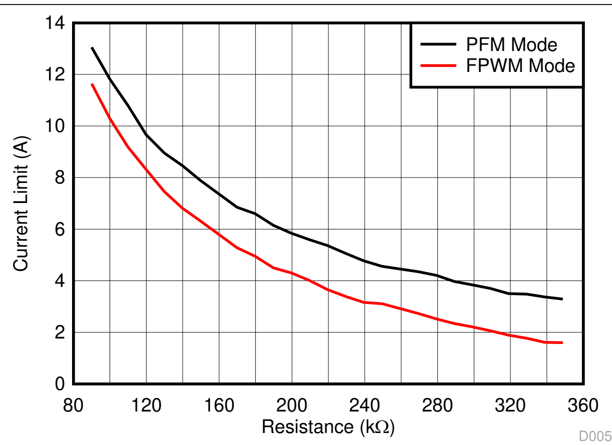

图 6-5. Current Limit vs Setting Resistance

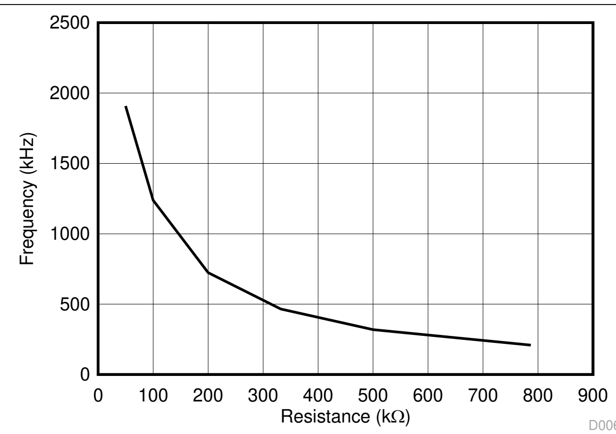

图 6-6. Switching Frequency vs Setting Resistance

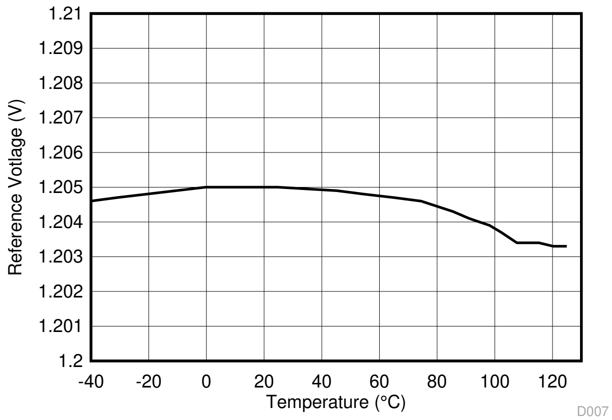

图 6-7. Reference Voltage vs Temperature

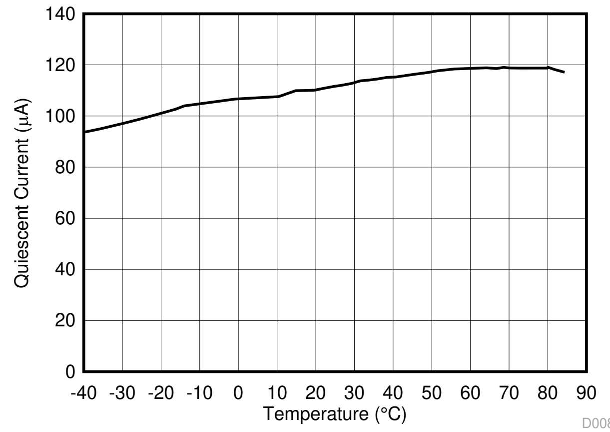

图 6-8. Quiescent Current vs Temperature

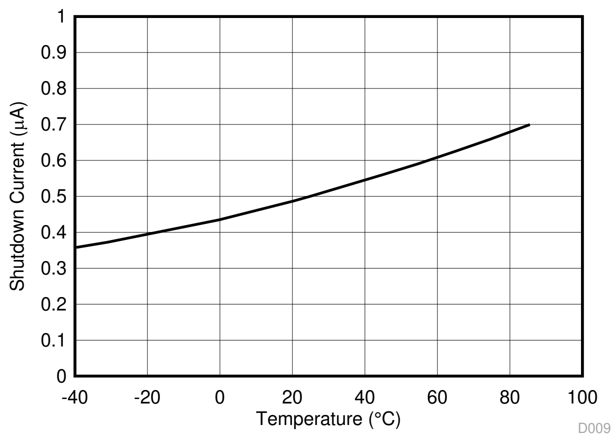

图 6-9. Shutdown Current vs Temperature

7 Detailed Description

7.1 Overview

The TPS61088 is a fully-integrated synchronous boost converter with a 11-mΩ power switch and a 13-mΩ rectifier switch to output high power from a single-cell or two-cell Lithium batteries. The device is capable of providing an output voltage of 12.6 V and delivering up to 30-W power from a single-cell Lithium battery.

The TPS61088 uses adaptive constant off-time peak current control topology to regulate the output voltage. In moderate-to-heavy load condition, the TPS61088 works in the quasi-constant frequency pulse width modulation (PWM) mode. The switching frequency in PWM mode is adjustable ranging from 200 kHz to 2.2 MHz by an external resistor. In light load condition, the device has two operation modes selected by the MODE pin. When the MODE pin is left floating, the TPS61088 works in pulse frequency modulation (PFM) mode. The PFM mode brings high efficiency at the light load. When the MODE pin is short to ground, the TPS61088 works in forced PWM mode (FPWM). The FPWM mode can avoid the acoustic noise and other problems caused by the low switching frequency. The TPS61088 implements cycle-by-cycle current limit to protect the device from overload conditions during boost switching. The switch peak current limit is programmable by an external resistor. The TPS61088 uses external loop compensation, which provides flexibility to use different inductors and output capacitors. The adaptive off-time peak current control scheme gives excellent transient line and load response with minimal output capacitance.

7.2 Functional Block Diagram

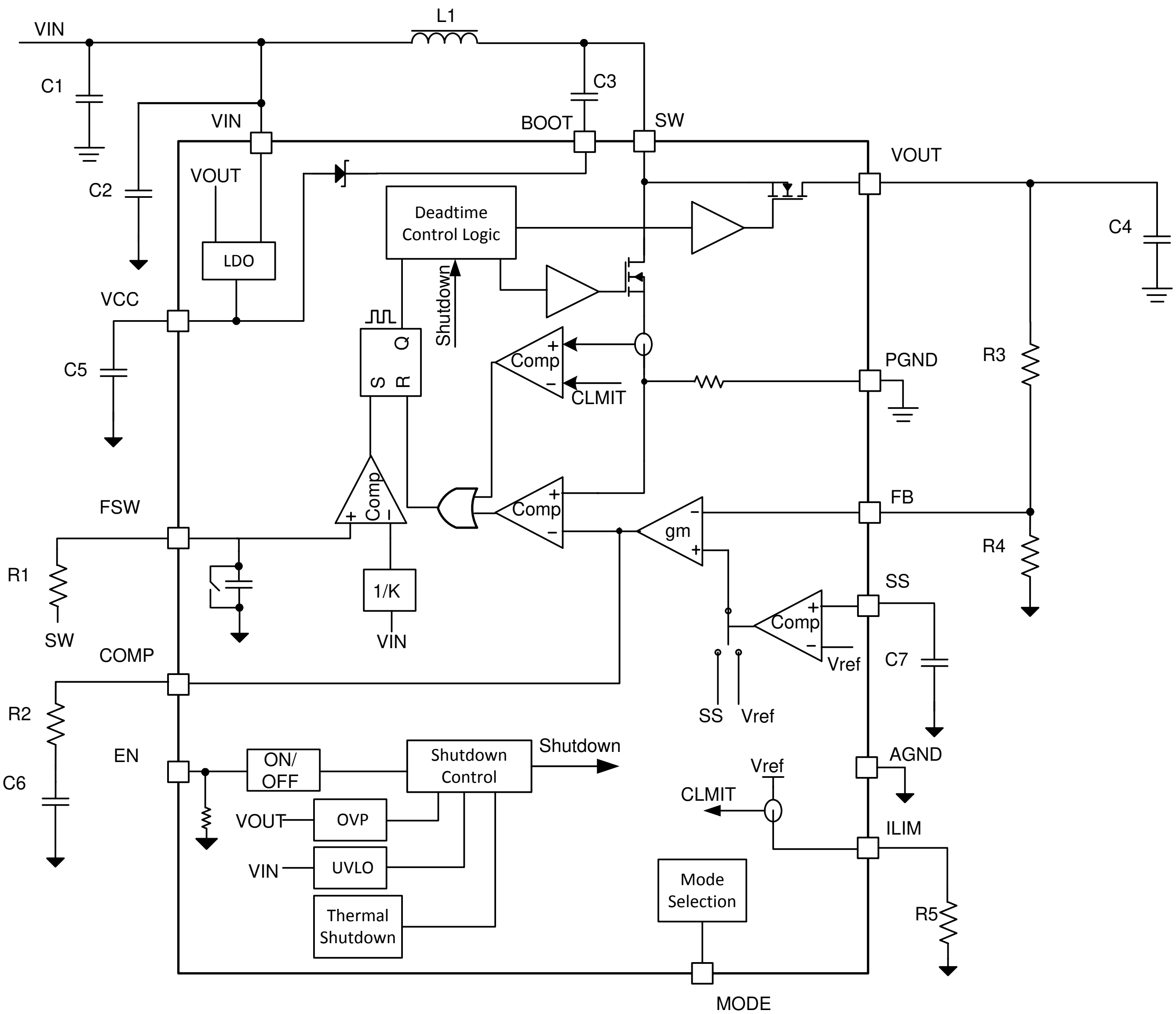

图 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Enable and Start-up

The TPS61088 has an adjustable soft start function to prevent high inrush current during start-up. To minimize the inrush current during start-up, an external capacitor, connected to the SS pin and charged with a constant current, is used to slowly ramp up the internal positive input of the error amplifier. When the EN pin is pulled high, the soft-start capacitor C_{SS} (C7 in 图 8-1) is charged with a constant current of 5 μA typically. During this time, the SS pin voltage is compared with the internal reference (1.204 V), the lower one is fed into the internal positive input of the error amplifier. The output of the error amplifier (which determines the inductor peak current value) ramps up slowly as the SS pin voltage goes up. The soft-start phase is completed after the SS pin voltage exceeds the internal reference (1.204 V). The larger the capacitance at the SS pin, the slower the ramp of the output voltage and the longer the soft-start time. A 47-nF capacitor is usually sufficient for most applications. When the EN pin is pulled low, the voltage of the soft-start capacitor is discharged to ground.

Use 方程式 1 to calculate the soft-start time.

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}} \quad (1)$$

where

- t_{SS} is the soft start time
- V_{REF} is the internal reference voltage of 1.204 V
- C_{SS} is the capacitance between the SS pin and ground
- I_{SS} is the soft-start charging current of 5 µA

7.3.2 Undervoltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The TPS61088 has both VIN UVLO function and VCC UVLO function. It disables the device from switching when the falling voltage at the VIN pin trips the UVLO threshold V_{IN_UVLO} , which is typically 2.4 V. The device starts operating when the rising voltage at the VIN pin is 200 mV above V_{IN_UVLO}. It also disables the device when the falling voltage at the VCC pin trips the UVLO threshold V_{CC_UVLO}, which is typically 2.1 V.

7.3.3 Adjustable Switching Frequency

This device features a wide adjustable switching frequency ranging from 200 kHz to 2.2 MHz. The switching frequency is set by a resistor connected between the FSW pin and the SW pin of the TPS61088. A resistor must always be connected from the FSW pin to SW pin for proper operation. The resistor value required for a desired frequency can be calculated using 方程式 2.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \times \frac{V_{OUT}}{V_{IN}}\right)}{C_{FREQ}} \quad (2)$$

where

- R_{FREQ} is the resistance connected between the FSW pin and the SW pin
- C_{FREQ} is 23 pF
- f_{SW} is the desired switching frequency
- t_{DELAY} is 89 ns
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

7.3.4 Adjustable Peak Current Limit

To avoid an accidental large peak current, an internal cycle-by-cycle current limit is adopted. The low-side switch is turned off immediately as soon as the switch current touches the limit. The peak switch current limit can be set by a resistor at the ILIM pin to ground. The relationship between the current limit and the resistance depends on the status of the MODE pin.

When the MODE pin is floating, namely the TPS61088, is set to work in the PFM mode at light load, use 方程式 3 to calculate the resistor value:

$$I_{LIM} = \frac{1190000}{R_{ILIM}} \quad (3)$$

where

- R_{ILIM} is the resistance between the ILIM pin and ground
- I_{LIM} is the switch peak current limit

When the resistor value is 100 kΩ, the typical current limit is 11.9 A.

When the MODE pin is connected to ground, namely the TPS61088 is set to work in forced PWM mode at light load, use 方程式 4 to calculate the resistor value.

$$I_{LIM} = \frac{1190000}{R_{ILIM}} - 1.6 \quad (4)$$

When the resistor value is 100 kΩ, the typical current limit is 10.3 A.

Considering the device variation and the tolerance over temperature, the minimum current limit at the worst case can be 1.3 A lower than the value calculated by above equations.

7.3.5 Overvoltage Protection

If the output voltage at the VOUT pin is detected above 13.2 V (typical value), the TPS61088 stops switching immediately until the voltage at the VOUT pin drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.3.6 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 130°C, then the device starts switching again.

7.4 Device Functional Modes

7.4.1 Operation

The synchronous boost converter TPS61088 operates at a quasi-constant frequency pulse width modulation (PWM) in moderate-to-heavy load condition. Based on the V_{IN} to V_{OUT} ratio, a circuit predicts the required off-time of the switching cycle. At the beginning of each switching cycle, the low-side N-MOSFET switch, as shown in 节 7.2, is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips. It turns off the low-side N-MOSFET switch and the inductor current goes through the body diode of the high-side N-MOSFET in a dead-time duration. After the dead-time duration, the high-side N-MOSFET switch is turned on. Since the output voltage is higher than the input voltage, the inductor current decreases. The high-side switch is not turned off until the fixed off-time is reached. After a short dead-time duration, the low-side switch turns on again and the switching cycle is repeated.

In light load condition, the TPS61088 implements two operation modes, PFM mode and forced PWM mode, to meet different application requirements. The operation mode is set by the status of the MODE pin. When the MODE pin is connected to ground, the device works in forced PWM mode. When the MODE pin is left floating, the device works in PFM mode.

7.4.1.1 PWM Mode

In forced PWM mode, the TPS61088 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor peak current down, delivering less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the off-time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency in light load condition.

7.4.1.2 PFM Mode

The TPS61088 improves the efficiency at light load with PFM mode. When the converter operates in light load condition, the output of the internal error amplifier decreases to make the inductor peak current down, delivering less power to the load. When the output current further reduces, the current through the inductor decrease to zero during the off-time. Once the current through the high side N-MOSFET is zero, the high-side MOSFET is turned off until the beginning of the next switching cycle. When the output of the error amplifier continuously goes down and reaches a threshold with respect to the peak current of I_{LIM} / 12, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the TPS61088 delivers, the output voltage increases above the nominal setting output voltage. The TPS61088 extends its off-time of the switching period to deliver less energy to the output and regulate the output voltage to 0.7% higher than the nominal setting voltage. With PFM operation mode, the TPS61088 keeps the efficiency above 80% even when the load current decreases to 1 mA. In addition, the output voltage ripple is much smaller at light load due to low peak current. Refer to 图 7-2.

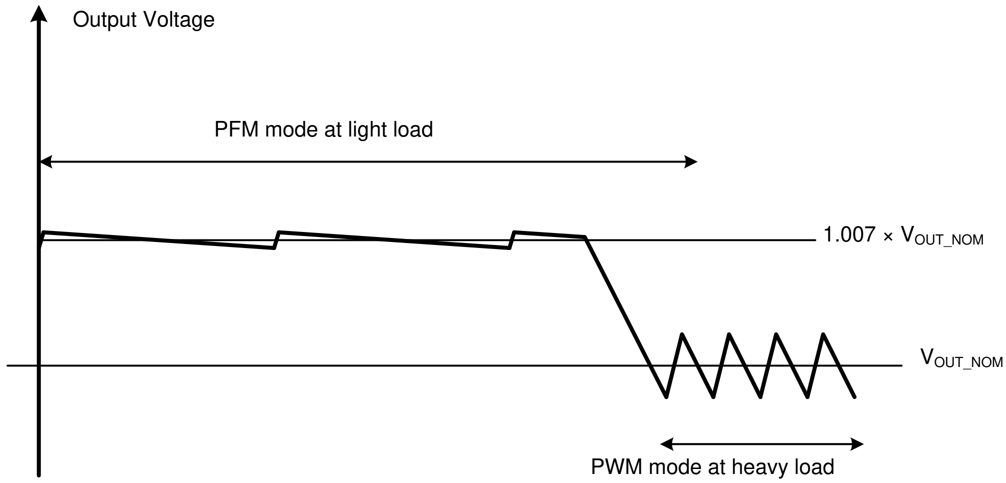

图 7-2. PFM Mode Diagram

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS61088 is designed for outputting voltage up to 12.6 V with 10-A switch current capability to deliver more than 30-W power. The TPS61088 operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate-to-heavy load condition. In light load condition, the converter can either operate in PFM mode or in forced PWM mode according to the mode selection. The PFM mode brings high efficiency over entire load range, but PWM mode can avoid the acoustic noise as the switching frequency is fixed. The converter uses the adaptive constant off-time peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The TPS61088 can work with different inductor and output capacitor combination by external loop compensation. It also supports adjustable switching frequency ranging from 200 kHz to 2.2 MHz.

8.2 Typical Application

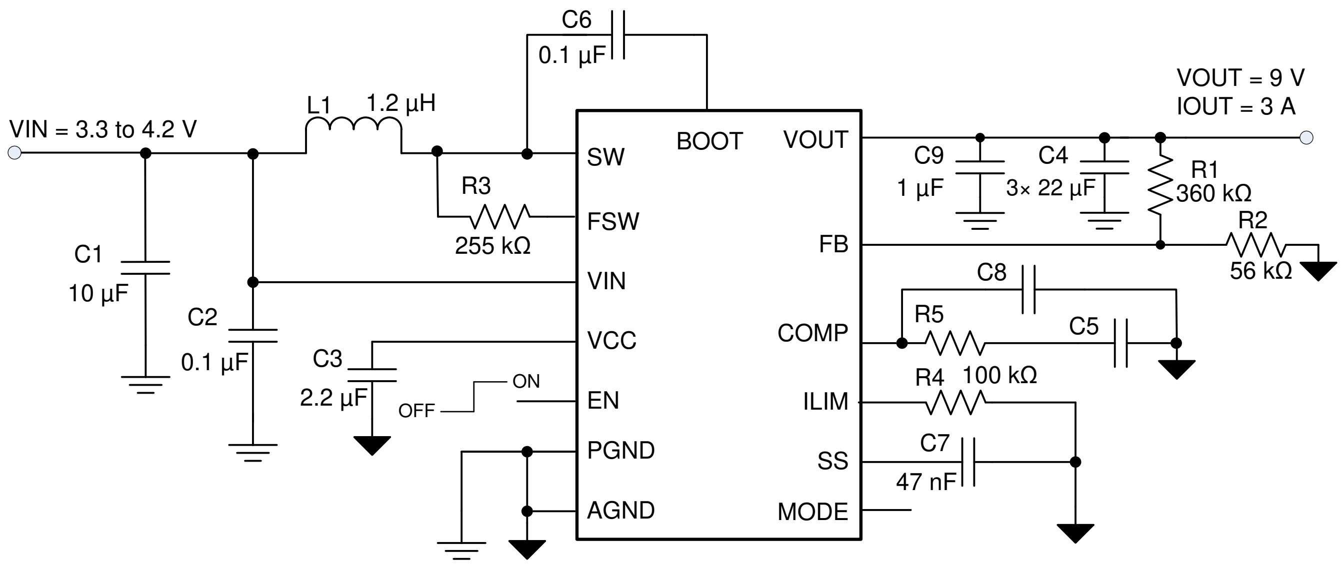

图 8-1. TPS61088 3.3 V to 9-V/3-A Output Converter

8.2.1 Design Requirements

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	3.3 to 4.2 V
Output voltage	9 V
Output voltage ripple	100 mV peak to peak
Output current rating	3 A
Operating frequency	600 kHz
Operation mode at light load	PFM

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS61088 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.2.2 Setting Switching Frequency

The switching frequency is set by a resistor connected between the FSW pin and the SW pin of the TPS61088. The resistor value required for a desired frequency can be calculated using 方程式 5.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \times \frac{V_{OUT}}{V_{IN}}\right)}{C_{FREQ}} \tag{5}$$

where

- R_{FREQ} is the resistance connected between the FSW pin and the SW pin
- C_{FREQ} is 23 pF
- f_{SW} is the desired switching frequency
- t_{DELAY} is 89 ns
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

8.2.2.3 Setting Peak Current Limit

The peak input current is set by selecting the correct external resistor value correlating to the required current limit. Since the TPS61088 is configured to work in PFM mode in light load condition, use 方程式 6 to calculate the correct resistor value:

$$I_{LIM} = \frac{1190000}{R_{ILIM}} \tag{6}$$

where

- R_{ILIM} is the resistance connected between the ILIM pin and ground
- I_{LIM} is the switching peak current limit

For a typical current limit of 11.9 A, the resistor value is 100 kΩ. Considering the device variation and the tolerance over temperature, the minimum current limit at the worst case can be 1.3 A lower than the value calculated by 方程式 6. The minimum current limit must be higher than the required peak switch current at the lowest input voltage and the highest output power to make sure the TPS61088 does not hit the current limit and can still regulate the output voltage in these conditions.

8.2.2.4 Setting Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in 图 8-1). Typically, a minimum current of 20 μA flowing through the feedback divider gives good accuracy and noise covering. A standard 56-kΩ resistor is typically selected for low-side resistor R2.

The value of R1 is then calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (7)$$

8.2.2.5 Inductor Selection

Because the selection of the inductor affects the steady state operation of the power supply, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The TPS61088 is designed to work with inductor values between 0.47 and 10 µH. A 0.47-µH inductor is typically available in a smaller or lower-profile package, while a 10-µH inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a 10-µH inductor can maximize the output current capability of the controller.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow 方程式 8 to 方程式 10 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductor value with –30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in 方程式 8.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (8)$$

where

- V_{OUT} is the output voltage of the boost regulator
- I_{OUT} is the output current of the boost regulator
- V_{IN} is the input voltage of the boost regulator
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple as in 方程式 9.

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}} \quad (9)$$

where

- I_{PP} is the inductor peak-to-peak ripple
- L is the inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with 方程式 10.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \quad (10)$$

Set the current limit of the TPS61088 higher than the peak current I_{Lpeak}. Then select the inductor with saturation current higher than the setting current limit.

Boost converter efficiency is dependent on the resistance of its current path, the switching loss associated with the switching MOSFETs, and the core loss of the inductor. The TPS61088 has optimized the internal switch resistance. However, the overall efficiency is affected significantly by the DC resistance (DCR) of the inductor, equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, TI would recommend an inductor with lower DCR and ESR. However, there is a tradeoff among the inductance of the inductor, DCR and ESR resistance, and its footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors. 表 8-2 lists recommended inductors for the TPS61088. Verify whether the recommended inductor can support your target application with the previous calculations and bench evaluation. In this application, the Sumida's inductor CDMC8D28NP-1R2MC is selected for its small size and low DCR.

表 8-2. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE MAX (L × W × H mm)	VENDOR
CDMC8D28NP-1R2MC	1.2	7.0	12.2 / 12.9	9.5 x 8.7 x 3.0	Sumida
744311150	1.5	7.2	14.0 / 11.0	7.3 x 7.2 x 4.0	Wurth
PIMB104T-2R2MS	2.2	7.0	18 / 12	11.2 × 10.3 × 4.0	Cyntec
PIMB103T-2R2MS	2.2	9.0	16 / 13	11.2 × 10.3 × 3.0	Cyntec
PIMB065T-2R2MS	2.2	12.5	12 / 10.5	7.4 × 6.8 × 5.0	Cyntec

8.2.2.6 Input Capacitor Selection

For good input voltage filtering, TI recommends low-ESR ceramic capacitors. The VIN pin is the power supply for the TPS61088. A 0.1-µF ceramic bypass capacitor is recommended as close as possible to the VIN pin of the TPS61088. The VCC pin is the output of the internal LDO. A ceramic capacitor of more than 1.0 µF is required at the VCC pin to get a stable operation of the LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasite inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 10-µF input capacitance is sufficient for most applications.

Note

DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. The differences between the rated capacitor value and the effective capacitance result from package size and voltage rating in combination with material. A 10-V rated 0805 capacitor with 10 µF can have an effective capacitance of less 5 µF at an output voltage of 5 V.

8.2.2.7 Output Capacitor Selection

For small output voltage ripple, TI recommends a low-ESR output capacitor like a ceramic capacitor. Typically, three 22-µF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Take care when evaluating the derating of a capacitor under DC bias. The bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the following equations to calculate the minimum required effective capacitance C_{OUT}:

$$V_{ripple\_dis} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (11)$$

$$V_{ripple\_ESR} = I_{Lpeak} \times R_{C\_ESR} \quad (12)$$

where

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor
- V_{IN_MIN} is the minimum input voltage of boost converter
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- I_{Lpeak} is the peak current of the inductor
- f_{SW} is the converter switching frequency
- R_{C_ESR} is the ESR of the output capacitors

8.2.2.8 Loop Stability

The TPS61088 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network comprised of resistor R5, ceramic capacitors C5 and C8 is connected to the COMP pin.

The power stage small signal loop response of constant off-time (COT) with peak current control can be modeled by 方程式 13.

$$G_{PS}(S) = \frac{R_O \times (1 - D)}{2 \times R_{sense}} \times \frac{\left(1 + \frac{S}{2 \times \pi \times f_{ESRZ}}\right)\left(1 - \frac{S}{2 \times \pi \times f_{RHPZ}}\right)}{1 + \frac{S}{2 \times \pi \times f_P}} \quad (13)$$

where

- D is the switching duty cycle
- R_O is the output load resistance
- R_{sense} is the equivalent internal current sense resistor, which is 0.08 Ω

$$f_P = \frac{2}{2\pi \times R_O \times C_O} \quad (14)$$

where

- C_O is output capacitor

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (15)$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor

$$f_{RHPZ} = \frac{R_O \times (1 - D)^2}{2\pi \times L} \quad (16)$$

The COMP pin is the output of the internal transconductance amplifier. 方程式 17 shows the small signal transfer function of compensation network.

$$Gc(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{S}{2 \times \pi \times f_{COMZ}}\right)}{\left(1 + \frac{S}{2 \times \pi \times f_{COMP1}}\right)\left(1 + \frac{S}{2 \times \pi \times f_{COMP2}}\right)} \tag{17}$$

where

- G_{EA} is the transconductance of the amplifier
- R_{EA} is the output resistance of the amplifier
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- f_{COMP1}, f_{COMP2} are the poles' frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The next step is to choose the loop crossover frequency, f_C. The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R5, C5, and C8 (in 图 8-1) by following these equations.

$$R5 = \frac{2\pi \times V_{OUT} \times R_{sense} \times f_C \times C_O}{(1 - D) \times V_{REF} \times G_{EA}} \tag{18}$$

where

- f_C is the selected crossover frequency

The value of C5 can be set by 方程式 19.

$$C5 = \frac{R_O \times C_O}{2R5} \tag{19}$$

The value of C8 can be set by 方程式 20.

$$C8 = \frac{R_{ESR} \times C_O}{R5} \tag{20}$$

If the calculated value of C8 is less than 10 pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

8.2.3 Application Curves

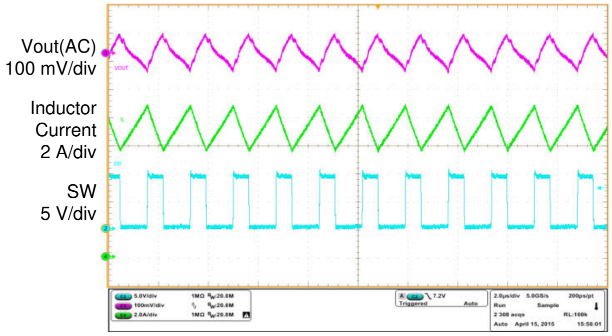

图 8-2. Switching Waveforms in CCM

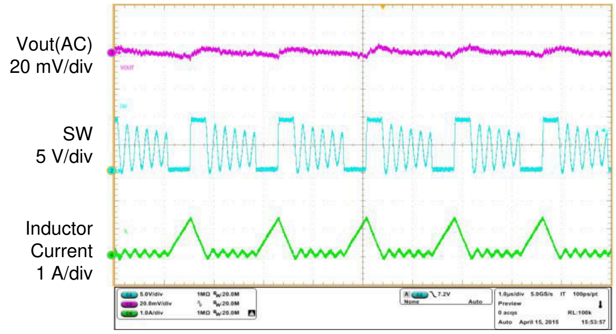

图 8-3. Switching Waveforms in DCM

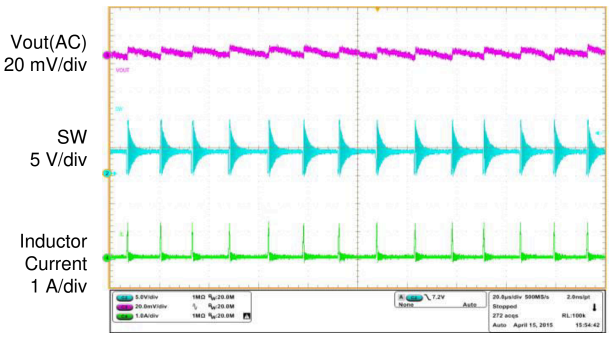

图 8-4. Switching Waveforms in PFM Mode

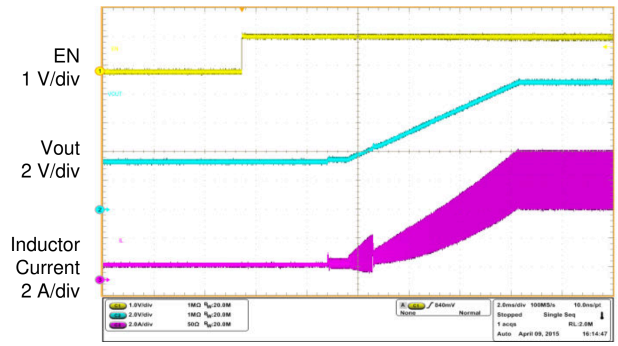

图 8-5. Startup Waveforms

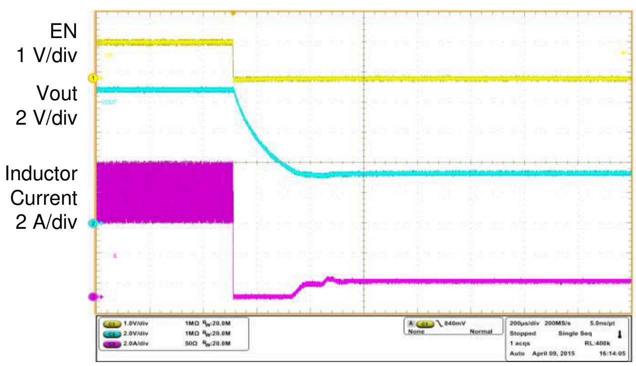

图 8-6. Shutdown Waveforms

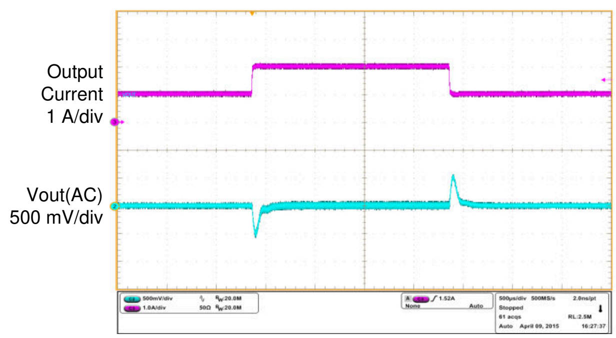

图 8-7. Load Transient (V_{OUT} = 9 V, I_{OUT} = 1 to 2 A)

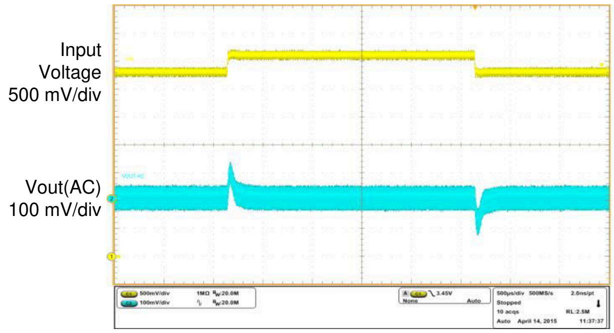

图 8-8. Line Transient (V_{OUT} = 9 V, V_{IN} = 3.3 to 3.6 V)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V to 12 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 µF.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

The input capacitor needs to be close to the VIN pin and GND pin in order to reduce the I_{input} supply ripple.

The layout should also be done with well consideration of the thermal as this is a high power density device. A thermal pad that improves the thermal capabilities of the package should be soldered to the large ground plate, using thermal vias underneath the thermal pad.

10.2 Layout Example

The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias.

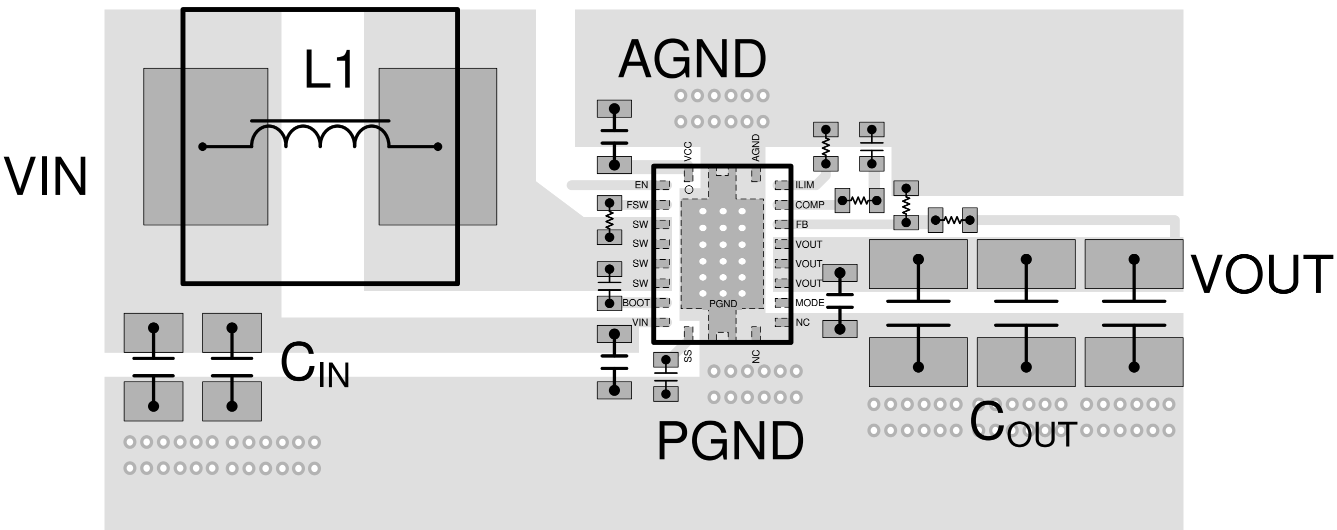

图 10-1. Bottom Layer

10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using 方程式 21.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{21}$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the *Thermal Information* table.

The TPS61088 comes in a thermally-enhanced VQFN package. This package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.1.2 Development Support

11.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS61088 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
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3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61088RHLR	ACTIVE	VQFN	RHL	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S61088A	Samples
TPS61088RHLT	ACTIVE	VQFN	RHL	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S61088A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS61088 :

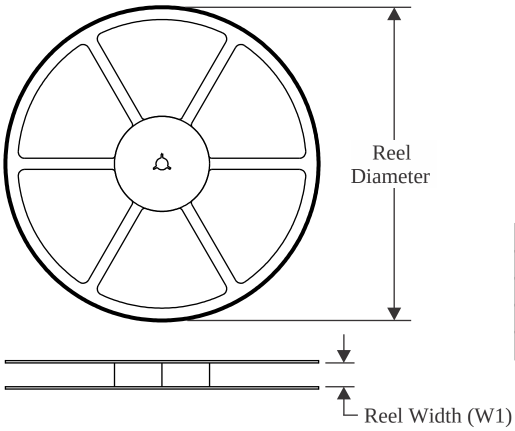
- Automotive : TPS61088-Q1

NOTE: Qualified Version Definitions:

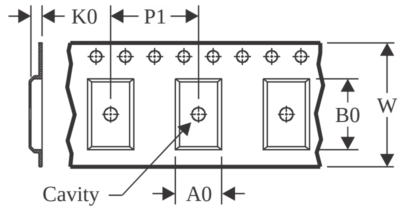
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

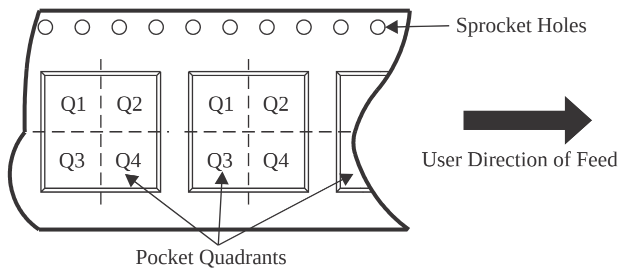


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

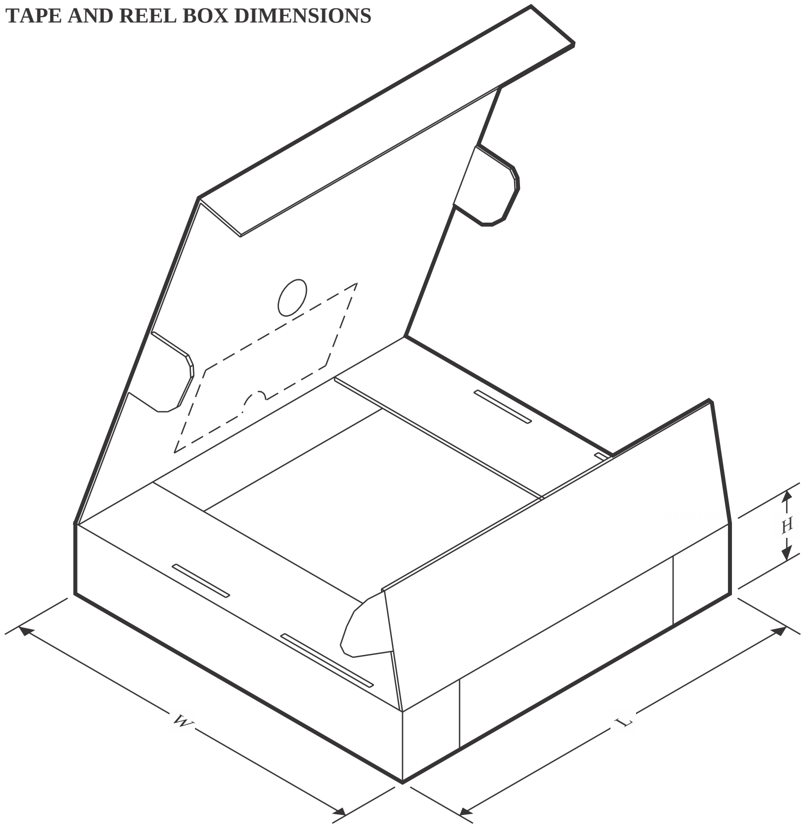
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61088RHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
TPS61088RHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

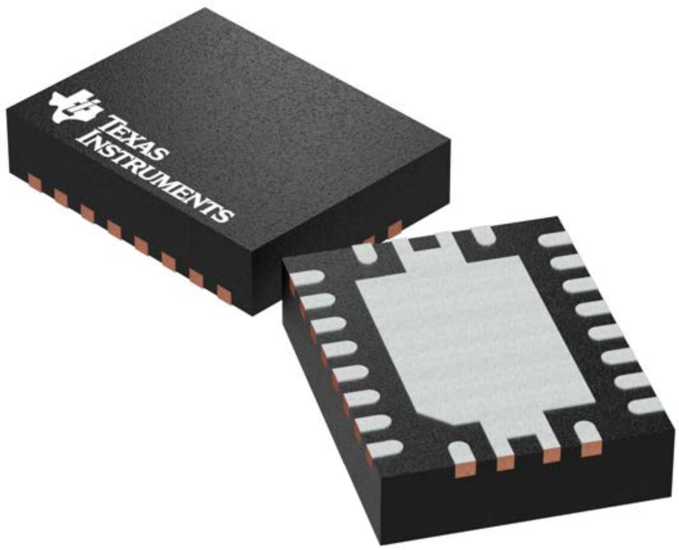
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61088RHLR	VQFN	RHL	20	3000	346.0	346.0	33.0
TPS61088RHLT	VQFN	RHL	20	250	210.0	185.0	35.0

RHL 20

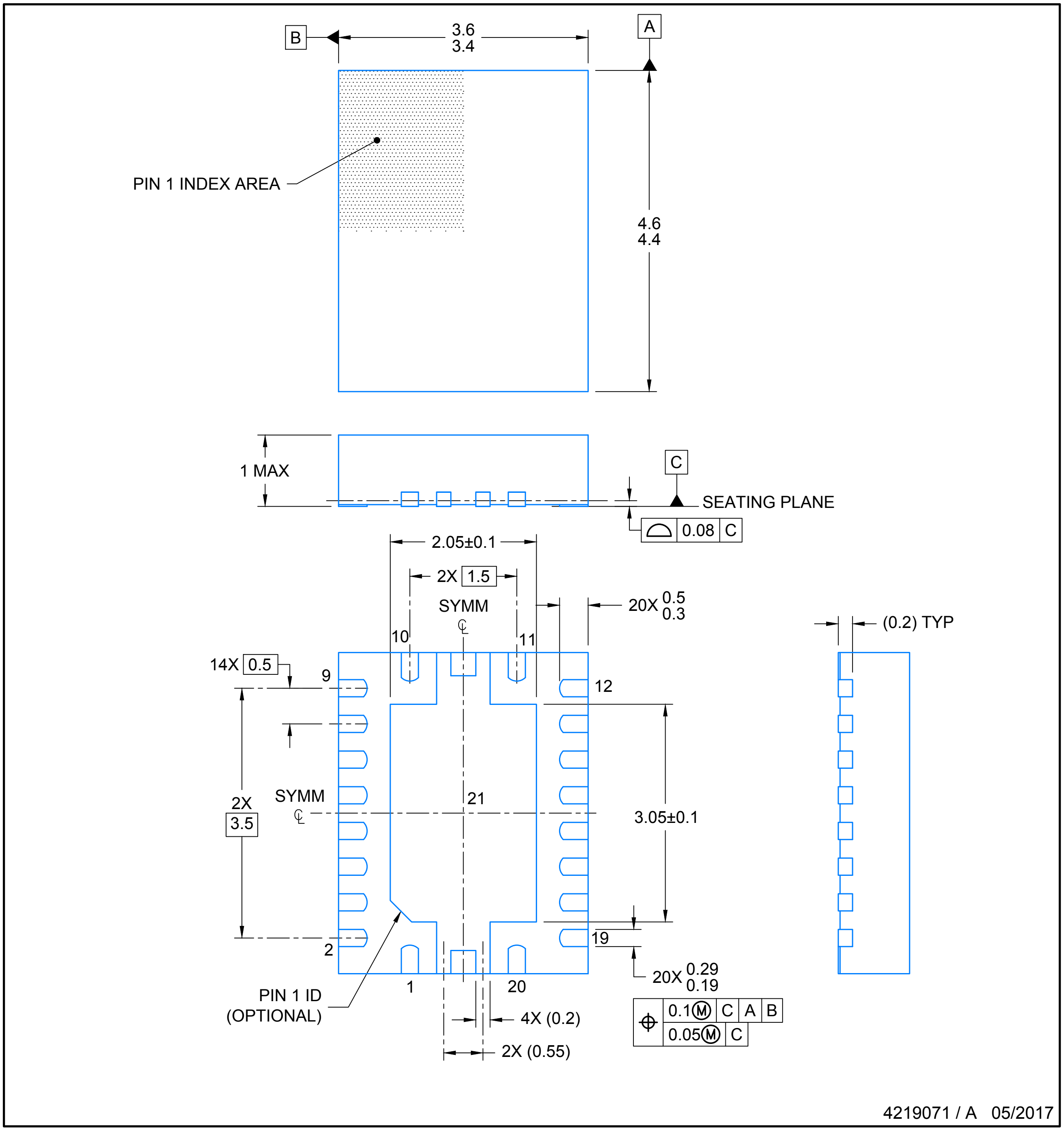
VQFN - 1 mm max height

3.5 x 4.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

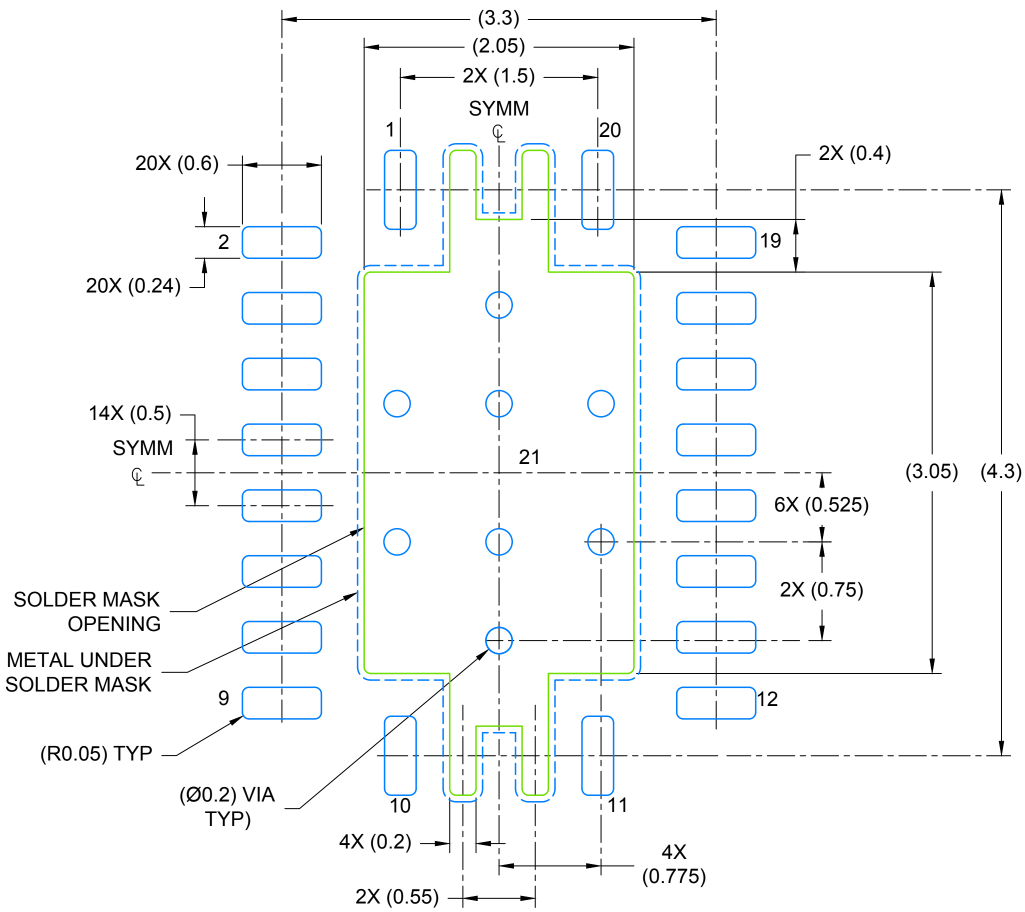


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

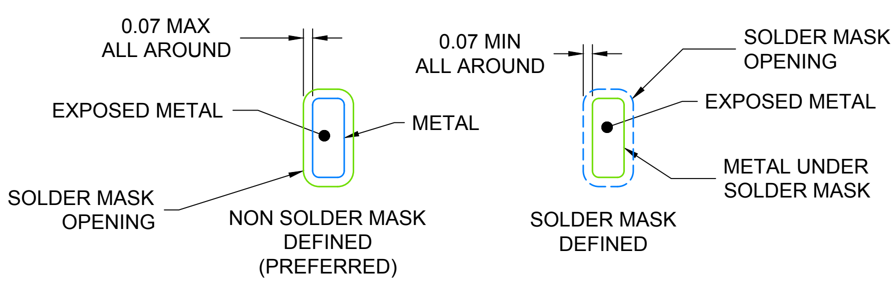


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

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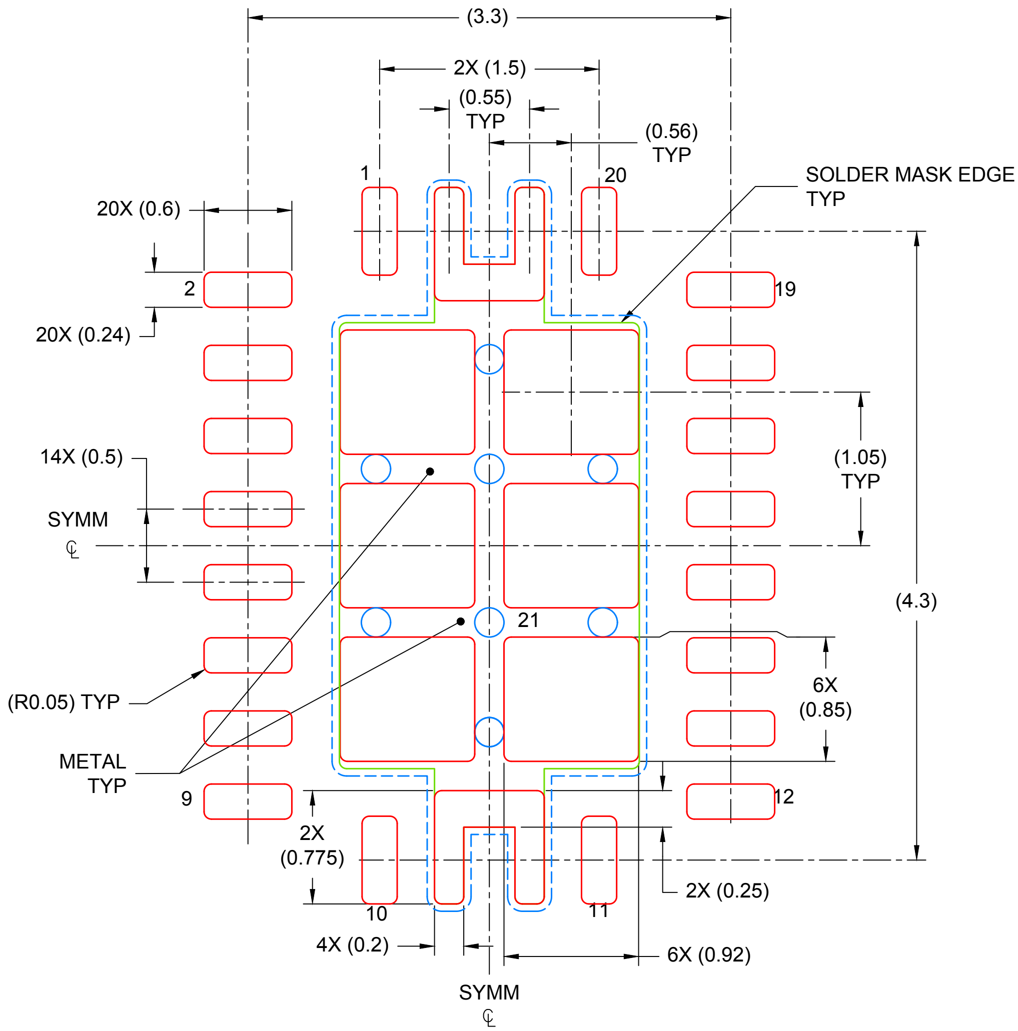
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265