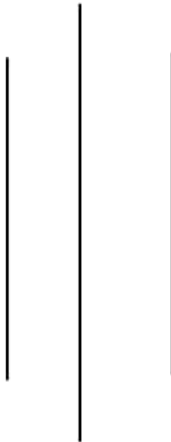


TRIBHUWAN UNIVERSITY

PATAN MULTIPLE CAMPUS



An Assignment on
Assignment No.

Submitted By

Name :

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Section:

Submitted To

Department of CSIT

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RISC vs CISC: A Comparative Analysis of Computer Architecture Paradigms

* RISC (Reduced Instruction Set Computing)

RISC is a CPU design architecture that utilizes a small set of simplified instructions, each executable within a single clock cycle, focusing on optimizing the execution of basic operations through register-to-register operations and a load-store memory access model.

↳ Key Features

- Fixed length instruction format
- Single clock cycle execution per instruction
- Load-store architecture
- Large register set.
- Hardware-based pipelining.
- Register-to-register operations
- Limited addressing modes

↳ Advantages

- Simplified hardware design
- Better instruction pipelining
- Lower power consumption
- Faster instruction execution
- Easier to implement and debug.

↳ Disadvantages

- Requires more RAM for program storage.
- More lines of code needed for complex operations.
- Higher complexity in compiler design
- Limited instruction functionality.
- Requires more registers.

* CISC (Complex Instruction Set Computing)

Cisc is a computer CPU design architecture that implements a large set of complex instructions of varying lengths, capable of performing multi-step operations within a single instruction, with direct memory-to-memory operations support.

↳ Key Features

- Variable length instruction format
- Multi-clock cycle instructions
- Memory-to-memory operations
- Smaller register set
- Multiple addressing modes
- Hardware-handled complexity
- Microcode implementation.

↳ Advantages

- Efficient memory usage
- Backward compability support
- Fewer lines of assembly code needed
- Direct memory-to-memory operations
- Complex operations in a single instructions.

↳ Disadvantages

- Complex decoder circuitry required
- Higher power consumption
- Longer instruction execution time
- More complex hardware design
- Difficult to implement efficient pipelining.