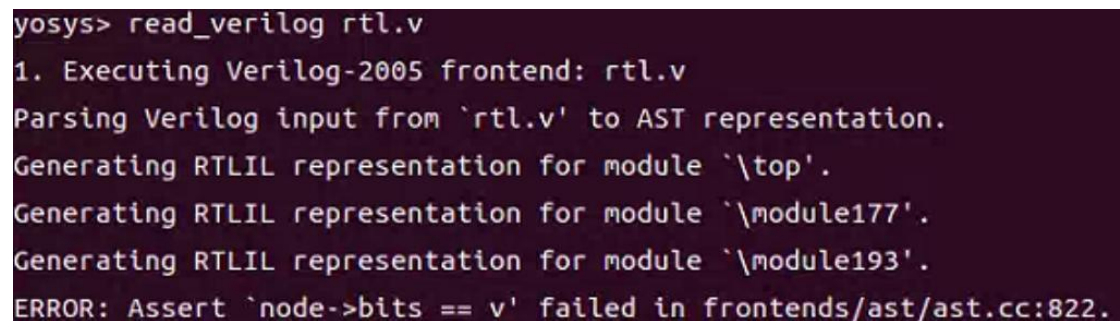


## Yosys Verilog Parsing Error: Issue in AST Generation

Hello,

Version: yosys 0.35+56

While attempting synthesis using Yosys, I encountered an issue. The command `read_verilog rtl.v` resulted in the error message shown in the attached screenshot.



```
yosys> read_verilog rtl.v
1. Executing Verilog-2005 frontend: rtl.v
Parsing Verilog input from `rtl.v' to AST representation.
Generating RTLIL representation for module `\'top'.
Generating RTLIL representation for module `\'module177'.
Generating RTLIL representation for module `\'module193'.
ERROR: Assert `node->bits == v' failed in frontends/ast/ast.cc:822.
```

Synthesis processes as follows:

`read_verilog rtl.v`

`synth`

`write_verilog syn_yosys.v`

The design file (rtl.v) successfully undergoes synthesis using Vivado synthesis tools, indicating that the problem seems to be unique to Yosys.

Please find attached the code of RTL .

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.

## **Expected Behavior**

synthesis success

## **Actual Behavior**

synthesis fail