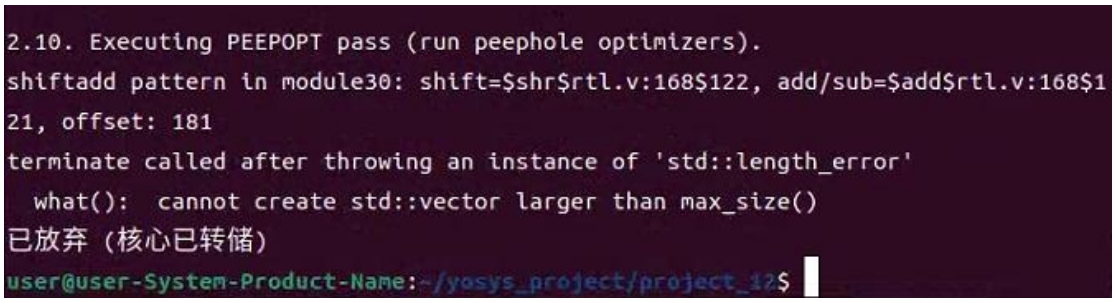
Issue in Yosys Synthesis: 'std::length_error' Leads to Termination

Hello,

Version: yosys 0.35+56

While undergoing the synthesis procedure using Yosys, I encountered a complication when processing the design file (rtl.v). The execution of the read_verilog rtl.v command resulted in an error, as indicated in the provided screenshot. This issue arose during the optimization and synthesis phases of the design using Yosys tools. Specifically, the error pertained to a 'std::length_error,' causing the termination of the synthesis process.



Synthesis processes as follows:

read_verilog rtl.v

synth

write_verilog syn_yosys.v

The Vivado synthesis tools have proven effective in successfully

generating the design file (rtl.v). This positive outcome indicates that the encountered issue is likely exclusive to Yosys, presenting a distinct challenge within that context.

Please find attached the code of RTL .

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.

Expected Behavior

synthesis success

Actual Behavior

synthesis fail