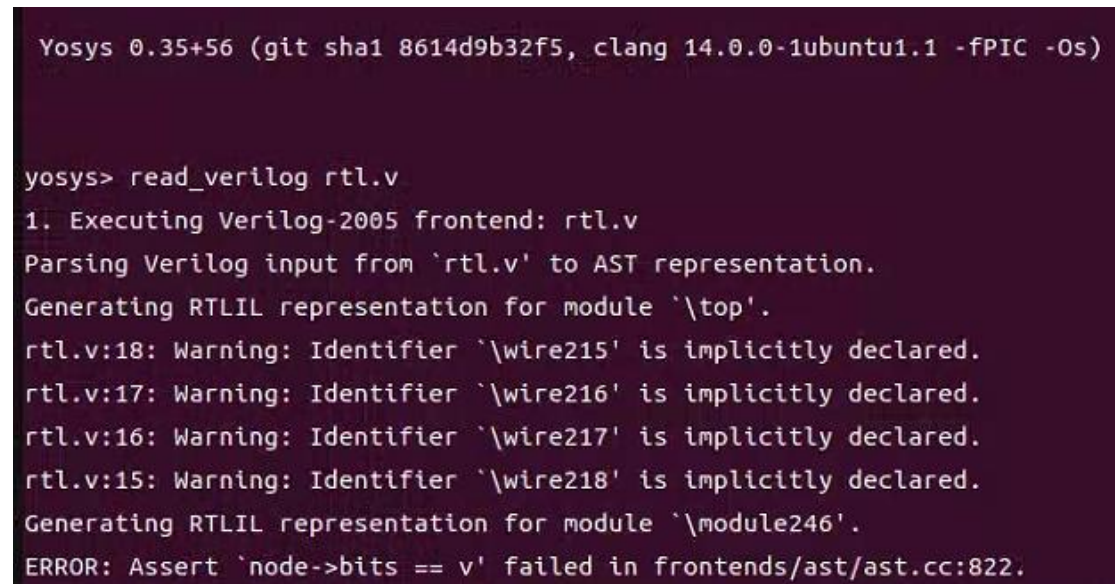


Assertion Failure in AST Processing during Verilog Synthesis

Hello,

Version: yosys 0.35+56

I encountered an issue when using Yosys for synthesis. After running ``read_verilog rtl.v`` in Yosys, I received the following error message: `ERROR: Assert `node->bits == v` failed in frontends/ast/ast.cc:822.` (as shown in the screenshot below).



```
Yosys 0.35+56 (git sha1 8614d9b32f5, clang 14.0.0-1ubuntu1.1 -fPIC -Os)

yosys> read_verilog rtl.v
1. Executing Verilog-2005 frontend: rtl.v
Parsing Verilog input from `rtl.v' to AST representation.
Generating RTLIL representation for module `top'.
rtl.v:18: Warning: Identifier `wire215' is implicitly declared.
rtl.v:17: Warning: Identifier `wire216' is implicitly declared.
rtl.v:16: Warning: Identifier `wire217' is implicitly declared.
rtl.v:15: Warning: Identifier `wire218' is implicitly declared.
Generating RTLIL representation for module `module246'.
ERROR: Assert `node->bits == v' failed in frontends/ast/ast.cc:822.
```

Synthesis processes as follows:

`read_verilog rtl.v`

`synth`

`write_verilog syn_yosys.v`

The design file (`rtl.v`) synthesizes successfully using Vivado synthesis tools, demonstrating that the issue appears to be specific to Yosys. The

same Verilog design file is able to undergo synthesis and generate synthesized files without errors when processed with Vivado synthesis tools.

Please find attached the code of RTL .

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.

Expected Behavior

synthesis success

Actual Behavior

synthesis fail