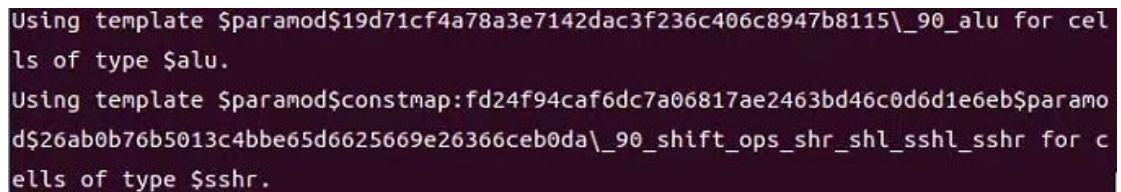


Long runtime and high memory usage for synth on fuzzer generated design eventually producing a small output netlist.

Hello,

Version: yosys 0.35+56

I am using Yosys to read RTL code files and perform synthesis. However, during the synthesis process, Yosys encounters a crash issue, preventing the completion of synthesis (as shown in the screenshot below).



```
Using template $paramod$19d71cf4a78a3e7142dac3f236c406c8947b8115\_90_alu for cells of type $alu.  
Using template $paramod$constmap:fd24f94caf6dc7a06817ae2463bd46c0d6d1e6eb$paramod$26ab0b76b5013c4bbe65d6625669e26366ceb0da\_90_shift_ops_shr_shl_sshl_sshr for cells of type $sshr.
```

Synthesis processes as follows:

read_verilog rtl.v

synth

write_verilog syn_yosys.v

Please find attached the code of RTL and the synthesis log.

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.