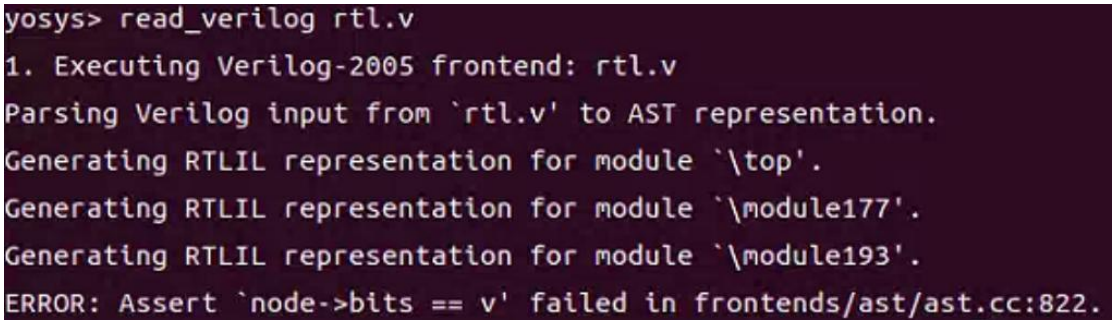
Yosys Verilog Parsing Error: Issue in AST Generation

Hello,

Version: yosys 0.35+56

While attempting synthesis using Yosys, I encountered an issue. The command read_verilog rtl.v resulted in the error message shown in the attached screenshot.



Synthesis processes as follows:

read_verilog rtl.v

synth

write_verilog syn_yosys.v

The design file (rtl.v) successfully undergoes synthesis using Vivado synthesis tools, indicating that the problem seems to be unique to Yosys.

Please find attached the code of RTL .

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.

Expected Behavior

synthesis success

Actual Behavior

synthesis fail