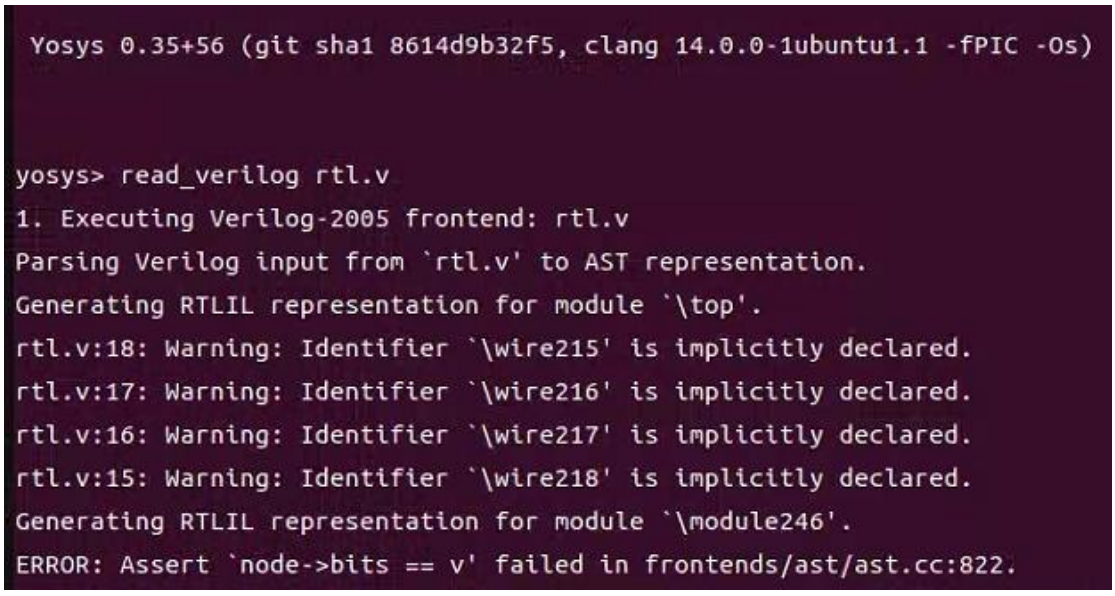
Assertion Failure in AST Processing during Verilog Synthesis

Hello,

Version: yosys 0.35+56

I encountered an issue when using Yosys for synthesis. After running `read_verilog rtl.v` in Yosys, I received the following error message: ERROR: Assert `node->bits == v' failed in frontends/ast/ast.cc:822. (as shown in the screenshot below).



Synthesis processes as follows:

read_verilog rtl.v

synth

write_verilog syn_yosys.v

The design file（rtl.v） synthesizes successfully using Vivado synthesis tools, demonstrating that the issue appears to be specific to Yosys. The

same Verilog design file is able to undergo synthesis and generate synthesized files without errors when processed with Vivado synthesis tools.

Please find attached the code of RTL .

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.

Expected Behavior

synthesis success

Actual Behavior

synthesis fail