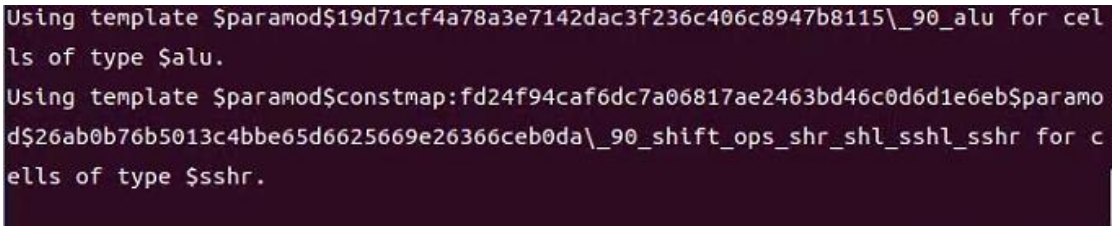
Long runtime and high memory usage for synth on fuzzer generated design eventually producing a small output netlist.

Hello,

Version: yosys 0.35+56

I am using Yosys to read RTL code files and perform synthesis. However, during the synthesis process, Yosys encounters a crash issue, preventing the completion of synthesis (as shown in the screenshot below).



Synthesis processes as follows:

read_verilog rtl.v

synth

write_verilog syn_yosys.v

Please find attached the code of RTL and and the synthesis log.

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.