





Microcontroller Programming (1)

Gerald Kupris, 08.10.2013

Personal Data



Prof. Dr.-Ing. Gerald Kupris geb. 1965

Lehrgebiet: Entwurf eingebetteter Systeme

Start an der HDU: 1.10.2009

Büro: Raum E 105 im ITC1

Ulrichsberger Str. 17

Gebäude: E

Sprechzeit: Donnerstags ab 11:30

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Plan Microcontroller Programming WS2013/14

Block 1: 08:00 - 09:30 Block 2: 09:45 - 11:15 Block 3: 12:00 - 13:30

3. Semester Bachelor AI (Stand: 12.09.2013)

Block 4: 14:00 - 15:30 Block 5: 15:45 - 17:15 Block 6: 17:30 - 19:00

| | Montag | Diens | Dienstag | | Mittwoch | | Donnerstag | | Freitag | |
|---|------------------------------------|---------|--|---------------------------------------|------------|--|--|--|-----------------------------|--|
| 1 | Vertiefte Elektrotechr | I I | Digitaltechnik | SW-Engineering gem. mit MT 5 | | | Messtechnik (bis Mitte Nov) | Einführung GIS LB Zink | | |
| | Bö D 1 | 3 | Bö E 101 | Jr. | ITC1-E 104 | | Wu E 101 | E 101 | | |
| 2 | Messtechnik (ab Mitte Nov) | | Digitaltechnik Praktikum Gruppe 1/2 (14-tägig) | SW-Engineering gem. mit MT 5 | | Bezugssyste me und Positionierung LB Reidelstürz | Nov) | Einführung GIS LB Zink | | |
| 3 | Bö D 1 Messtechnik (ab Mitte | | LabIng Digitaltechnik Praktikum Gruppe 1/2 | Jr SW-Engineering gem. mit MT 5 | ITC1-E 104 | Bezugssyste me und Positionierung | Wu E 101 | Grundlagen der Raumwis- senschaften | | |
| | Nov) Bö A 2: | I I | (14-tägig) LabIng | Jr | ITC1-E 103 | LB Reidelstürz ITC1-E 104 | | LB Reidelstürz /Zink E 101 | | |
| 4 | 14:00 - 15:30 Uhr ► | | Mikrorechnert echnik Vorligs (79) Ku E 104 ITC1-E 104 | | | Mobile Betriebssyste me Do ITC2- Geoinformatik lab. | Vertiefte Elektrotechnik Praktikum Ku ITC1-E 103 | Grundlagen der Raumwis- senschaften LB Reidelstürz / Zink E 101 | | |
| 5 | 15:45 - 17:1 | i Uhr ▶ | Mikrorechnert echnical praktikan E 103 ITC1-E 104 | AWP | | Mobile Betriebssyste me Do ITC2- Geoinformatik lab. | ITC1 E 103 | ◀ 15:4 | 5 - 17:15 | |

Lectures Microcontroller Programming WS2013/14



- 08.10.2013 Microcontroller, Programming and Debuging Interfaces
- 15.10.2013 Reading and Writing of Registers
- 22.10.2013 I/O-Pins, Reading and Writing of Single Bits
- 29.10.2013 Clock Generation, CPU und Computing Power
- 05.11.2013 Interrupts
- 12.11.2013 No lecture!
- 19.11.2013 Memory
- 26.11.2013 Timer and PWM, Watchdog Timer
- 03.12.2013 Analog to Digital Converter
- 10.12.2013 Serial Interfaces: SPI, IIC and UART
- 17.12.2013 Additional Explanation of the Freescale Cup Cars
- 14.01.2014 Project Work on the Freescale Cup Cars
- 21.01.2014 Project Work on the Freescale Cup Cars

Practical Courses Microcontroller Programming



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08.10.2013 Practical Course 1: Preparation of the Work Place
15.10.2013 Practical Course 2: Loading and Debugging of Programs
22.10.2013 Practical Course 3: Using the GPIO Pins
29.10.2013 Practical Course 4: Clock Generation and Calculations
05.11.2013 Practical Course 5: Interrupts
12.11.2013 No Practical Course!
19.11.2013 Practical Course 6: Using the Flash Memory
26.11.2013 Practical Course 7: Timer and Pulse Width Modulation (PWM)
03.12.2013 Practical Course 8: Analog to Digital Conversion
10.12.2013 Practical Course 9: Serial Communication
17.12.2013 Project Work on the Freescale Cup Cars
14.01.2014 Project Work on the Freescale Cup Cars
21.01.2014 Project Work on the Freescale Cup Cars
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Participation on all Practical Courses is required!

Literature Recommendations

Helmut Bähring: Anwendungsorientierte Mikroprozessoren, Mikrocontroller und Digitale Signalprozessoren Springer Verlag 2010

Beierlein / Hagenbruch: Taschenbuch Mikroprozessortechnik Carl Hanser Verlag 2010

Joseph Yiu: The Definitive Guide to the Arm Cortex-M3 Newnes Verlag 2007

Brian W. Kernighan, Dennis M. Ritchie: The C Programming Language

Freescale: K60 Sub-Family Reference Manual

Freescale: Kinetis Peripheral Module Quick Reference

Freescale: CodeWarrior Development Studio for Microcontrollers

V10.x FAQ Guide

Project work at the end of the semester

As a project work at the end of the semester, students will participate at the Freescale Cup.

The Freescale Cup is a global competition where student teams build, program, and race a model car around a track for speed. The fastest car to complete the track without derailing, wins.

Up to 4 students will be together in one team. Up to 10 teams will compete against each other.

Task: Building and Programming of Cars for the Freescale Cup

All teams will register with Freescale.

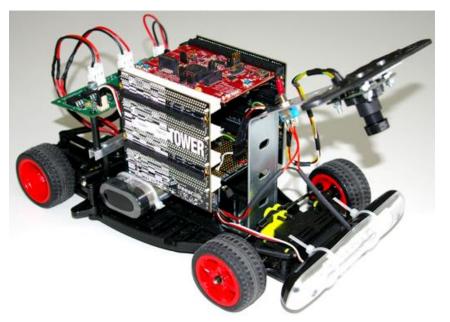
The Semester Final Race will take place in January 2014. The grade of the course will depend on the results of the semester finals.

The best teams will participate in the Germany Final Race in March 2014.

The Freescale Cup Car

The car is build from pre-fabricated, standardized parts and is controlled by a microcontroller.

The camera is looking at the road and is sensing the black line.

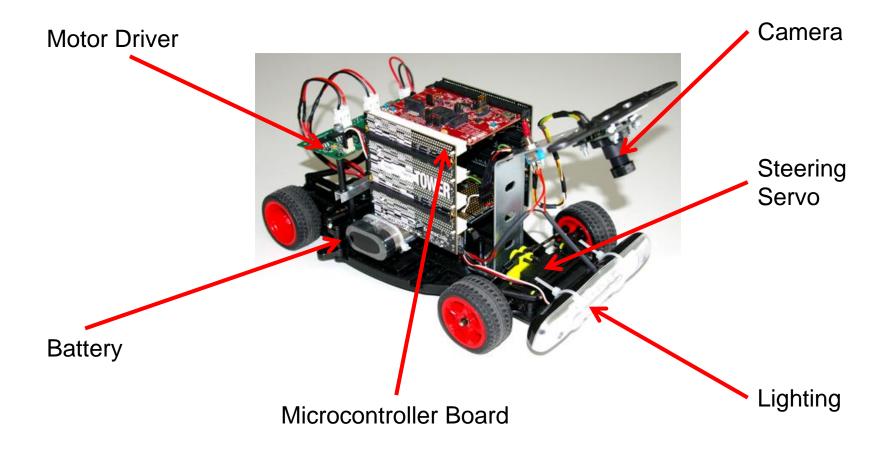




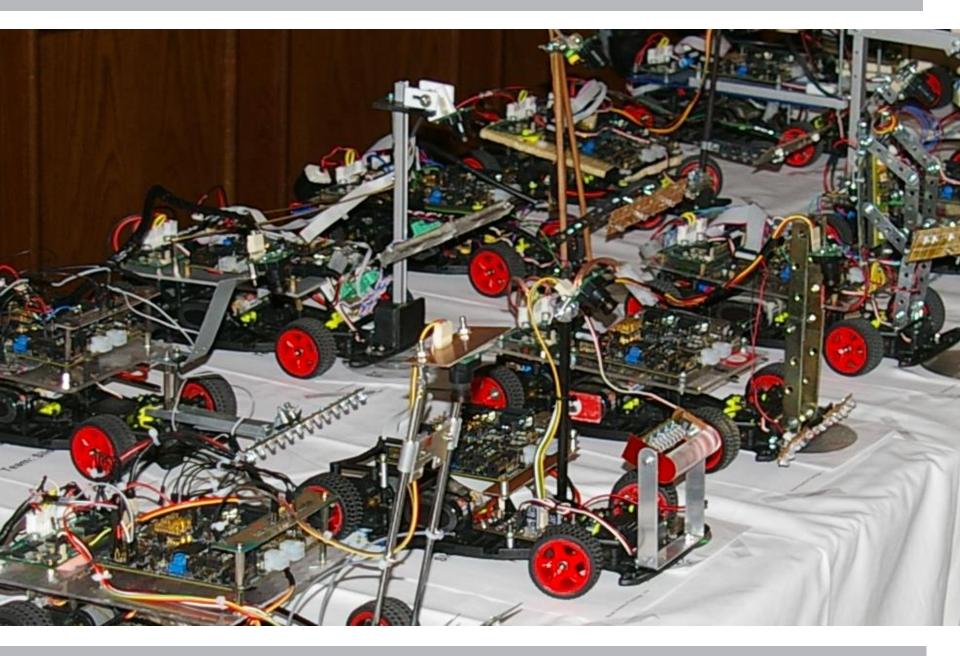




The Freescale Cup Car



ECHNISCHE HOCHSCHULE DEGGENDORF



The Race Track

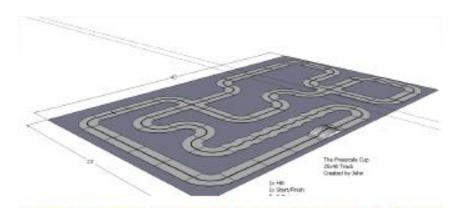
The race track consists of standardized parts. The exact layout of the track is not known and may change from race to race.

The road itself is white with a black line in the middle of the road. Additional elements may be: curves, crossovers, wiggly line, bumpers, hills.

The track has an electronic time measurement system. The car has to go one round as fast as possible and has to stop after one round.

There are official rules available.

We have our training and race track in the next room.

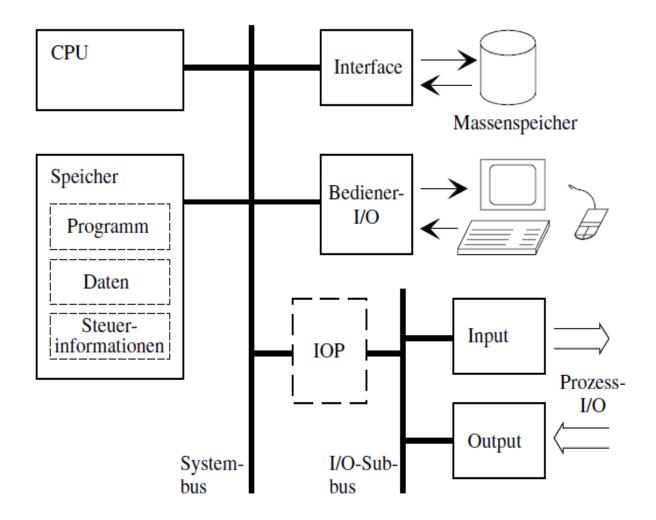




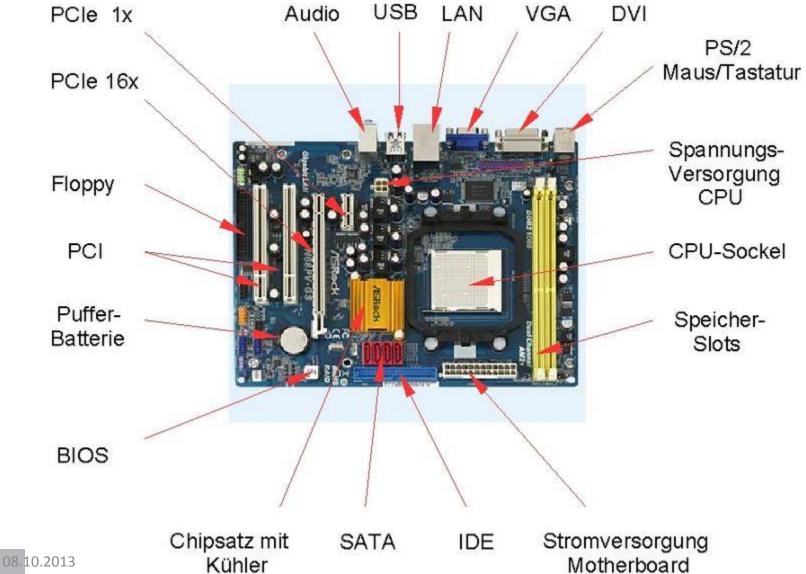




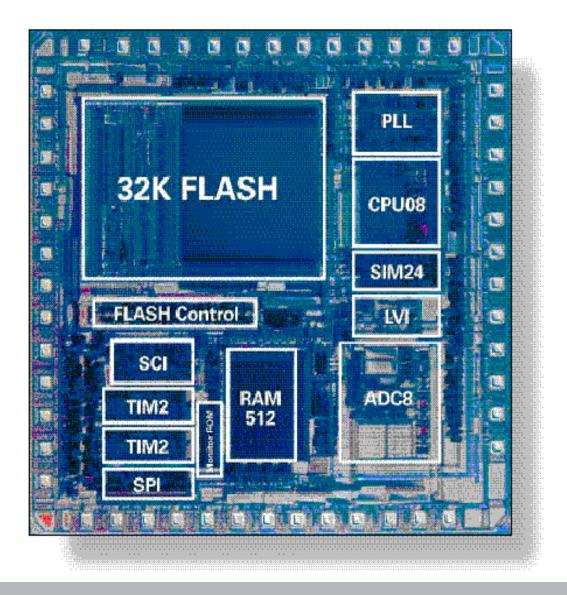
Block Diagram of a Computer System



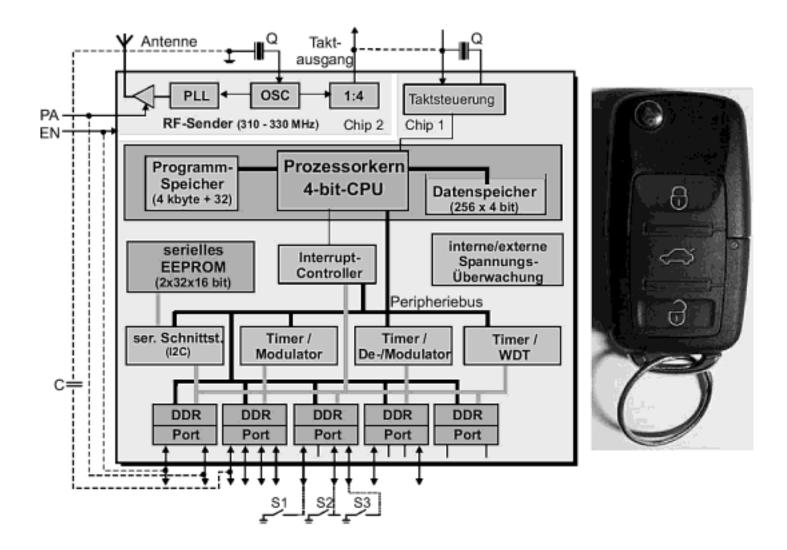
Example: Computer Motherboard



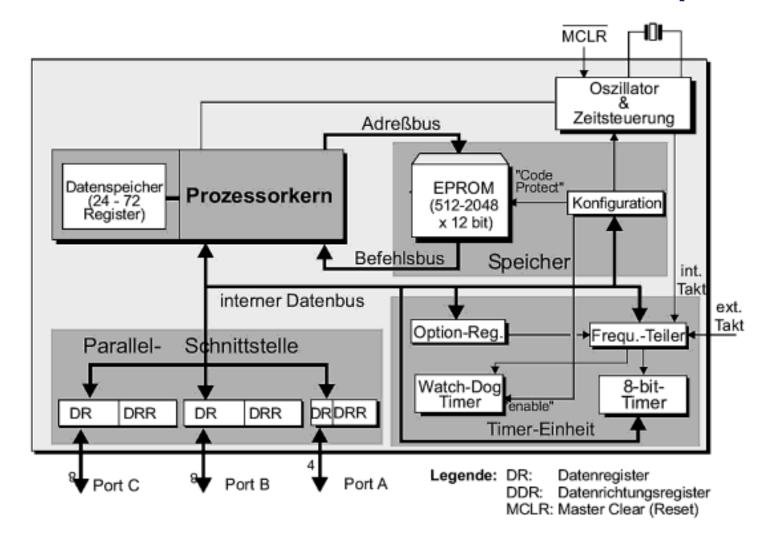
Example: MC68HC908GP32 Microcontroller (MCU)



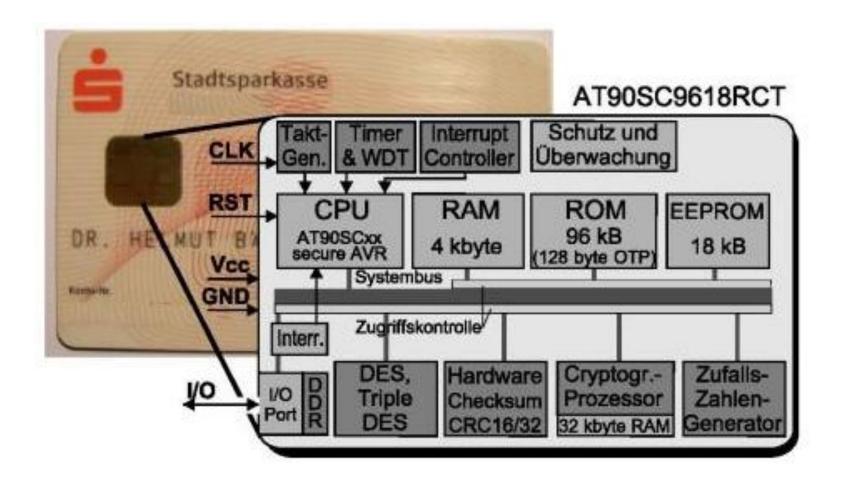
4-Bit Microcontroller ATAM862-3 from Atmel



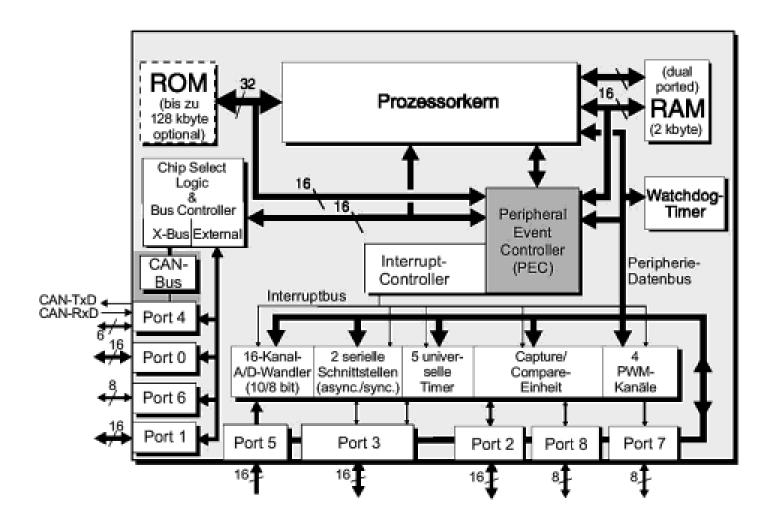
8-Bit Microcontroller PIC16C5x from Microchip



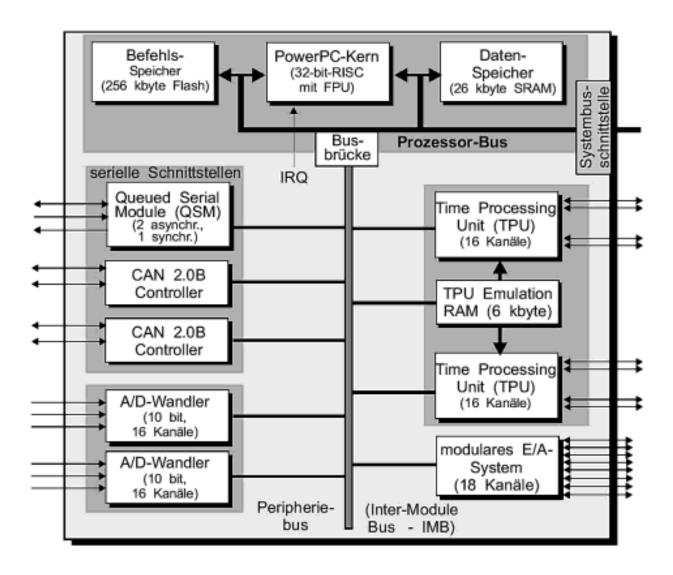
8-Bit AT90SC9618RCT secureAVR from Atmel



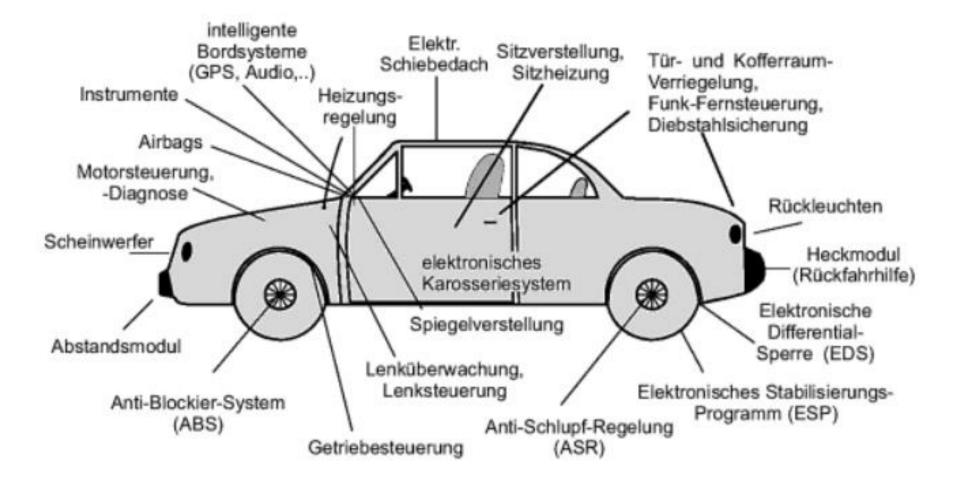
16-Bit Microcontroller C167CR from Infineon



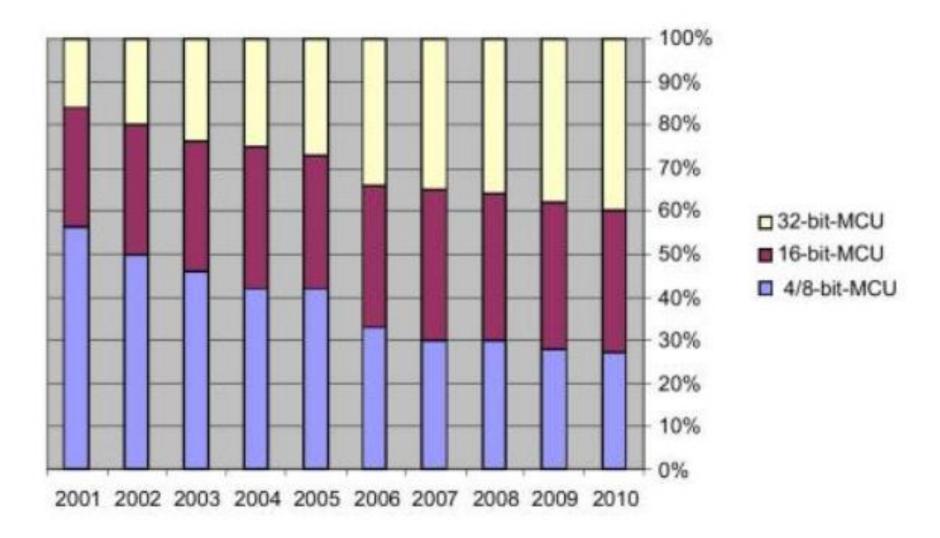
32-Bit Microcontroller MPC555 from Freescale



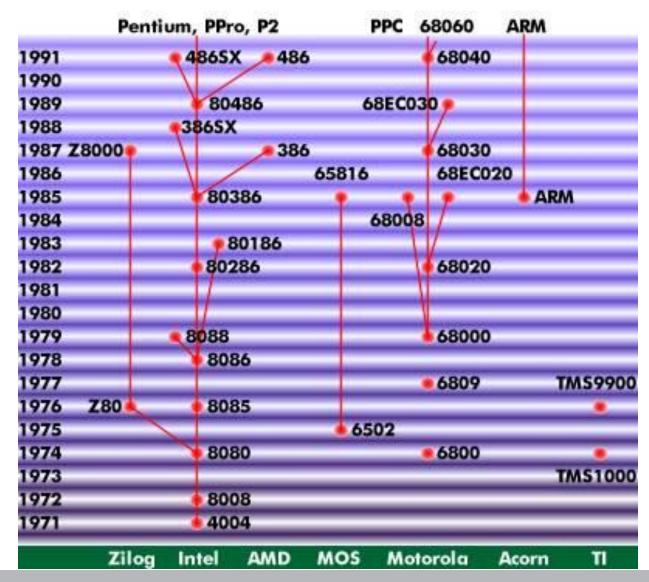
Use of Microcontrollers in a Car



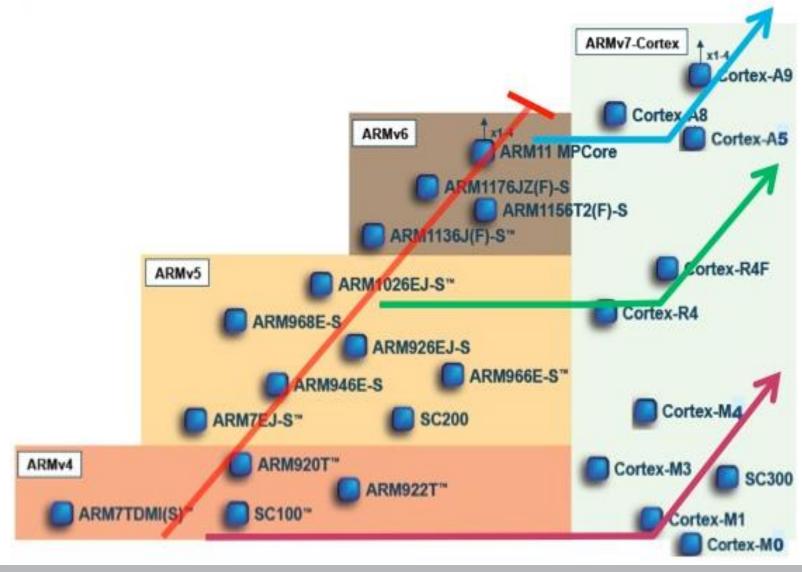
Markt Share of different Microcontrollers



Development of 32-Bit Processors



ARM Architectures



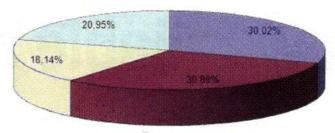
Mikrocontroller-Studie 2011:

Fast 30 % wollen zu ARM wechseln

Von Oktober bis Ende November 2011 beantworteten über 1.100 elektroniknet-Leser 19 Einzelfragen zu Mikrocontroller-Trends und Herstellerzufriedenheit. Fast 30 % der Teilnehmer, die heute noch eine herstellerspezifische Architektur einsetzen, wollen auf den Standard ARM wechseln.

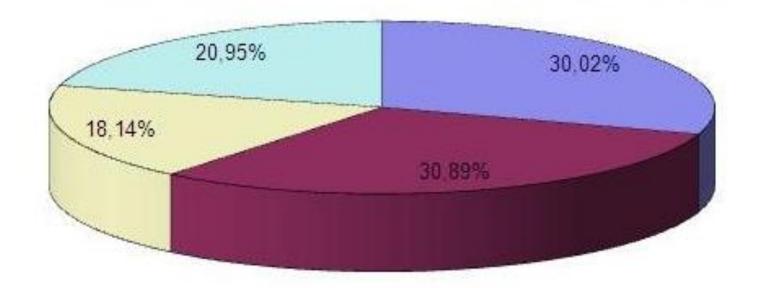
Insgesamt wurden 1.107 Fragebögen vollständig und plausibel beantwortet. 74 % der ausgewerteten Teilnehmer arbeiten als Entwickler oder Systemingenieure. Die

Warum planen Sie einen Wechsel auf eine Standardarchitektur?



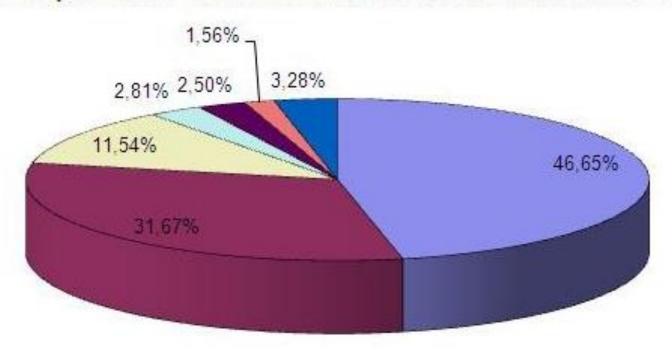
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Warum planen Sie einen Wechsel auf eine Standardarchitektur?



- ■Ich möchte herstellerunabhängiger werde als heute
- ■Die Migration von einer MCU auf eine andere wird vereinfacht
- □Ich möchte am Ecosystem von ARM partizipieren
- Es besteht eine Auf- und Abwährtskompatibilität des Cores

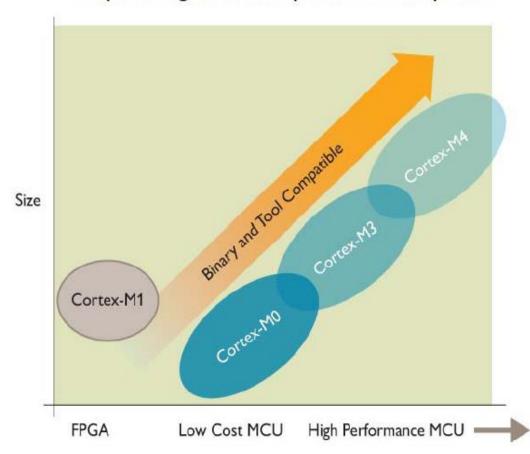
Warum planen Sie einen Wechsel von 8/16-bit- auf 32-bit-MCUs?



- Die Rechenleistung reicht nicht mehr aus
- ■Der Speicher reicht nicht mehr aus
- alch steige von Assembler auf eine Hochsprache um
- □Peripherie (z.B: TCP/IP, USB)
- ■Vereinheitlichung der Plattform (ARM)
- ■Preis-/Leistungsverhältnis
- ■Sonstige

ARM Cortex Processor Family

- Seamless embedded architecture
 - Spanning cost and performance points





ARM Cortex-A Series:

Applications processors for feature-rich OS and user applications

ARM Cortex-R Series:

Embedded processors for real-time signal processing and control applications

ARM Cortex-M Series:

Deeply embedded processors optimized for microcontroller and low-power applications

ARM Cortex-M Series

- Traditional 8/16/32-bit classification obsolete
 - Seamless architecture across all applications
 - Every product optimised for ultra low power systems

Cortex-M0 Cortex-M3 Cortex-M4

"8/16-bit" applications

"16/32-bit" applications

"32-bit/DSP" applications

Lowest cost Optimised connectivity

Performance efficiency Feature rich connectivity

SIMD/DSP Instructions Floating Point Unit (optional) High Performance MCU





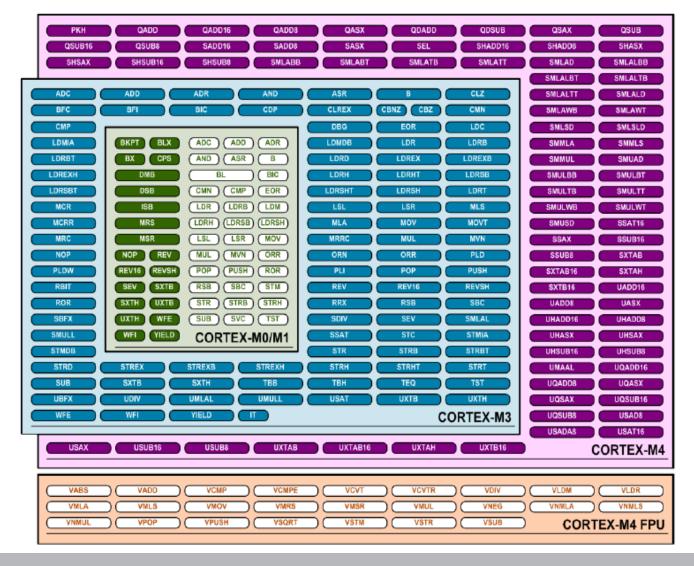




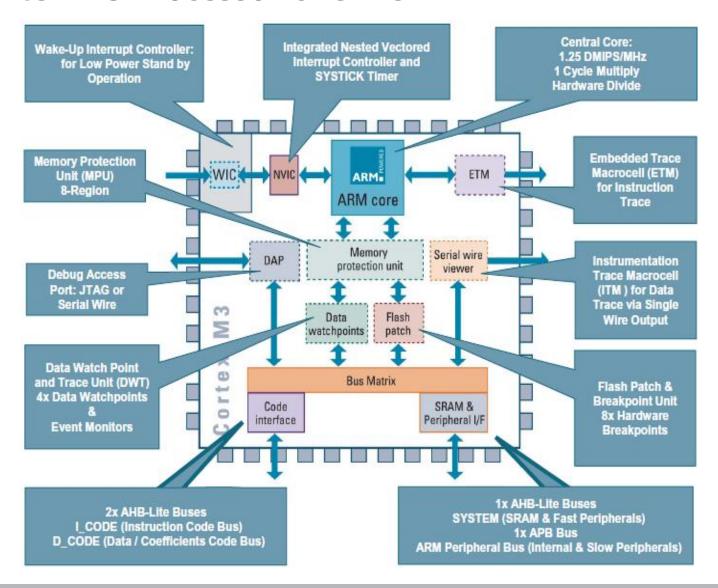




ARM Cortex-M Instruction Set



Cortex-M3 Processor Overview



Manufacturers of Microcontrollers Cortex M3/4

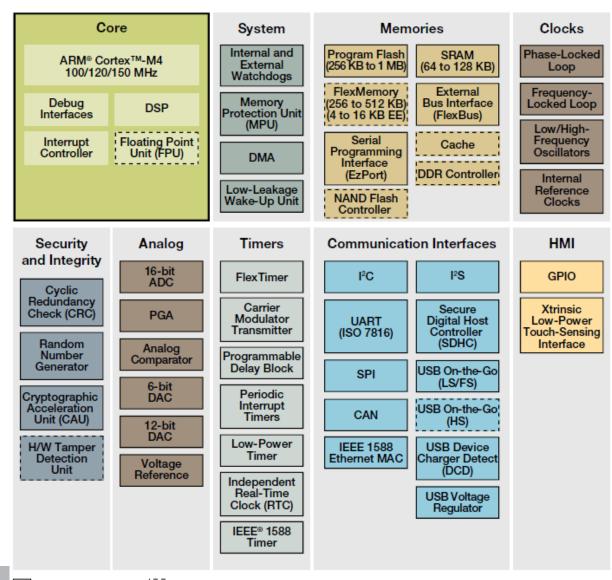
Texas Instruments
NXP (ehemals Philips)
ST Microelectronics
Infineon
Atmel
Freescale
Energy Micro
Toshiba
Analog Devices
Fujitsu

... and more!

Technology Levels

| Cortex-M3 Performance, Power & Area | | | | | | | | | | |
|-------------------------------------|-----------------|----------------|-----------------|----------------|--|--|--|--|--|--|
| Process | TSMC 18 | 30nm G | TSMC 90nm G | | | | | | | |
| Optimization Type | Speed Optimized | Area Optimized | Speed Optimized | Area Optimized | | | | | | |
| Standard Cell Library | ARM SC7 | ARM SC7 | ARM SC9 | ARM SC9 | | | | | | |
| Performance (Total DMIPS) | 125 | 75 | 340 | 75 | | | | | | |
| Frequency (MHz) | 100 | 50 | 275 | 50 | | | | | | |
| Power Efficiency (DMIPS/mW) | 3.75 | 6.25 | TBD | 12.5 | | | | | | |
| Area (mm²) | 0.37 | 0.25 | 0.083 | 0.047 | | | | | | |

Kinetis K60 Family (Freescale)



Standard Feature

MK60N512VMD10 Microcontroller

M Qualifikation Status: Production

K60 K60 Family

DN N Programm Flash

512 512 kByte

V Temperature: -40°C to 85°C

MD 144 MAPBGA Package

10 100 MHz

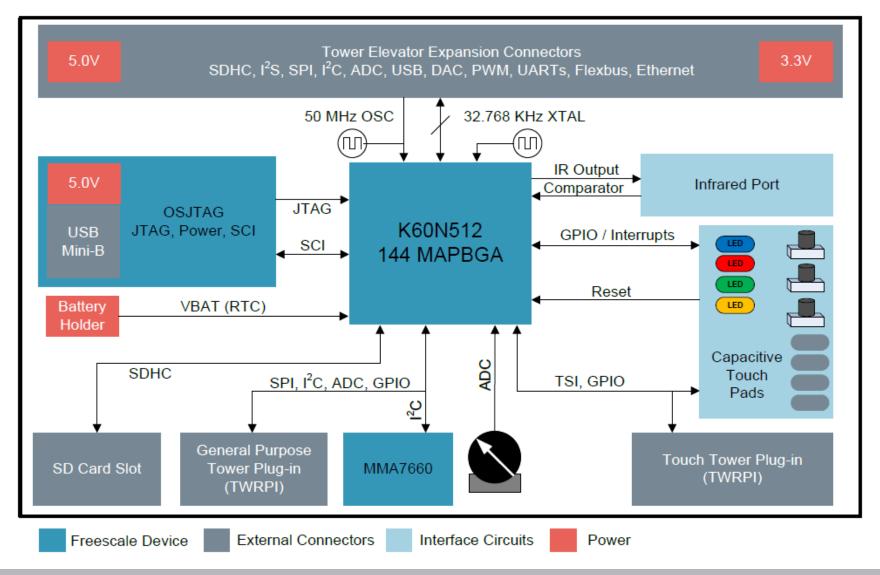
MK60N512VMD10 Microcontroller Features

- 100 MHz ARM Cortex M4 CPU with DSP
- 512 kByte Flash, 128 kByte RAM
- External Bus Interface 32-Bit
- Serial Programing Interface, JTAG Debug Interface
- 2x 16-bit A/D-Converter with up to 23 Channels
- 2x 12-bit D/A-Converter, 3x Analog Comparators
- 1x 8 Channel PWM, 2x 2 Channel PWM,
- Low Power Timer, PIT Timer, General Purpose Timer
- 2x UART with high Baud rate, 4x Standard UART
- 2x SPI, 2x I²C, 1x I²S
- 2x CAN
- 1x USB OTG Full Speed
- 1x Ethernet Interface (MII)

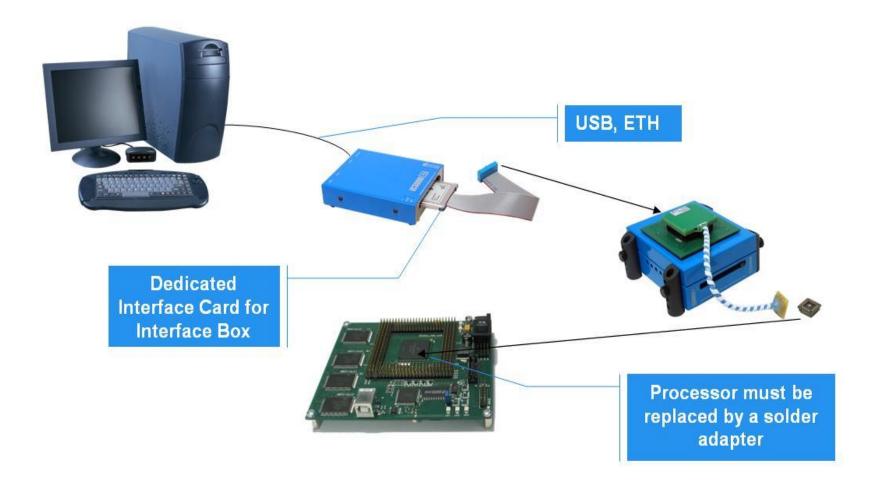
Kinetis TWR-K60N512 Module



Kinetis TWR-K60N512 Module



In-Circuit-Emulator (iSystem)



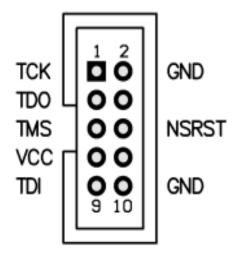
JTAG (Joint Tect Acess Group) Debugging

Debugging within the circuit (ICE) with the original CPU without any additional adapters.

- set or reset break points
- Run/Stop
- Single Step
- set or reset watch points
- Register und IO-Port view

Theoretically, the same JATG interface hardware could be user for all types of microcontrollers.

Practically, this is not possible, bacause the different MCU manufacturers implement special functions which require specific interface hardware.



JTAG Interface for Debugging (Atmel AVR)

ARM Standard JTAG Interface Pinout

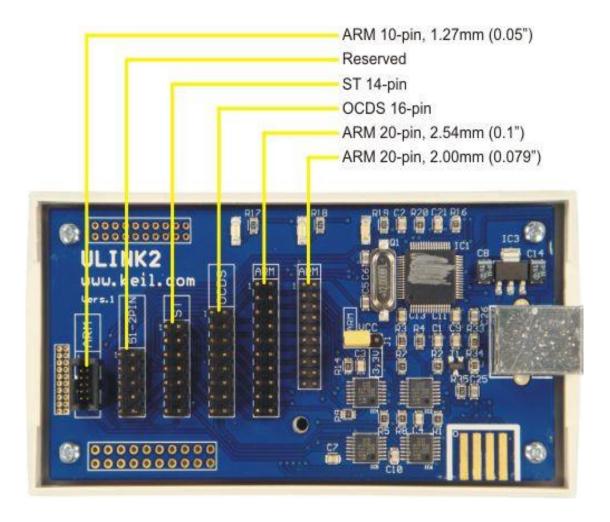
| ARM 10-Pin Connector | ST 14-Pin Connector | OCDS 16-Pin Connector | ARM 20-Pin Connector | | | |
|----------------------|-----------------------|--------------------------|--|--|--|--|
| VCC 1 2 TMS | /JEN 1 2 /TRST | TMS 1 2 VCC (optional) | VCC 1 2 VCC (optional) | | | |
| GND 3 🗌 🖂 4 TCLK | GND 3 4 N/C | TDO 3 🗌 🗎 4 GND | TRST 3 🔲 🔲 4 GND | | | |
| GND 5 🗌 🖂 6 TDO | TDI 5 🗌 🗎 6 TSTAT | CPUCLK 5 6 GND | TDI 5 6 GND | | | |
| RTCK 7 🔲 🖂 8 TDI | VCC 7 8 /RST | TDI 7 🗌 🗎 8 RESET | TMS 7 8 GND | | | |
| GND 9 🗌 🔲 10 RESET | TMS 9 🔲 🔲 10 GND | TRST 9 10 BRKOUT | TCLK 9 10 GND | | | |
| | TCLK 11 12 GND | TCLK 11 | RTCK 11 12 GND | | | |
| | TDO 13 14 /TERR | BRKIN 13 14 OCDSE | TDO 13 14 GND | | | |
| | | TRAP 15 🔲 🔲 16 GND | RESET 15 🔲 🔲 16 GND | | | |
| | | | N/C 17 🔲 🔲 18 GND | | | |
| | | | N/C 19 20 GND | | | |

Serial Wire Mode Interface

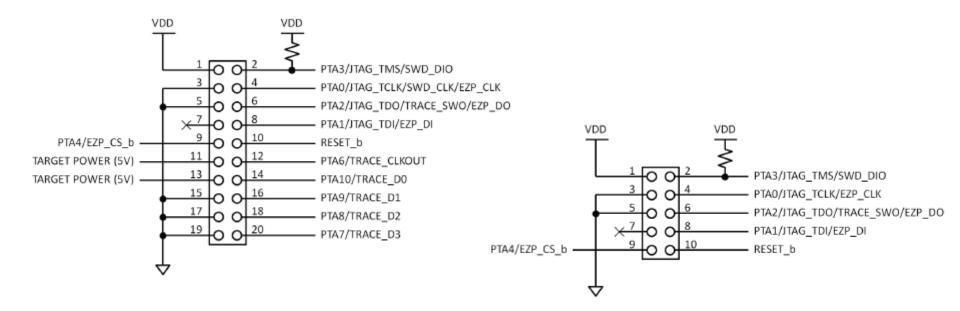
The Serial Wire (SW) mode is a different operating mode for the JTAG port where only two pins, TCLK and TMS, are used for the communication. A third pin can be use optionally to trace data. JTAG pins and SW pins are shared.

| ARM 10-Pin Connector | | | | | ARM 20-Pin Connector | | | | | | | |
|----------------------|---|--|--|----|----------------------|----|------|----|--|--|----|----------------|
| vcc | 1 | | | 2 | SWDIO | | vcc | 1 | | | 2 | VCC (optional) |
| GND | 3 | | | 4 | SWCLK | | N/U | 3 | | | 4 | GND |
| GND | 5 | | | 6 | swo | | N/U | 5 | | | 6 | GND |
| N/U | 7 | | | 8 | N/U | SI | NDIO | 7 | | | 8 | GND |
| GND | 9 | | | 10 | RESET | SW | /CLK | 9 | | | 10 | GND |
| | ١ | | | • | | | N/U | 11 | | | 12 | GND |
| | | | | | | | swo | 13 | | | 14 | GND |
| | | | | | | RI | ESET | 15 | | | 16 | GND |
| | | | | | | | N/C | 17 | | | 18 | GND |
| | | | | | | | N/C | 19 | | | 20 | GND |
| | | | | | | | | | | | | |

Keil ULINK2 Connector (typical JTAG Debugger)



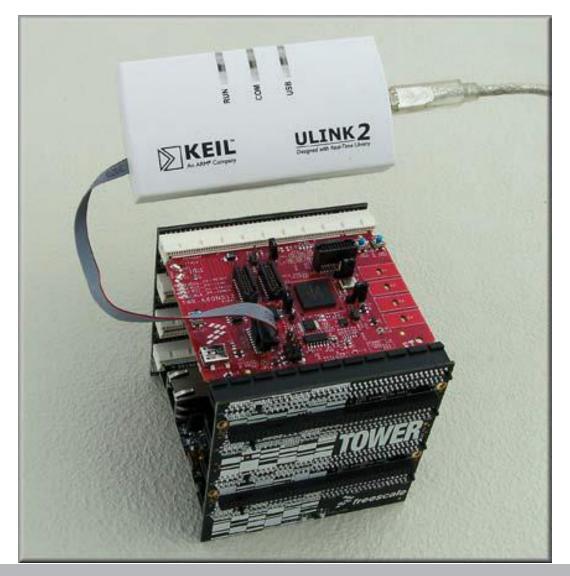
Kinetis Debug Interface



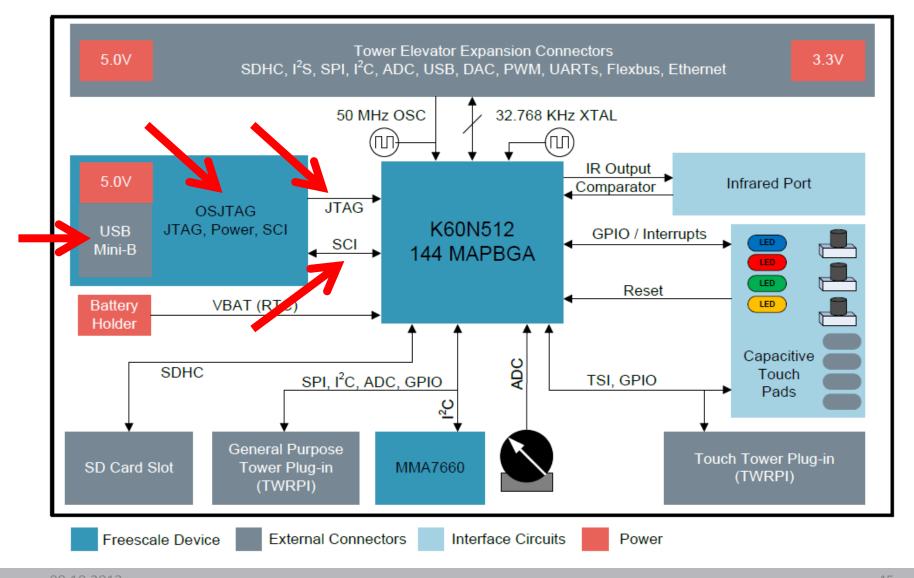
20-Pin Interface

10-Pin Interface

Keil ULINK2 Debug Interface connected to Tower System



OSJTAG Debug-Interface in the TWR-K60N512 Module



Development Environment: CodeWarrior

CodeWarrior for Microcontrollers Version 10.3

Development Environment of Freescale Semiconductor

for ColdFire®, ColdFire+, DSC, Kinetis, Qorivva, PX, RS08 and S08

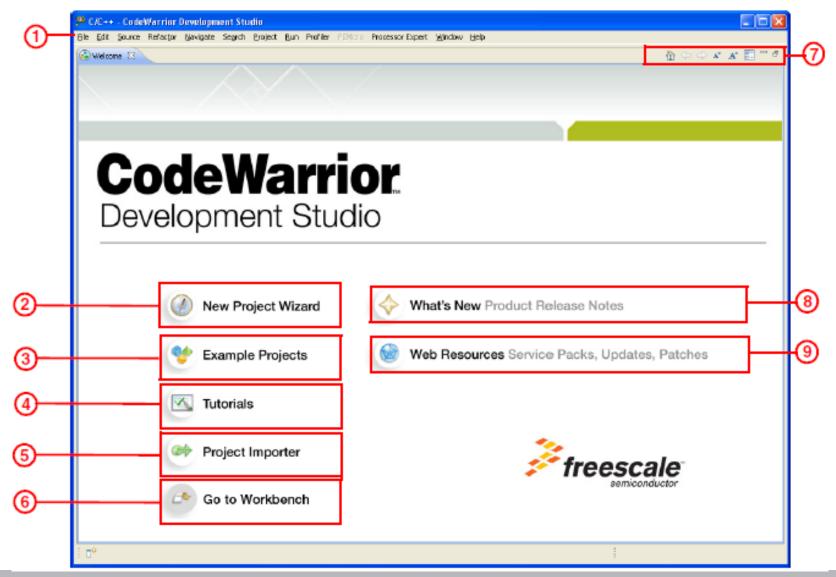
Based on Eclipse 3.6.1 User Interface

(None Real Time) Trace and profile support for S08, V1 ColdFire, ColdFire+ and Kinetis on-chip trace buffers to provide emulator-like debug capability without additional trace capture hardware (**nicht mit OSJTAG**)

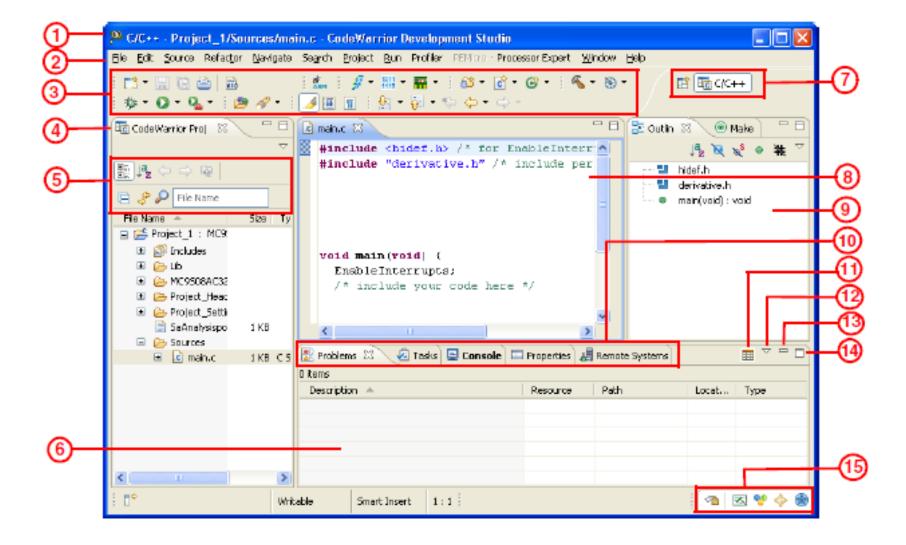
Real-time (non-intrusive) trace and profile support for V2-V4 ColdFire and Kinetis with external trace capture hardware (**nicht mit OSJTAG**)

We will use the **Special Edition** (free of charge), for Kinetis up to 128 kByte http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=CW-MCU10&tab=Design_Tools_Tab

CodeWarrior for Microcontrollers - Welcome Page



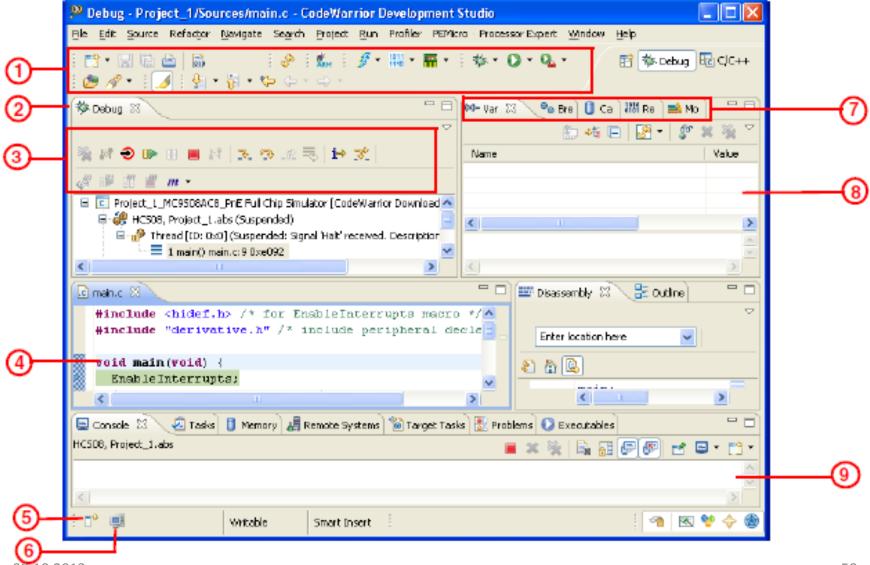
Workbench Window-C/C++ Perspective



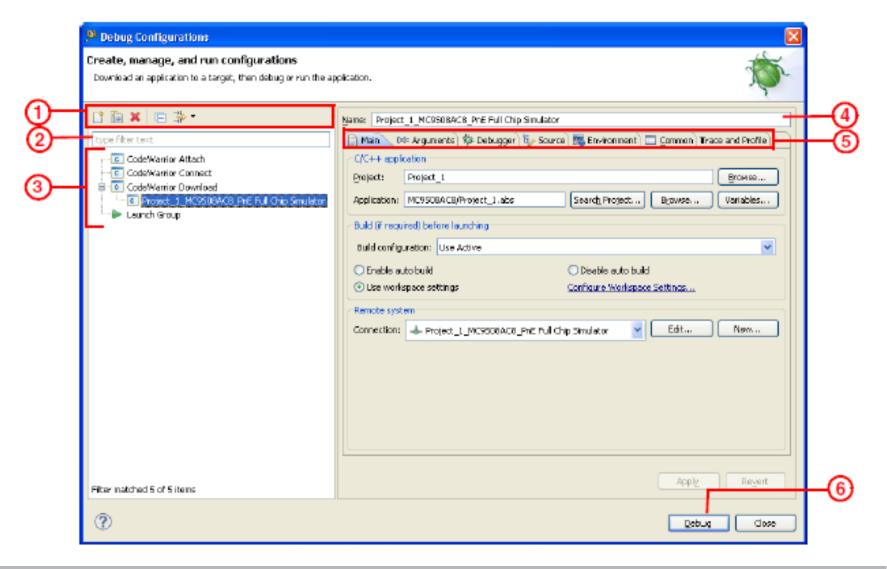
C/C++ Perspective: Editor Area

```
*msc8144_main.c 🛭 🗎 *startup.asm
            3277, 328, 98<mark>30, 4915, -3276, -9829, 8192, -6553, -655</mark>
   Word16 DataOut[DataBlockSize];
   int func1();
   int func1()
   #pragma noinline
       Word16 YNM1=0, YNM2=0;
       Word32 TN, TNP1, YN, YNP1;
        int i:
       for (i = 0; i < DataBlockSize/2; i++) {      /* do all samp</pre>
         TN = L deposit h(DataIn[2*i]);
          TNP1 = L deposit h(DataIn[2*i+1]);
          TN = L mac(TN, YNM2,a2);
                                      YN = L mult(YNM2,b2);
         TN = L mac(TN, YNN1,a1);
                                         YN = L mac(YN, YNM1, b1);
          YN as is L add(YN,TN)
                                           YNM2 = round(TN);
          TNP1 = L mac(TNP1, YNM1,a2); YNP1 = L mult(YNM1,b2);
         TNP1 = L mac(TNP1, round(TN),a1); YNP1 = L mac(YNP1,YNM
         YNP1 = L add(YNP1,TNP1); YNM1 = round(TNP1);
```

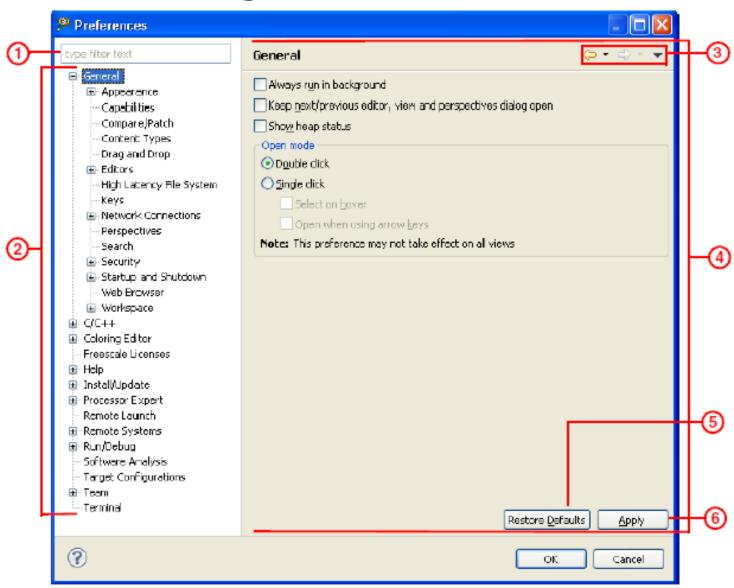
Workbench Window—Debug Perspective



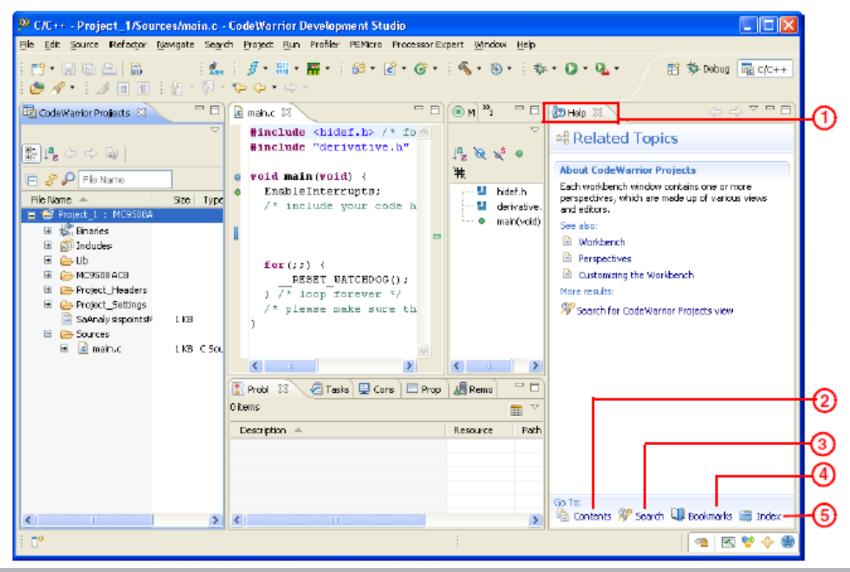
Debug Configurations Dialog Box



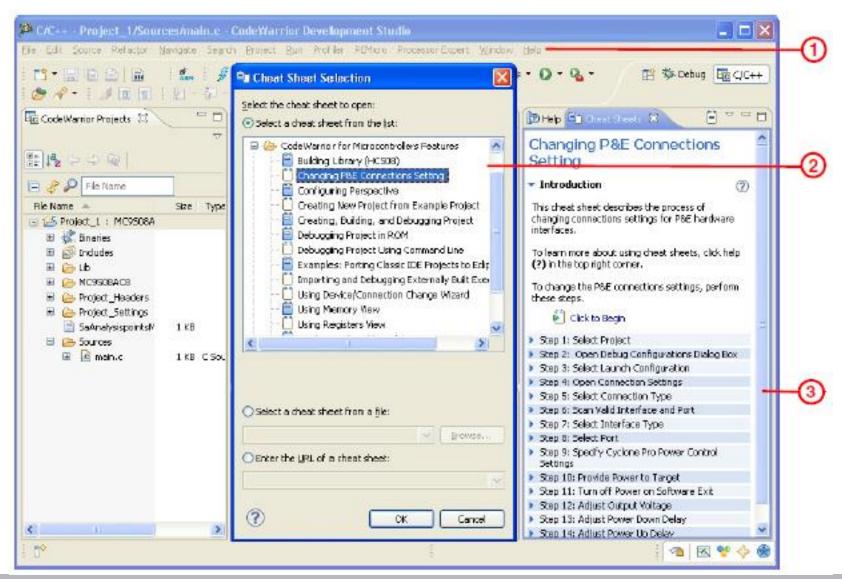
Preferences Dialog Box



Help View



Cheat Sheets



Other Tools: Segger J-Trace ARM

- Trace supports up to 200 MHz full and 100 MHz half clock rate
- Trace based on ARM ETM (Embedded Trace Macrocell)
- Trace support for devices with built-in trace ports
- 2 Mbyte trace memory buffer

enables "Trace and Profile" in Real Time



TECHNISCHE HOCHSCHULE DEGGENDORF

Technische Hochschule Deggendorf – Edlmairstr. 6 und 8 – 94469 Deggendorf