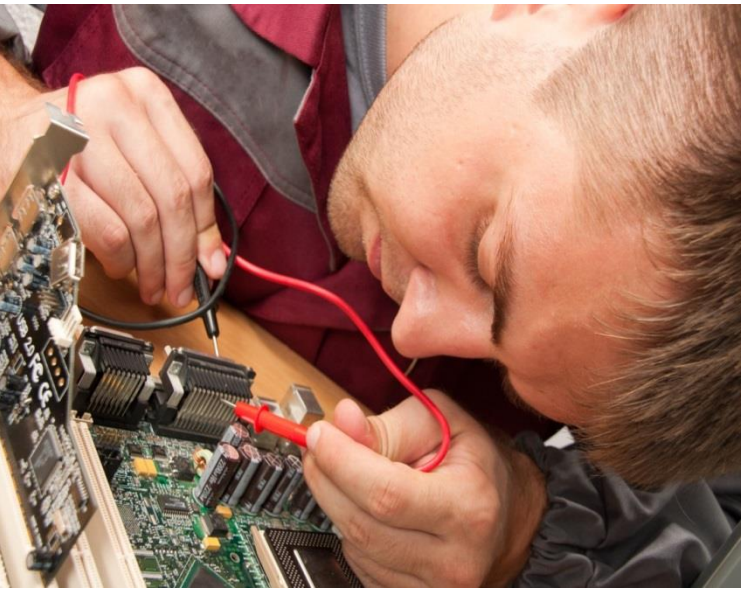
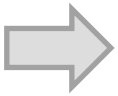
TECHNISCHE HOCHSCHULE DEGGENDORF



Microcontroller Programming (4)

Gerald Kupris, 29.10.2013

Lectures Microcontroller Programming WS2013/14



08.10.2013 Microcontroller, Programming and Debuging Interfaces
15.10.2013 Reading and Writing of Registers
22.10.2013 I/O-Pins, Reading and Writing of Single Bits
29.10.2013 Clock Generation, CPU und Computing Power
05.11.2013 Interrupts
12.11.2013 No lecture !
19.11.2013 Memory
26.11.2013 Timer and PWM, Watchdog Timer
03.12.2013 Analog to Digital Converter
10.12.2013 Serial Interfaces: SPI, IIC and UART
17.12.2013 Additional Explanation of the Freescale Cup Cars
14.01.2014 Project Work on the Freescale Cup Cars
21.01.2014 Project Work on the Freescale Cup Cars

Hands-On Workshops Microcontroller Programming

08.10.2013 Workshop 1: Preparation of the Work Place
15.10.2013 Workshop 2: Loading and Debugging of Programs
22.10.2013 Workshop 3: Using the GPIO Pins
29.10.2013 Workshop 4: Clock Generation and Calculations
05.11.2013 Workshop 5: Interrupts
12.11.2013 No Workshop !
19.11.2013 Workshop 6: Using the Flash Memory
26.11.2013 Workshop 7: Timer and Pulse Width Modulation (PWM)
03.12.2013 Workshop 8: Analog to Digital Conversion
10.12.2013 Workshop 9: Serial Communication
17.12.2013 Project work on the Freescale Cup Cars
14.01.2014 Project work on the Freescale Cup Cars
21.01.2014 Project work on the Freescale Cup Cars

Participation on all workshops is required for admittance to the final project!

Start Time Tuesday: 15:45 p.m.
New Start Time Thursday: 14:45 p.m.

Attention: No Workshop on the 07.11.2013!

Block 1: 08:00 - 09:30
Block 2: 09:45 - 11:15
Block 3: 12:00 - 13:30

3. Semester Bachelor AI (Stand: 12.09.2013)

07.11.2013

Block 4: 14:00 - 15:30
Block 5: 15:45 - 17:15
Block 6: 17:30 - 19:00

	Montag	Dienstag	Mittwoch	Donnerstag	Freitag
1	Vertiefte Elektrotechnik Bö D 113	Digitaltechnik Bö E 101	SW-Engineering gem. mit MT 5 Jr ITC1-E 104	Messtechnik (bis Mitte Nov) Wu E 101	Einführung GIS LB Zink E 101
2	Messtechnik (ab Mitte Nov) Bö D 113	Digitaltechnik Praktikum Gruppe 1/2 (14-tägig) LabIng	SW-Engineering gem. mit MT 5 Jr ITC1-E 104	Bezugssysteme und Positionierung LB Reidelstürz ITC1-E 104 Messtechnik (bis Mitte Nov) Wu E 101	Einführung GIS LB Zink E 101
3	Messtechnik (ab Mitte Nov) Bö A 210	Digitaltechnik Praktikum Gruppe 1/2 (14-tägig) LabIng	SW-Engineering gem. mit MT 5 Jr ITC1-E 103	Bezugssysteme und Positionierung LB Reidelstürz ITC1-E 104	Grundlagen der Raumwissenschaften LB Reidelstürz /Zink E 101
4	AWP	Mikrorechnertechnik Vorlesung Ku ITC1-E 104	AWP	Mobile Betriebssysteme Do ITC2-Geoinformatiklab.	Vertiefte Elektrotechnik Praktikum Ku ITC1-E 103 Grundlagen der Raumwissenschaften LB Reidelstürz / Zink E 101
5	AWP	Mikrorechnertechnik Praktikum Ku ITC1-E 104	AWP	Mobile Betriebssysteme Do ITC2-Geoinformatiklab.	

Attention: No Lecture on the 12.11.2013!

Block 1: 08:00 - 09:30
Block 2: 09:45 - 11:15
Block 3: 12:00 - 13:30

3. Semester Bachelor AI (Stand: 12.09.2013)

12.11.2013

Block 4: 14:00 - 15:30
Block 5: 15:45 - 17:15
Block 6: 17:30 - 19:00

	Montag	Dienstag	Mittwoch	Donnerstag	Freitag
1	Vertiefte Elektrotechnik Bö D 113	Digitaltechnik Bö E 101	SW-Engineering gem. mit MT 5 Jr ITC1-E 104	Messtechnik (bis Mitte Nov) Wu E 101	Einführung GIS LB Zink E 101
2	Messtechnik (ab Mitte Nov) Bö D 113	Digitaltechnik Praktikum Gruppe 1/2 (14-tägig) LabIng	SW-Engineering gem. mit MT 5 Jr ITC1-E 104	Bezugssysteme und Positionierung LB Reidelstürz ITC1-E 104 Messtechnik (bis Mitte Nov) Wu E 101	Einführung GIS LB Zink E 101
3	Messtechnik (ab Mitte Nov) Bö A 210	Digitaltechnik Praktikum Gruppe 1/2 (14-tägig) LabIng	SW-Engineering gem. mit MT 5 Jr ITC1-E 103	Bezugssysteme und Positionierung LB Reidelstürz ITC1-E 104	Grundlagen der Raumwissenschaften LB Reidelstürz /Zink E 101
4	AWP	Mikrorechnertechnik Vorlesung Ku ITC1-E 104	AWP	Mobile Betriebssysteme Do ITC2-Geoinformatik lab. Vertiefte Elektrotechnik Praktikum Ku ITC1-E 103	Grundlagen der Raumwissenschaften LB Reidelstürz / Zink E 101
5	AWP	Mikrorechnertechnik Praktikum Ku ITC1-E 104	AWP	Mobile Betriebssysteme Do ITC2-Geoinformatik lab.	

Recall: Bitwise Operations

AND: "&" (not the same as "&&")

OR: "|" (not the same as "||")

NOT: "~" (not the same as "!")

XOR: "^"

LEFT SHIFT: "<< *n*"

RIGHT SHIFT*: ">> *n*"

*Note: Compiler decides what happens to uppermost bit for signed data!

Recall: Bit Mask Examples

Testing bits

```
if (pTimer->control & TIMER_COMPLETE) { }
```

Setting bits

```
pTimer->control |= TIMER_INTERRUPT;
```

Clearing bits

```
pTimer->control &= ~TIMER_INTERRUPT;
```

Toggling bits

```
pTimer->control ^= TIMER_PERIODIC;
```

Recall: Using the I/O Pins

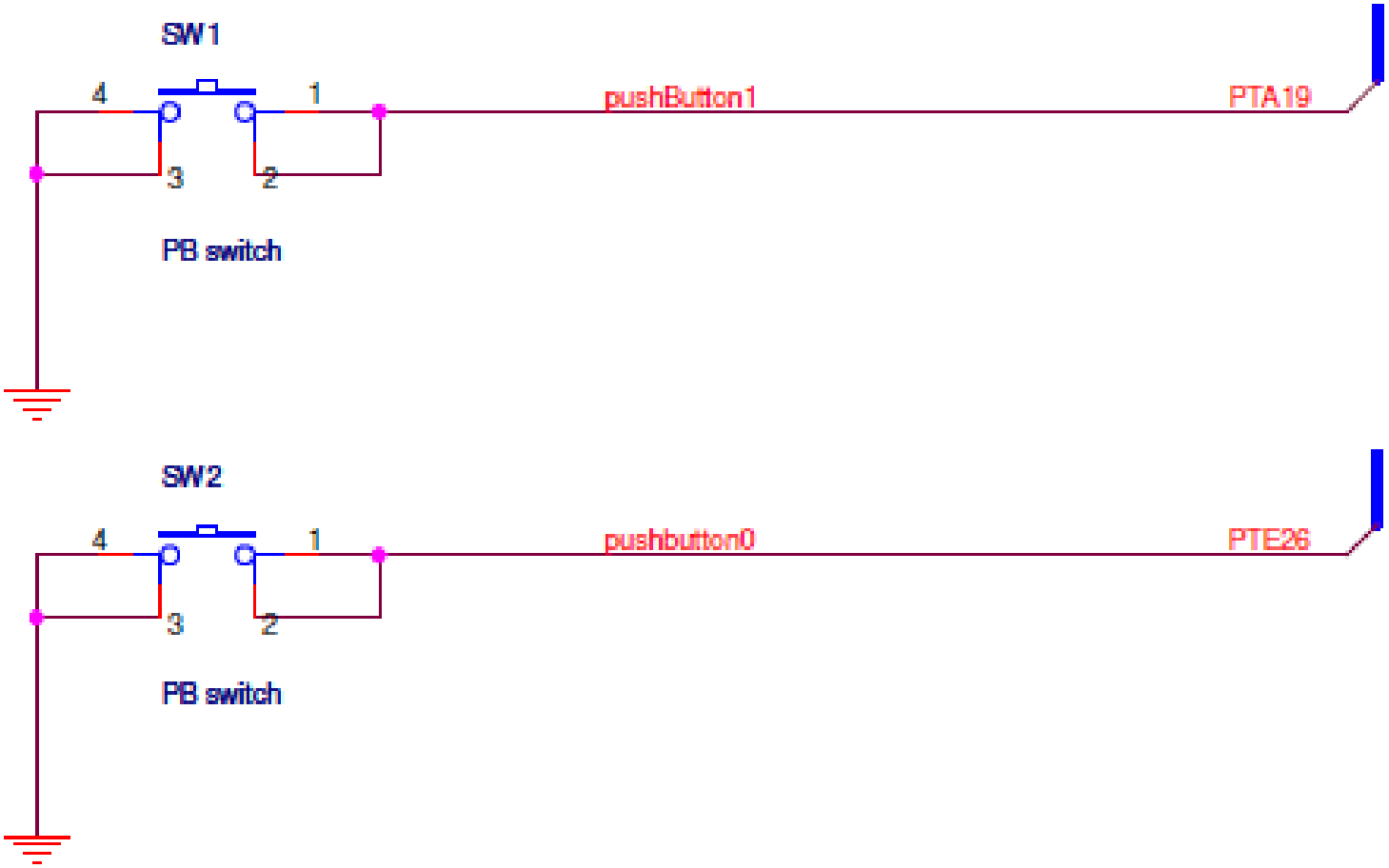
The configuration of the I/O pins takes place place in most cases at the very beginning of the program, directly after the reset of the microcontroller (so called initialization):

1) Step 1: Enable clock of the I/O pins
2) Step 2: Define pin function as a GPIO
3) Step 3: Define the direction of the GPIO (input or output)
4) Step 4: Set additional options (Pull-Up, Pull-Down, Open Drain ...)
5) Step 5: Set interrupt options

Then, the I/O pin can be used during the program itself:

1) Set the output value (0 or 1) or
2) Read the input value (0 or 1) or
3) Use the Interrupts

Recall: I/O Pins as Inputs



SW1: Port Pin PTA19
SW2: Port Pin PTE26

Recall: Configuration of the I/O-Pins as Input

```
// Set PTA 19 and PTE26 for GPIO functionality
    PORTA_PCR19 = (0|PORT_PCR_MUX(1));
    PORTE_PCR26 = (0|PORT_PCR_MUX(1));
```

```
// Set PTA19 and PTE26 to inputs
    GPIOA_PDDR &= ~GPIO_PDDR_PDD(GPIO_PIN(19));
    GPIOE_PDDR &= ~GPIO_PDDR_PDD(GPIO_PIN(26));
```

54.2.6 Port Data Direction Register (GPIOx_PDDR)

The PDDR configures the individual port pins for input or output.

Addresses: GPIOA_PDDR is 400F_F000h base + 14h offset = 400F_F014h
GPIOB_PDDR is 400F_F040h base + 14h offset = 400F_F054h
GPIOC_PDDR is 400F_F080h base + 14h offset = 400F_F094h
GPIOD_PDDR is 400F_F0C0h base + 14h offset = 400F_F0D4h
GPIOE_PDDR is 400F_F100h base + 14h offset = 400F_F114h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PDD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Recall: Using the I/O Pin as Input

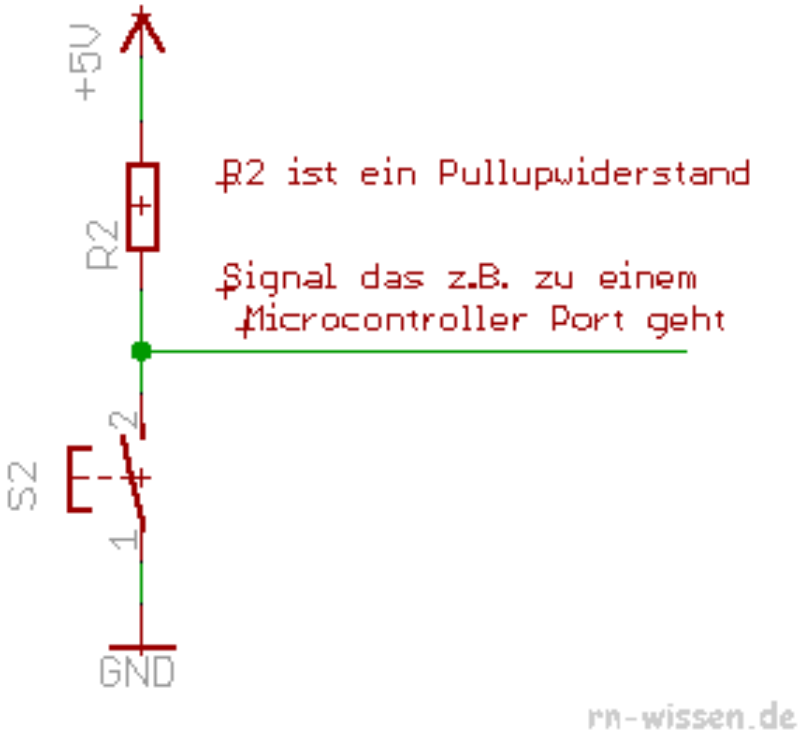
```
if (!(GPIOA_PDIR & (GPIO_PIN(19))))    // bit 19 not set
                                        // button SW1 on
{
        ....
}
```

54.2.5 Port Data Input Register (GPIOx_PDIR)

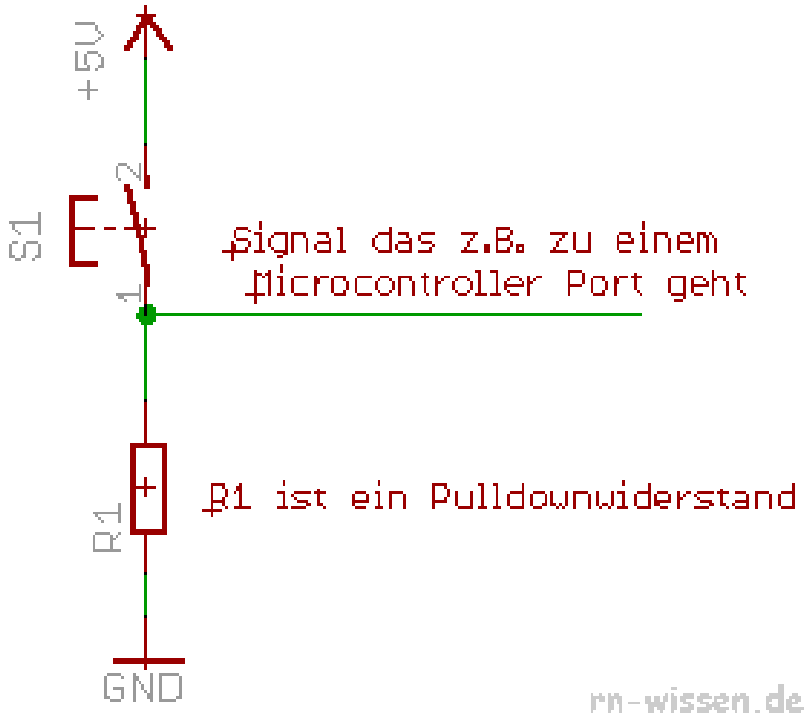
Addresses: GPIOA_PDIR is 400F_F000h base + 10h offset = 400F_F010h
GPIOB_PDIR is 400F_F040h base + 10h offset = 400F_F050h
GPIOC_PDIR is 400F_F080h base + 10h offset = 400F_F090h
GPIOD_PDIR is 400F_F0C0h base + 10h offset = 400F_F0D0h
GPIOE_PDIR is 400F_F100h base + 10h offset = 400F_F110h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PDI																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Recall: Input Options of the I/O Pins



Pull-Up Resistor



Pull-Down Resistor

Recall: Additional Options: Pin Control Register

11.4.1 Pin Control Register n (PORTx_PCR*n*)

For PCR1 to PCR5 of the port A, bit 0, 1, 6, 8, 9,10 reset to 1; for the PCR0 of the port A, bit 1, 6, 8, 9, 10 reset to 1; in other conditions, all bits reset to 0.

Addresses: 4004_9000h base + 0h offset + (4d × *n*), where *n* = 0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							ISF	0				IRQC				LK	0				MUX			0	DSE	ODE	PFE	0	SRE	PE	PS
W								w1c																								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

If the pin is an input:

Interrupt / DMA Request

Passive Filter Enable

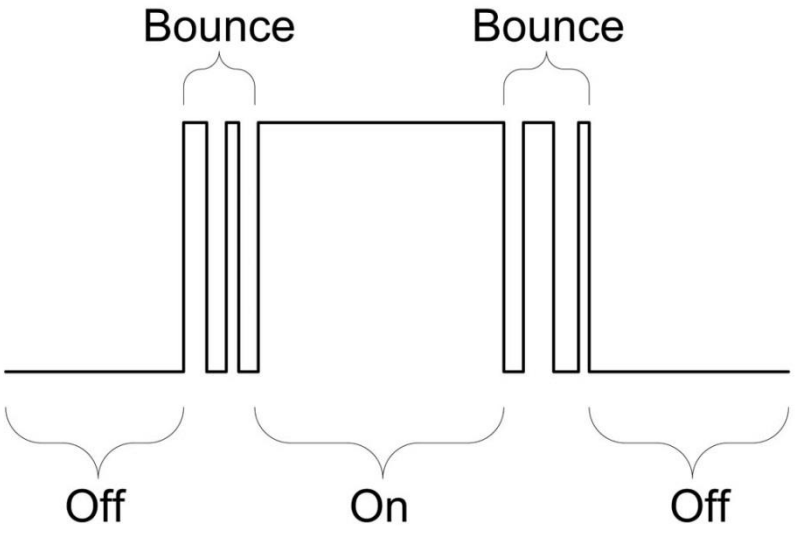
Pull Enable

Pull Select

Recall: Debouncing of contacts

Bouncing is the tendency of any two metal contacts in an electronic device to generate multiple signals as the contacts close or open; debouncing is any kind of hardware device or software that ensures that only a single signal will be acted upon for a single opening or closing of a contact.

When you press a key on your keyboard , you expect a single contact to be recorded by your computer. In fact, however, there is an initial contact, a slight bounce or lightening up of the contact, then another contact as the bounce ends, yet another bounce back, and so forth.



A similar effect takes place when a switch made using a metal contact is opened. The usual solution is a debouncing device or software that ensures that only one digital signal can be registered within the space of a given time (usually milliseconds).

Clock Generation

A microcontroller requires a lot of different clock options like:

- **external crystal with high frequency**
  to create a clock for the CPU and the communication interfaces

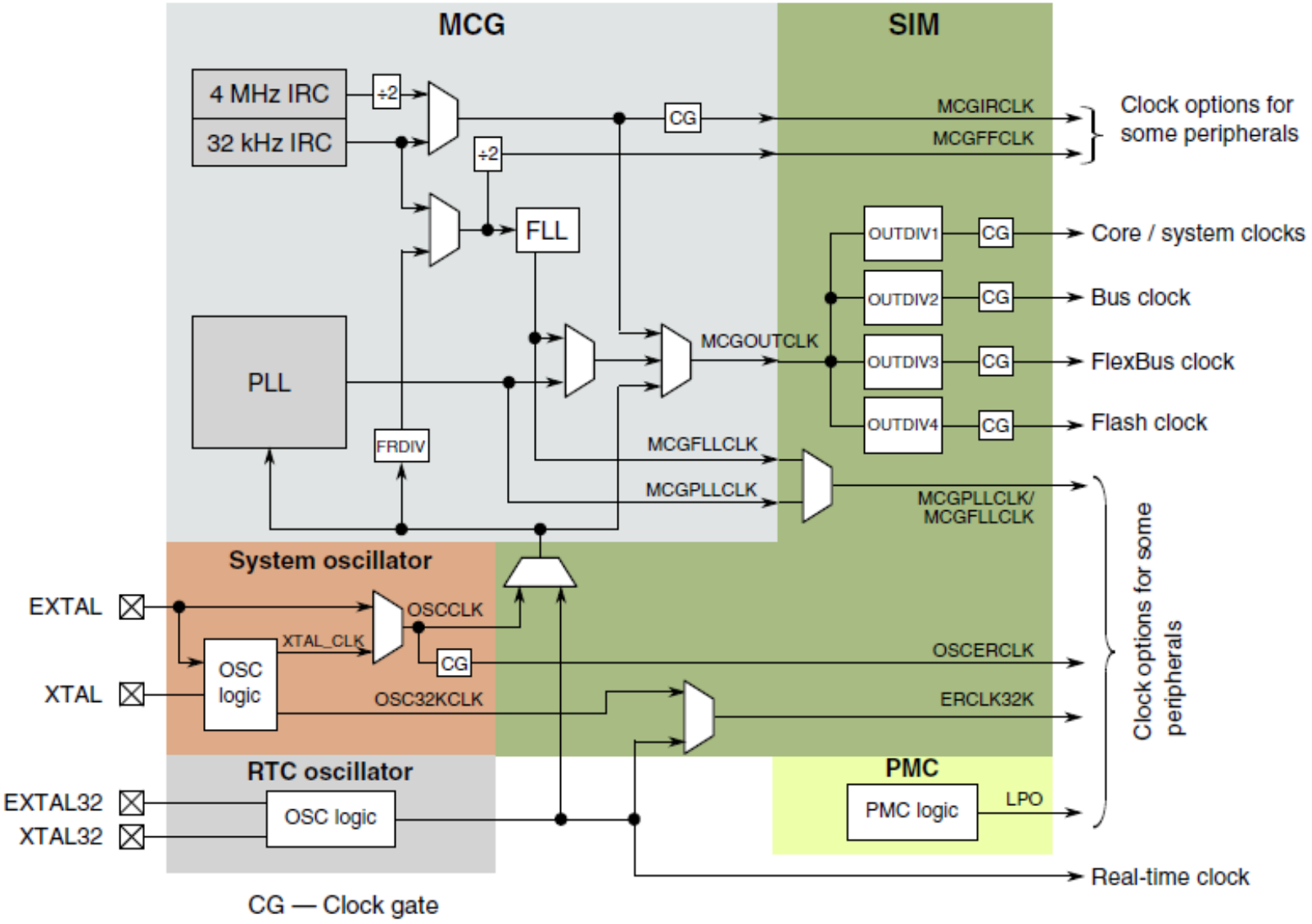
- **external crystal with low frequency**
  is often used to drive a real time clock, should be low power

- **external oscillator**
  to create additional alternative clock options

- **external RC oscillator**
  clock with external RC combinantion, not precise, fast start-up

- **internal RC oscillator**
  clock generation without any external components (low cost)

Clock Generation at the Kinetis K60



Most Important Frequencies of the MK60N512VMD10

Clock name		Description
Core clock	Up to 100 MHz	MCGOUTCLK divided by OUTDIV1 clocks the ARM Cortex-M4 core
System clock	Up to 100 MHz	MCGOUTCLK divided by OUTDIV1 clocks the crossbar switch and bus masters directly connected to the crossbar. In addition, this clock is used for UART0 and UART1.
Bus clock	Up to 50 MHz	MCGOUTCLK divided by OUTDIV2 clocks the bus slaves and peripheral (excluding memories)
FlexBus clock	Up to 50 MHz	MCGOUTCLK divided by OUTDIV3 clocks the external FlexBus interface
Flash clock	Up to 25 MHz	MCGOUTCLK divided by OUTDIV4 clocks the flash memory

OSCCLK	System oscillator output of the internal oscillator or sourced directly from EXTAL
OSCERCLK	System oscillator output sourced from OSCCLKthat may clock some on-chip modules
OSC32KCLK	System oscillator 32kHz output
ERCLK32K	Clock source for some modules that is chosen as OSC32KCLK or the RTC clock
RTC clock	RTC oscillator output for the RTC module
LPO	PMC 1kHz output

Modules for Clock Generation

Module	Description
Multi-clock generator (MCG)	The MCG provides several clock sources for the MCU that include: • Phase-locked loop (PLL) — Voltage-controlled oscillator (VCO) • Frequency-locked loop (FLL) — Digitally-controlled oscillator (DCO) • Internal reference clocks — Can be used as a clock source for other on-chip peripherals
System oscillator	The system oscillator, in conjunction with an external crystal or resonator, generates a reference clock for the MCU.
Real-time clock oscillator	The RTC oscillator has an independent power supply and supports a 32 kHz crystal oscillator to feed the RTC clock. Optionally, the RTC oscillator can replace the system oscillator as the main oscillator source.

Table 10-7. OSC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL0	EXTAL	External clock/Oscillator input	I
XTAL0	XTAL	Oscillator output	O

Table 10-8. RTC OSC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

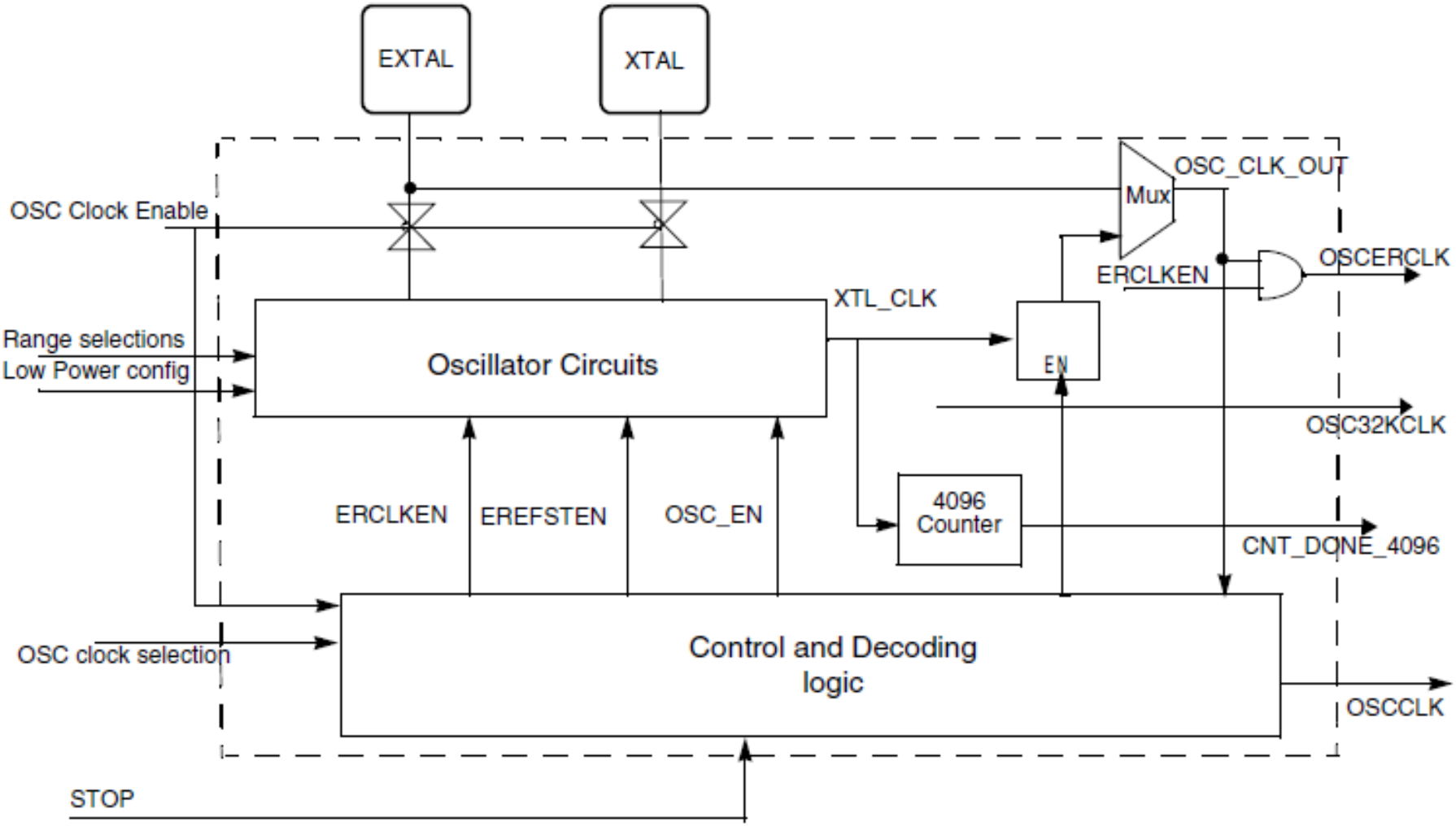
System Oscillator (OSC)

The OSC module is a crystal oscillator. The module, in conjunction with an external crystal or resonator, generates a reference clock for the MCU.

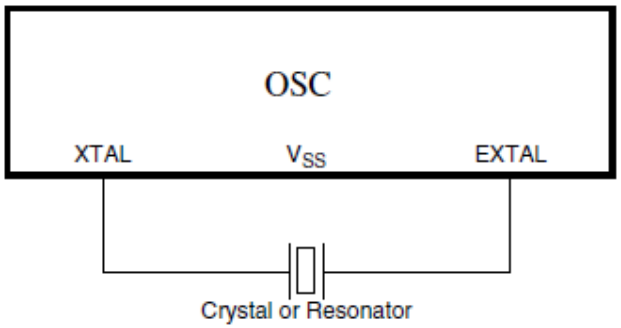
Key features of the module are:

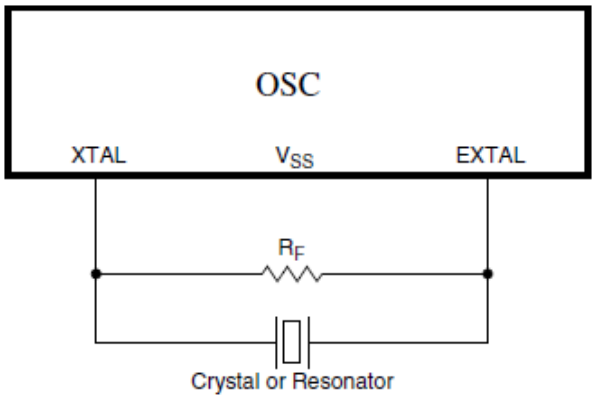
- Supports 32 kHz crystals (Low Range mode)
- Supports 3–8 MHz, 8–32 MHz crystals and resonators (High Range mode)
- Automatic Gain Control (AGC) to optimize power consumption in high frequency ranges 3–8 MHz, 8–32 MHz using low-power mode
- High gain option in frequency ranges: 32 kHz, 3–8 MHz, and 8–32 MHz
- Voltage and frequency filtering to guarantee clock frequency and stability
- Optionally external input bypass clock from EXTAL signal directly
- One clock for MCU clock system
- Two clocks for on-chip peripherals that can work in Stop modes

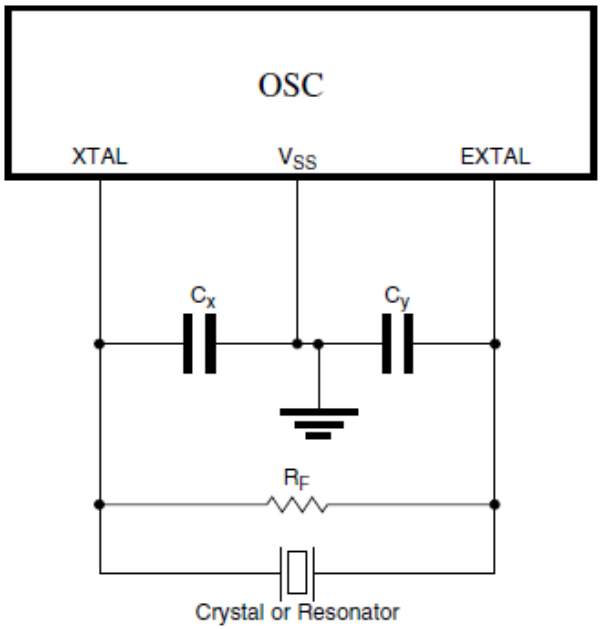
System Oscillator Block Diagram



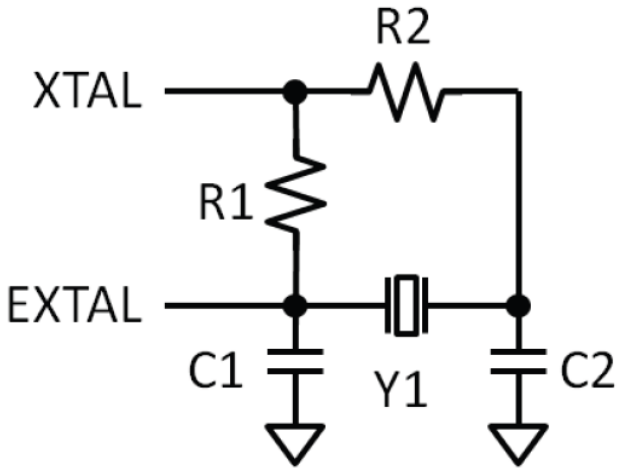
Connection Options of External Crystals

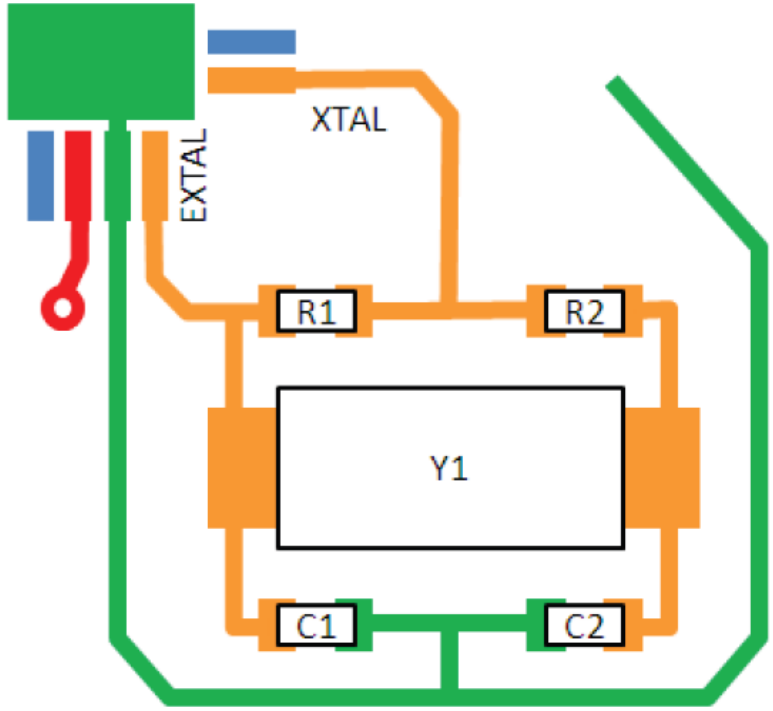




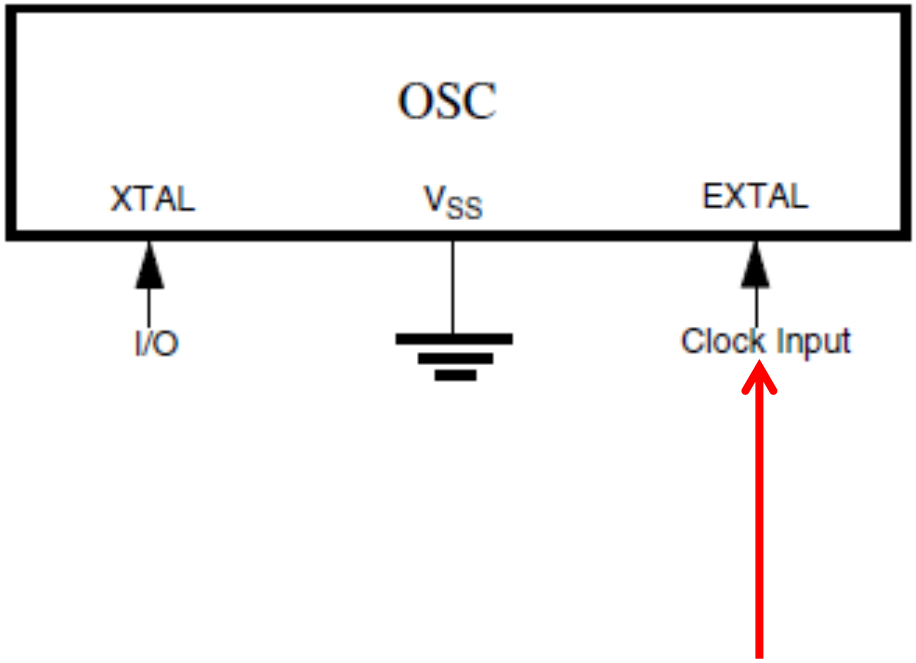


Crystal Oscillator with Layout Recomandation





Input of an External Clock



OSC Control Register (OSC_CR)

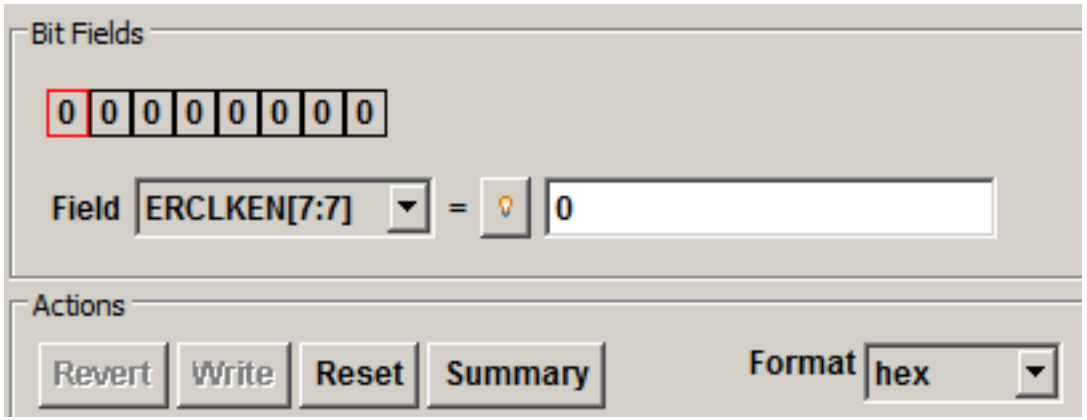
25.71.1 OSC Control Register (OSC_CR)

After OSC is enabled and starts generating the clocks, the configurations such as low power and frequency range, must not be changed.

Address: OSC_CR is 4006_5000h base + 0h offset = 4006_5000h

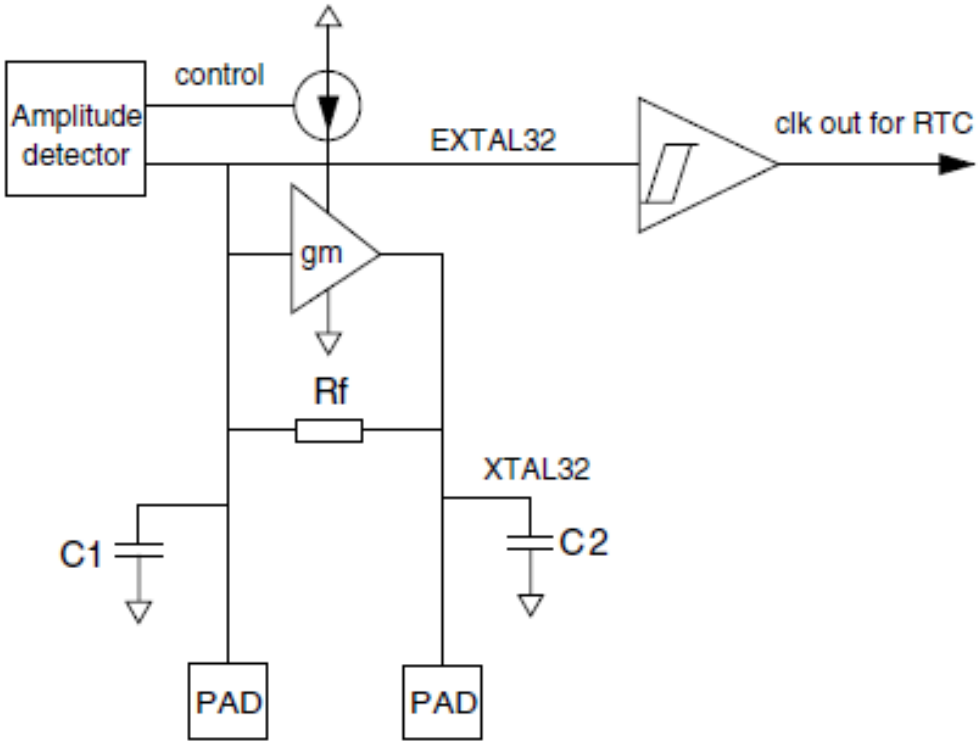
Bit	7	6	5	4	3	2	1	0
Read	ERCLKEN	0	EREFSTEN	0	SC2P	SC4P	SC8P	SC16P
Write								
Reset	0	0	0	0	0	0	0	0

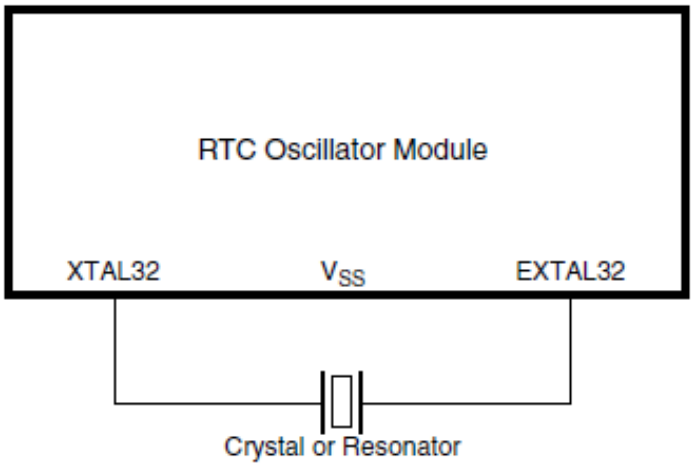
0 External reference clock is inactive.
1 External reference clock is enabled.



RTC Oscillator

The RTC (Real Time Clock) is an independend clock, which can be driven from a separate battery. In current saving mode it runs independently from the main power. The RTC is clocked from a 32.768 kHz crystal.





RTC Register

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value
4003_D000	RTC Time Seconds Register (RTC_TSR)	32	R/W	0000_0000h
4003_D004	RTC Time Prescaler Register (RTC_TPR)	32	R/W	0000_0000h
4003_D008	RTC Time Alarm Register (RTC_TAR)	32	R/W	0000_0000h
4003_D00C	RTC Time Compensation Register (RTC_TCR)	32	R/W	0000_0000h
4003_D010	RTC Control Register (RTC_CR)	32	R/W	0000_0000h
4003_D014	RTC Status Register (RTC_SR)	32	R/W	0000_0001h
4003_D018	RTC Lock Register (RTC_LR)	32	R/W	0000_00FFh
4003_D01C	RTC Interrupt Enable Register (RTC_IER)	32	R/W	0000_0007h
4003_D800	RTC Write Access Register (RTC_WAR)	32	R/W	0000_00FFh
4003_D804	RTC Read Access Register (RTC_RAR)	32	R/W	0000_00FFh

RTC Control Register

43.2.5 RTC Control Register (RTC_CR)

Address: RTC_CR is 4003_D000h base + 10h offset = 4003_D010h

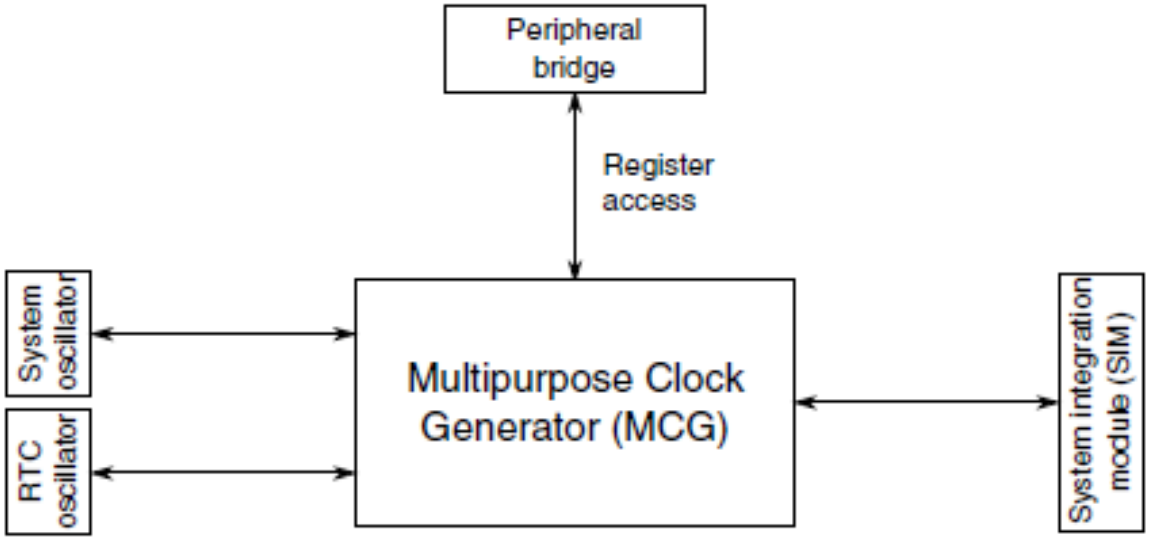
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	Reserved	SC2P	SC4P	SC8P	SC16P	CLKO	OSCE	0				UM	SUP	WPE	SWR
W		0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

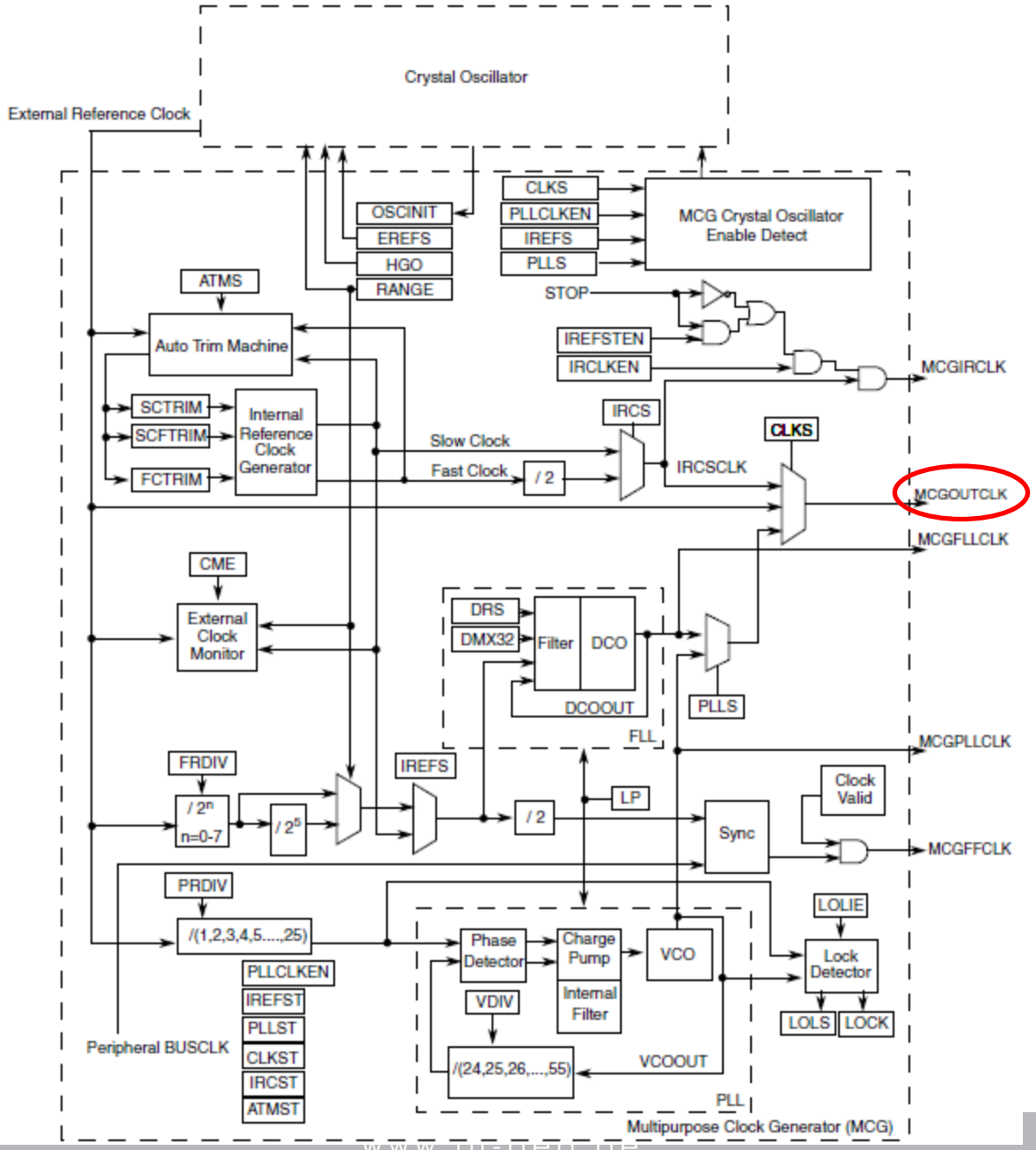
Multipurpose Clock Generator (MCG)

The multipurpose clock generator (MCG) module provides several clock source choices for the MCU. The module contains a frequency-locked loop (FLL) and a phase-locked loop (PLL). The FLL is controllable by either an internal or an external reference clock.

The PLL is controllable by the external reference clock. The module can select either of the FLL or PLL output clocks, or either of the internal or external reference clocks as a source for the MCU system clock. The MCG operates in conjunction with a crystal oscillator, which allows an external crystal, ceramic resonator, or another external clock source to produce the external reference clock.



MCG


Crystal Oscillator
External Reference Clock
OSCINIT
EREFS
HGO
RANGE
CLKS
PLLCLKEN
IREFS
PLLS
MCG Crystal Oscillator Enable Detect
STOP
ATMS
Auto Trim Machine
IREFSTEN
IRCLKEN
MCGIRCLK
SCTRIM
SCFTRIM
FCTRIM
Internal Reference Clock Generator
Slow Clock
Fast Clock
/ 2
IRCS
IRCSCLK
CLKS
MCGOUTCLK
MCGFLLCLK
CME
External Clock Monitor
DRS
DMX32
Filter
DCO
DCOOUT
FLL
PLLS
MCGPLLCLK
FRDIV
/ 2^n
n=0-7
/ 2^5
IREFS
/ 2
LP
Sync
Clock Valid
MCGFFCLK
PRDIV
/(1,2,3,4,5....,25)
Phase Detector
Charge Pump
Internal Filter
VCO
VDIV
/(24,25,26,...,55)
VCOOUT
PLL
LOLIE
Lock Detector
LOLS
LOCK
PLLCLKEN
IREFST
PLLST
CLKST
IRCST
ATMST
Peripheral BUSCLK
Multipurpose Clock Generator (MCG)

FLL and PLL

Frequency-locked loop (FLL)

- Digitally-controlled oscillator (DCO)
- DCO frequency range is programmable for up to four different frequency ranges.
- Option to program and maximize DCO output frequency for a low frequency external reference clock source.
- Option to prevent FLL from resetting its current locked frequency when switching clock modes if FLL reference frequency is not changed.
- Internal or external reference clock can be used as the FLL source.
- Can be used as a clock source for other on-chip peripherals.

Phase-locked loop (PLL)

- Voltage-controlled oscillator (VCO)
- External reference clock is used as the PLL source
- Modulo VCO frequency divider
- Phase/Frequency detector
- Integrated loop filter
- Can be used as a clock source for other on-chip peripherals.

2x IRC

Internal Reference Clock Generator

- **Slow** clock (32 kHz) with nine trim bits for accuracy
- **Fast** clock (4 MHz) with four trim bits
- Can be used as source clock for the FLL. In FEI mode, only the slow Internal Reference Clock (IRC) can be used as the FLL source.
- Either the slow or the fast clock can be selected as the clock source for the MCU
- Can be used as a clock source for other on-chip peripherals

The following non-volatile locations (4 bytes) are reserved for custom IRC user trim supported by some development tools. An alternate IRC trim to the factory loaded trim can be stored at this location. To override the factory trim, user software must load new values into the MCG trim registers.

Non-Volatile Byte Address	Alternate IRC Trim Value
0x0000_03FC	Reserved
0x0000_03FD	Reserved
0x0000_03FE (bit 0)	SCFTRIM
0x0000_03FE (bit 4:1)	FCTRIM
0x0000_03FF	SCTRIM

MCG Register

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value
4006_4000	MCG Control 1 Register (MCG_C1)	8	R/W	04h
4006_4001	MCG Control 2 Register (MCG_C2)	8	R/W	See section
4006_4002	MCG Control 3 Register (MCG_C3)	8	R/W	Undefined
4006_4003	MCG Control 4 Register (MCG_C4)	8	R/W	Undefined
4006_4004	MCG Control 5 Register (MCG_C5)	8	R/W	00h
4006_4005	MCG Control 6 Register (MCG_C6)	8	R/W	00h
4006_4006	MCG Status Register (MCG_S)	8	R	10h
4006_4008	MCG Auto Trim Control Register (MCG_ATC)	8	R/W	00h
4006_400A	MCG Auto Trim Compare Value High Register (MCG_ATCVH)	8	R/W	00h
4006_400B	MCG Auto Trim Compare Value Low Register (MCG_ATCVL)	8	R/W	00h

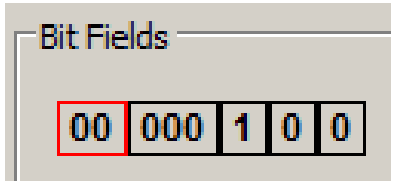
MCG Control 1 Register

24.3.1 MCG Control 1 Register (MCG_C1)

Address: MCG_C1 is 4006_4000h base + 0h offset = 4006_4000h

Bit	7	6	5	4	3	2	1	0
Read / Write	CLKS		FRDIV			IREFS	IRCLKEN	IREFSTEN
Reset	0	0	0	0	0	1	0	0

Internal Reference Select
Selects the reference clock source for the FLL.
0 External reference clock is selected.
1 The slow internal reference clock is selected.



MCG Control 2-4 Register

24.3.2 MCG Control 2 Register (MCG_C2)

Address: MCG_C2 is 4006_4000h base + 1h offset = 4006_4001h

Bit	7	6	5	4	3	2	1	0
Read	0	0	RANGE		HGO	EREFS	LP	IRCS
Write								
Reset	0	0	0	0	0	0	0	0

24.3.3 MCG Control 3 Register (MCG_C3)

Address: MCG_C3 is 4006_4000h base + 2h offset = 4006_4002h

Bit	7	6	5	4	3	2	1	0
Read	SCTRIM							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

24.3.4 MCG Control 4 Register (MCG_C4)

Reset values for DRST and DMX32 bits are 0.

Address: MCG_C4 is 4006_4000h base + 3h offset = 4006_4003h

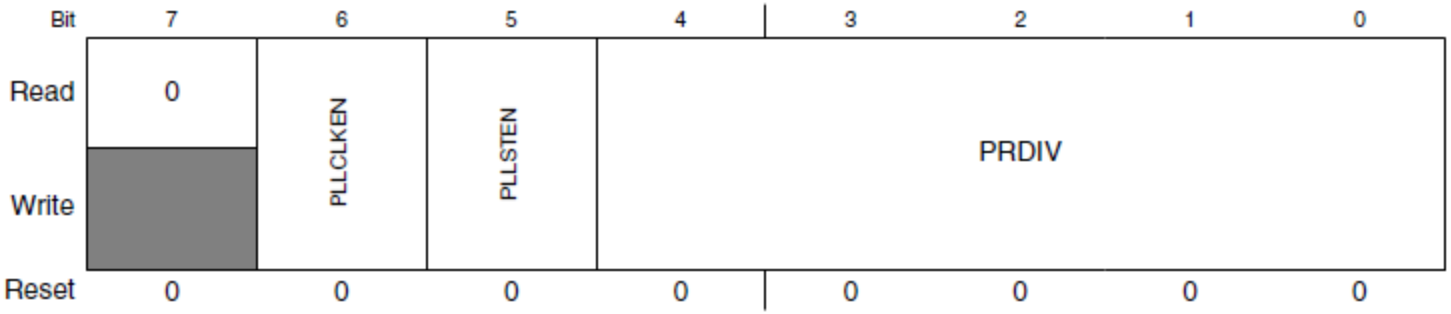
Bit	7	6	5	4	3	2	1	0
Read	DMX32	DRST_DRS		FCTRIM				SCFTRIM
Write								
Reset	0	0	0	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.
- A value for FCTRIM is loaded during reset from a factory programmed location . x = Undefined at reset.

MCG Control 5-6 Register

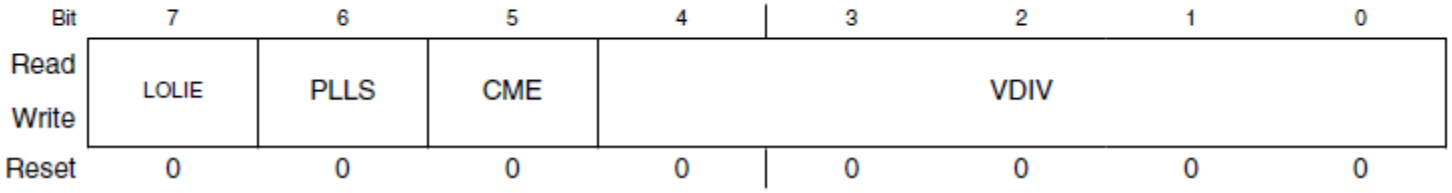
24.3.5 MCG Control 5 Register (MCG_C5)

Address: MCG_C5 is 4006_4000h base + 4h offset = 4006_4004h

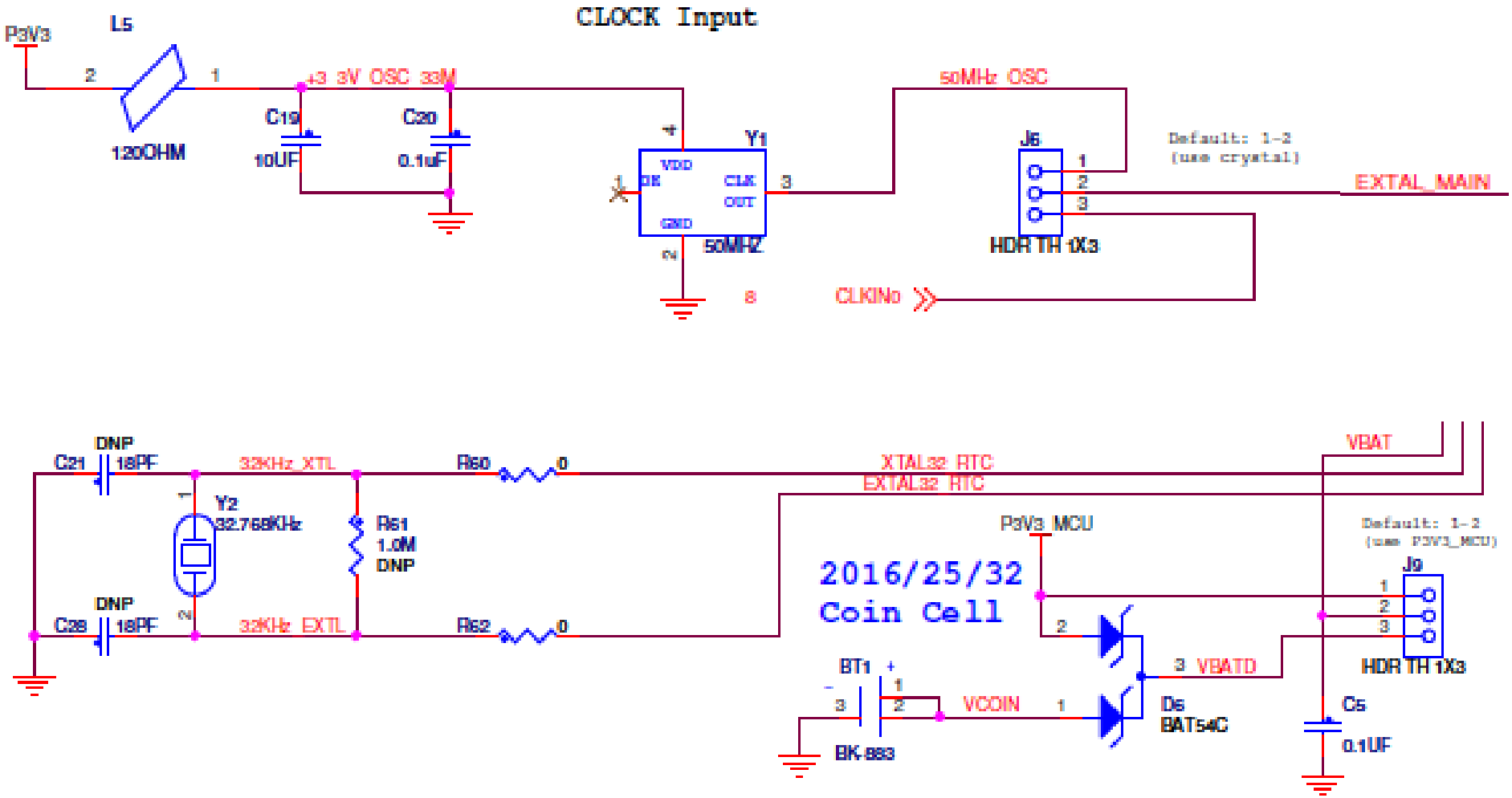


24.3.6 MCG Control 6 Register (MCG_C6)

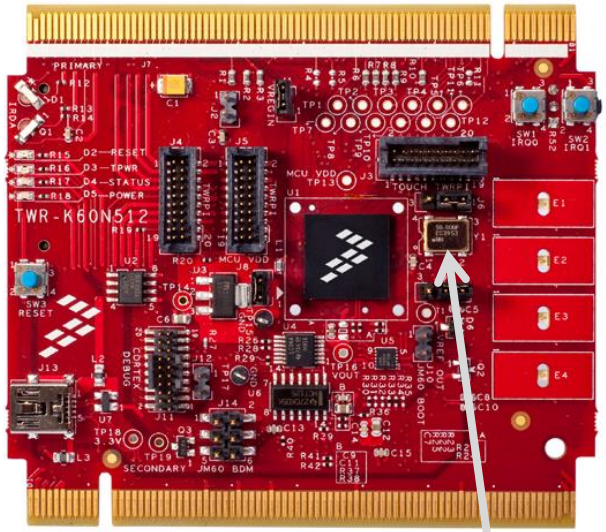
Address: MCG_C6 is 4006_4000h base + 5h offset = 4006_4005h

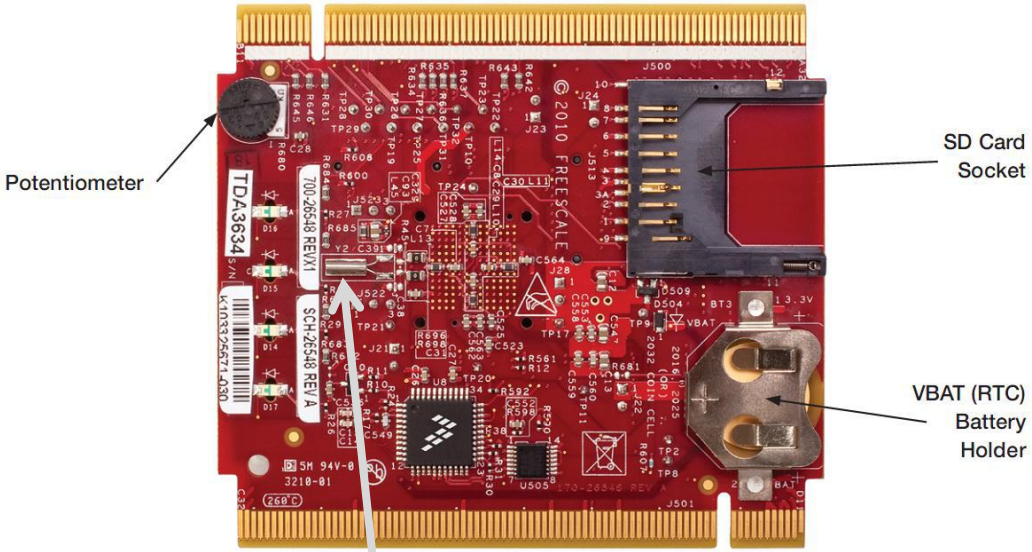


Clock Generation at the K60 Tower Module



Clock Generation at the K60 Tower Module

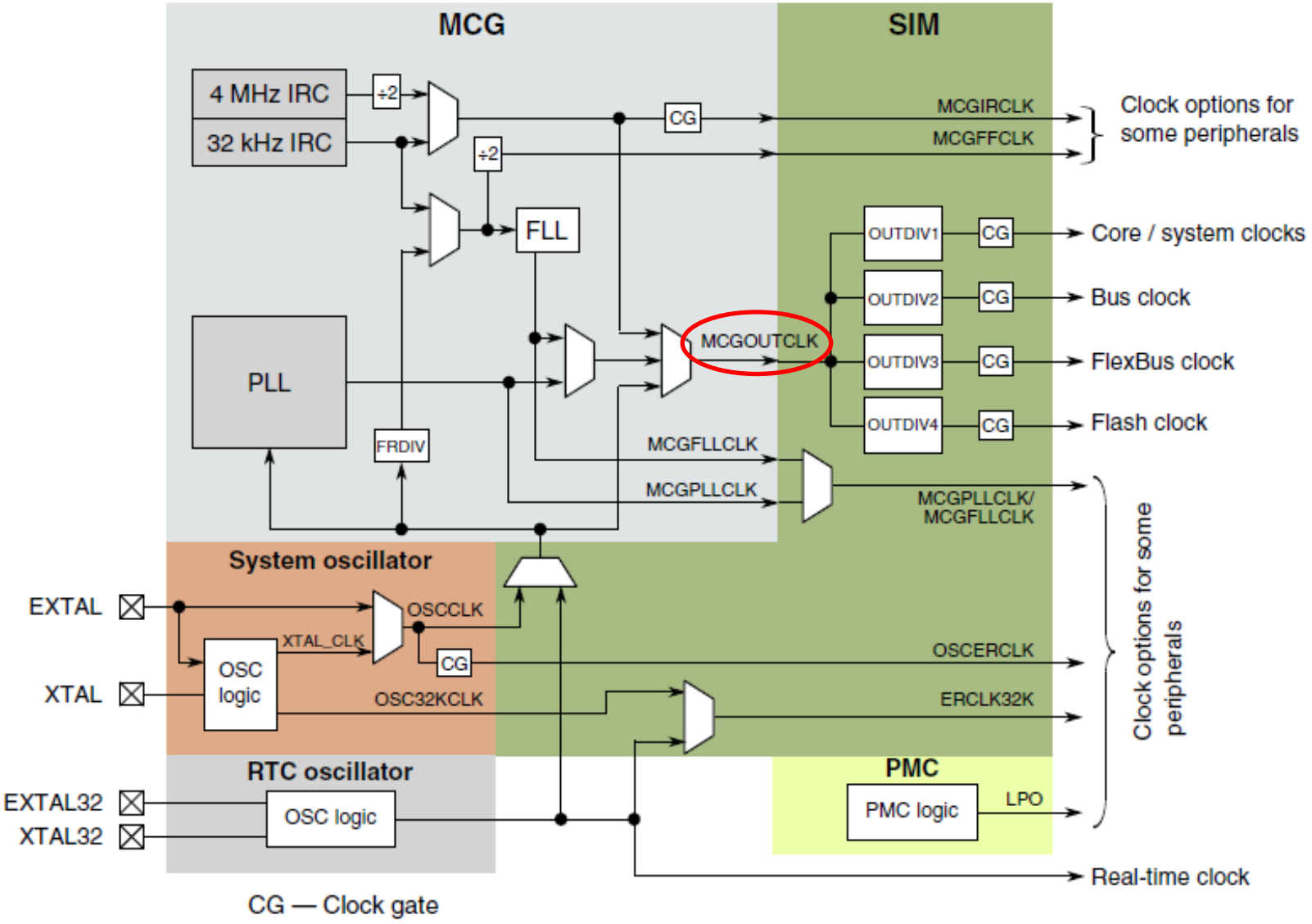




50 MHz Oscillator

32.768 kHz
Watch Crycstal

Clock Generation at the Kinetis K60



Which Module is Clocked from Which Clock?

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			
ARM Cortex-M4 core	System clock	Core clock	—
NVIC	System clock	—	—
DAP	System clock	—	—
ITM	System clock	—	—
ETM	System clock	TRACE clock	TRACE_CLKOUT
ETB	System clock	—	—
cJTAG, JTAGC	—	—	JTAG_CLK
System modules			
DMA	System clock	—	—
DMA Mux	Bus clock	—	—
Port control	Bus clock	LPO	—
Crossbar Switch	System clock	—	—
Peripheral bridges	System clock	Bus clock	—
MPU	System clock	—	—
LLWU, PMC, SIM	Bus clock	LPO	—
Mode controller	Bus clock	—	—
MCM	System clock	—	—
EWM	Bus clock	LPO	—
Watchdog timer	Bus clock	LPO	—

System Clock Gating Control Register 1 - 3

12.2.8 System Clock Gating Control Register 1 (SIM_SCGC1)

Address: SIM_SCGC1 is 4004_7000h base + 1028h offset = 4004_8028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							0	0		0	0									UART5	UART4	0									
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

12.2.9 System Clock Gating Control Register 2 (SIM_SCGC2)

Address: SIM_SCGC2 is 4004_7000h base + 102Ch offset = 4004_802Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																		DAC1	DAC0	0										ENET	
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

12.2.10 System Clock Gating Control Register 3 (SIM_SCGC3)

Address: SIM_SCGC3 is 4004_7000h base + 1030h offset = 4004_8030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0		ADC1	0		FTM2	0						SDHC	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0			SPI2	0							FLEXCAN1	0			RNGB
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

System Clock Gating Control Register 4 & 5

12.2.11 System Clock Gating Control Register 4 (SIM_SCGC4)

Address: SIM_SCGC4 is 4004_7000h base + 1034h offset = 4004_8034h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	1		LLWU	0							VREF	CMP	USBOTG	0	
W																
Reset	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		UART3	UART2	UART1	UART0	0		I2C1	I2C0	1		0	CMT	EWM	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

12.2.12 System Clock Gating Control Register 5 (SIM_SCGC5)

Address: SIM_SCGC5 is 4004_7000h base + 1038h offset = 4004_8038h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0													1	0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		PORTE	PORTD	PORTC	PORTB	PORTA	1		0	TSI		0		REGFILE	LPTIMER
W																
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

System Clock Divider Register 1

12.2.15 System Clock Divider Register 1 (SIM_CLKDIV1)

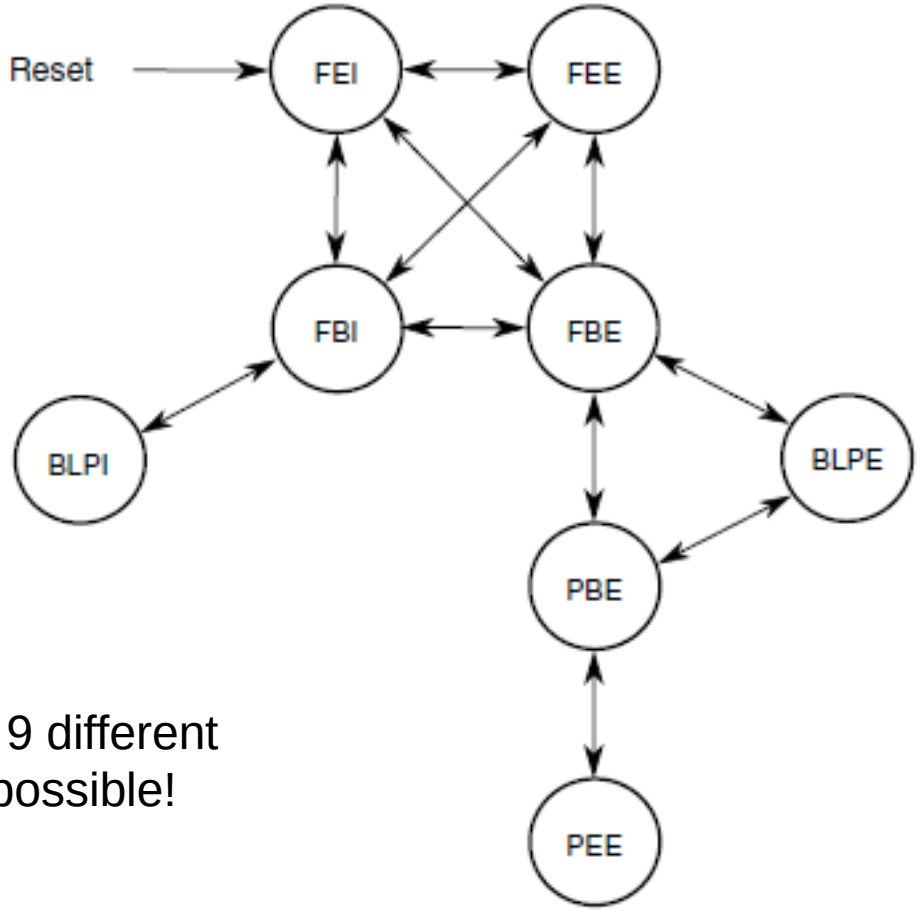
The CLKDIV1 register cannot be written to when the device is in VLPR mode.

Address: SIM_CLKDIV1 is 4004_7000h base + 1044h offset = 4004_8044h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	OUTDIV1				OUTDIV2				OUTDIV3				OUTDIV4				0															
W																																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

MCG Mode State Diagram



Alltogether 9 different states are possible!

Entered from any state when the MCU enters Stop mode → Stop → Returns to the state that was active before the MCU entered Stop mode, unless a reset occurs while in Stop mode.

MCGOUTCLK Frequency Calculation Options

Clock Mode	$f_{MCGOUTCLK}$[1]	Note
FEI (FLL engaged internal)	(f_{int} * F)	Typical $f_{MCGOUTCLK}$ = 20 MHz immediately after reset.
FEE (FLL engaged external)	(f_{ext} / FLL_R) *F	f_{ext} / FLL_R must be in the range of 31.25 kHz to 39.0625 kHz
FBE (FLL bypassed external)	f_{ext}	f_{ext} / FLL_R must be in the range of 31.25 kHz to 39.0625 kHz
FBI (FLL bypassed internal)	f_{int}	Typical f_{int} = 32 kHz
PEE (PLL engaged external)	(f_{ext} / PLL_R) * M	f_{ext} / PLL_R must be in the range of 2 – 4 MHz
PBE (PLL bypassed external)	f_{ext}	f_{ext} / PLL_R must be in the range of 2 – 4 MHz
BLPI (Bypassed low power internal)	f_{int}	
BLPE (Bypassed low power external)	f_{ext}	

1. FLL_R is the reference divider selected by the C1[FRDIV] bits, PLL_R is the reference divider selected by C5[PRDIV] bits, F is the FLL factor selected by C4[DRST_DRS] and C4[DMX32] bits, and M is the multiplier selected by C6[VDIV] bits.

1. Tuning Option: Clock Source Select

24.3.1 MCG Control 1 Register (MCG_C1)

Address: MCG_C1 is 4006_4000h base + 0h offset = 4006_4000h

Bit	7	6	5	4	3	2	1	0
Read / Write	CLKS		FRDIV			IREFS	IRCLKEN	IREFSTEN
Reset	0	0	0	0	0	1	0	0

Clock Source Select

Selects the clock source for MCGOUTCLK .

00 Encoding 0 — Output of FLL or PLL is selected (depends on PLLS control bit).

01 Encoding 1 — Internal reference clock is selected.

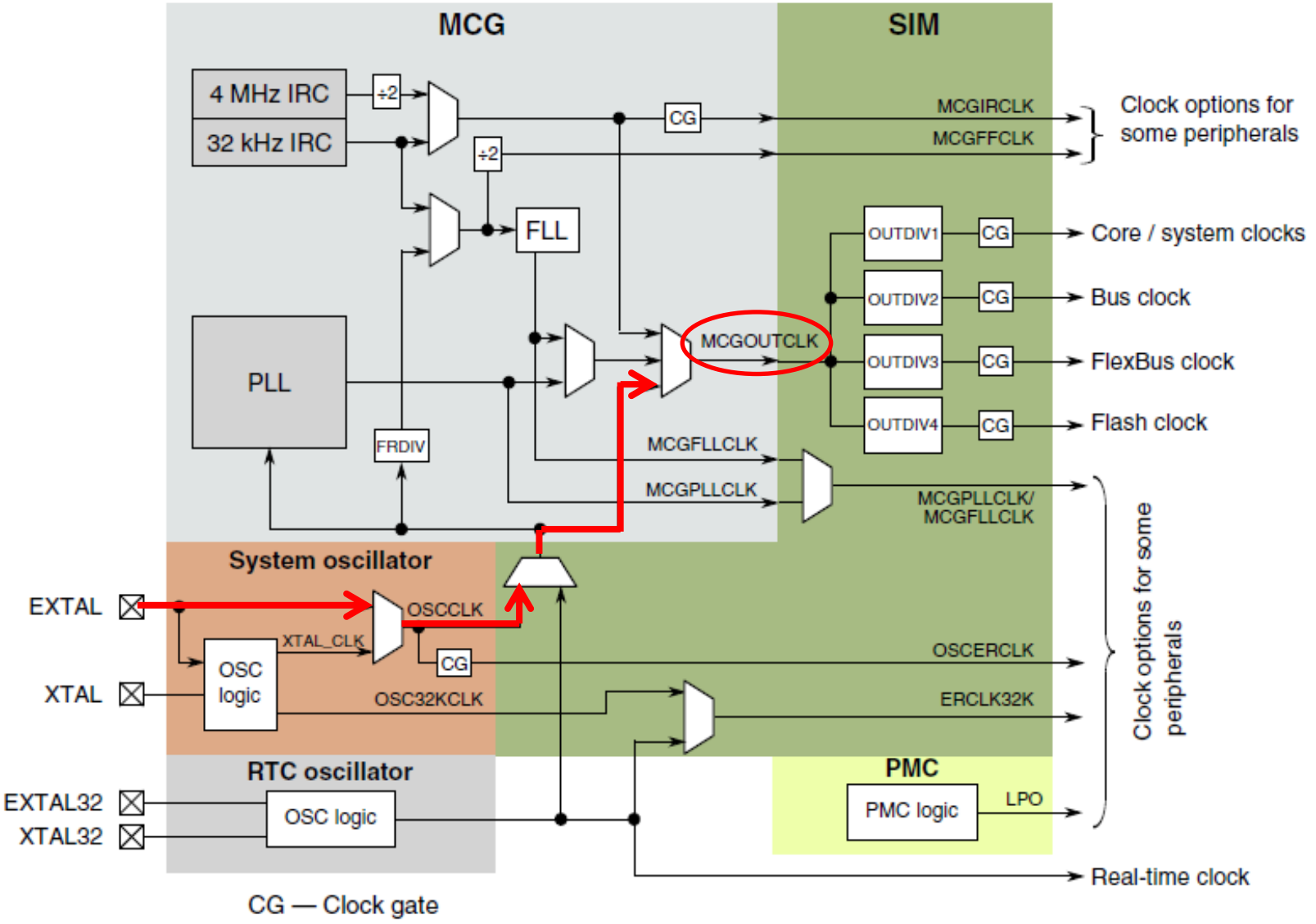
10 Encoding 2 — External reference clock is selected.

11 Encoding 3 — Reserved, defaults to 00.

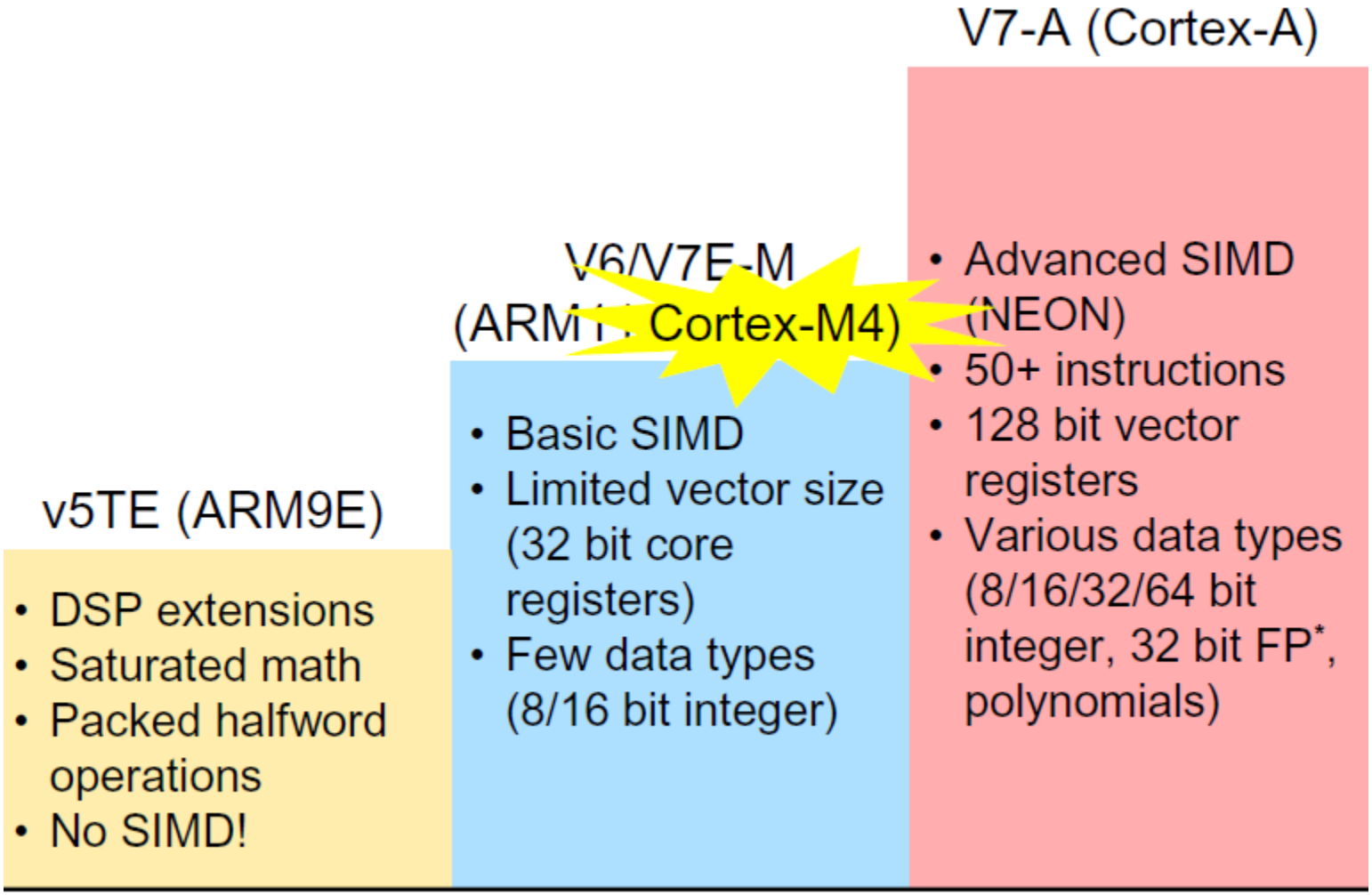
typ. 20 MHz

50 MHz

Clock Generation at the Kinetis K60



ARM Core Architectures



ARM Cortex M4 Core

Special Features of the Cortex M4 are:

- Supports up to 150 MHz frequency with 1.25DMIPS/MHz
- ARM Core based on the ARMv7 Architecture & ThumbR-2 ISA
- Microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments
- Harvard bus architecture
- 3-stage pipeline with branch speculation
- Integrated bus matrix
- Integrated Digital Signal Processor (DSP)
- Configurable nested vectored interrupt controller (NVIC)
- Advanced configurable debug and trace components
- Embedded Trace Macrocell (ETM)
- Optional single precision floating point unit (SPFPU)

Clock Cycles of the Cortex-M4 Core

Table 3-1 Cortex-M4 instruction set summary

Operation	Description	Assembler	Cycles
Move	Register	`MOV Rd, <op2>`	1
	16-bit immediate	`MOVW Rd, #<imm>`	1
	Immediate into top	`MOVT Rd, #<imm>`	1
	To PC	`MOV PC, Rm`	1 + P
Add	Add	`ADD Rd, Rn, <op2>`	1
	Add to PC	`ADD PC, PC, Rm`	1 + P
	Add with carry	`ADC Rd, Rn, <op2>`	1
	Form address	`ADR Rd, <label>`	1
Subtract	Subtract	`SUB Rd, Rn, <op2>`	1
	Subtract with borrow	`SBC Rd, Rn, <op2>`	1
	Reverse	`RSB Rd, Rn, <op2>`	1

Clock Cycles of the Cortex-M4 Core

Operation	Description	Assembler	Cycles
Multiply	Multiply	`MUL Rd, Rn, Rm`	1
	Multiply accumulate	`MLA Rd, Rn, Rm`	1
	Multiply subtract	`MLS Rd, Rn, Rm`	1
	Long signed	`SMULL RdLo, RdHi, Rn, Rm`	1
	Long unsigned	`UMULL RdLo, RdHi, Rn, Rm`	1
	Long signed accumulate	`SMLAL RdLo, RdHi, Rn, Rm`	1
	Long unsigned accumulate	`UMLAL RdLo, RdHi, Rn, Rm`	1
Divide	Signed	`SDIV Rd, Rn, Rm`	2 to 12[a]
	Unsigned	`UDIV Rd, Rn, Rm`	2 to 12[a]

Clock Cycles of the Cortex-M4 Core

Operation	Description	Assembler	Cycles
Count	Leading zeroes	`CLZ Rd, Rn`	1
Load	Word	`LDR Rd, [Rn, <op2>]`	2^b
	To PC	`LDR PC, [Rn, <op2>]`	$2^b + P$
	Halfword	`LDRH Rd, [Rn, <op2>]`	2^b
	Byte	`LDRB Rd, [Rn, <op2>]`	2^b
	Signed halfword	`LDRSH Rd, [Rn, <op2>]`	2^b
	Signed byte	`LDRSB Rd, [Rn, <op2>]`	2^b
	User word	`LDRT Rd, [Rn, #<imm>]`	2^b
	User halfword	`LDRHT Rd, [Rn, #<imm>]`	2^b

Literature and Links

http://www.arm.com/products/processors/cortex-m/cortex-m3.php

http://www.arm.com/products/processors/technologies/instruction-set-architectures.php

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=K60

K60 Sub-Family Reference Manual

Kinetis Peripheral Module Quick Reference

Cortex-M4 Technical Reference Manual

http://www.arm.com/products/processors/cortex-m/index.php

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