Journal

\* *Note: Unless stated otherwise, the work was done together*

***July 5th (Friday)***

***----------------------------------------------------------------------------------------------------***

* 10:15 - Debugged a logical error in forwarding unit
* 11:46 - We all worked on the forwarding unit for the lab and the project
* 12:15 - Edited the code realized we did not make a mistake, so we went back to the original code
* 12:16 - Restarting hazard control unit
* 13:01 - Testing hazard unit and recording results
* 13:33 - Started flushing
* 14:03 - Began testing and recording results
* 14:28 - Finished recording results
* 16:00 - Shahd worked on the diagram
* 16:15 – Took a 2 hr break
* 18:15 – Started debugging the forwarding unit again

***July 6th (Saturday)***

***----------------------------------------------------------------------------------------------------***

* 11:10 - Shahd worked on the diagram
* 13:06 - Discovered we do not need the mux for the jal that chooses between pc and rs1 going to the ALU because the immgen does it. We also discussed if we should start with 2 memories or 1 then do the pipelined.
* 13:56 - Lobna and Mariane started integrating the pipeline into the previous code
* 19:48 pm - Lobna started renaming diagram wires according to code as she finished the RISCV module (till 22:11)

***July 7th (Sunday)***

***----------------------------------------------------------------------------------------------------***

* 10:15 - Lobna finished the final connections (consulted Mariane and Shahd before doing WB stage code), then I fixed the warnings that appeared while running the testbench while Shahd and Mariane were working on correcting some mistakes we found in diagram
* 12:14 - Shahd edited the diagram
* 12:15 - Mariane and Shahd worked on analyzing the lab results while Lobna debugged the RISCV module
* 15:28 - Analyzing results, and realizing we forgot the pc + part of the auipc
* 16:24 - Found an error in storing byte, trying to debug
* 16:51 - Found the error and fixed it
* 18:31 - Found the error for the reg file (wrong cntrl signal) that we fixed
* 18:31 - Fixed the target error and the unknown PCin value
* 21:45 - Added the multiplexer for PC for auipc

***July 8th (Monday)***

***----------------------------------------------------------------------------------------------------***

* 10:15 - Debugging
* 11:27 - Lobna debugged. Shahd and Mariane worked on report and diagram
* 11:45 - Shahd finished diagram
* 12:30 - The Dr. came and found an error we had trouble finding in the regfile
* 12:40 - Reanalyzing the results
* 12:45 -Taking screenshots of the test results
* 1:06 - Started making instruction memory byte addressable
* 1:10 - Brainstorming for single memory
* 11:27 - Added multiplexer for single memory address input

* 14:43 - Shahd was working on the report, Mariane on the journal and Lobna on the readme

* 15:23 - Mariane finished the journal and is adding the comments on top of each module, and Lobna is cleaning up the journal while Shahd continues working on the report

***July 9th (Tuesday)***

***----------------------------------------------------------------------------------------------------***

* 10:15 - Asked the professor about the clock inputs
* 10:30 - Changed the flushing mechanism, and removed the hazard unit
* 10:45 - Added a nop as the first intruction in the memory
* 12:00 - Debugging
* 12:30 - Noticed that we need to move the comparator to the EX stage
* 1:00 - Debugged
* 1:40 - Tried to change the flushing again
* 2:00 - Changed the forwarding multiplexers
* 6:15 - Forwarded the PCplus4
* 6:30 - Testing
* 7:00 - Noticed the jal is not working
* 7:20 - Identified problem, do not know how to solve yet
* 9:08 - Testing the shift instructions

***July 10th (Wenesday)***

***----------------------------------------------------------------------------------------------------***

* 10:15 - Fixed the control unit to accomidate for the jal
* 12:00 - Noticed the immediates were wrong, so we fixed those as well
* 2:00 - Testing on simulation
* 5:00 - Testing on FPGA

***July 11th (Thursday)***

***----------------------------------------------------------------------------------------------------***

* 10:24 – Shahd and Lobna are testing on FPGA
* 10:47 – We agree on a method of implementing the bonus, and now Mariane is working on it as Shahd and Lobna tabulate the FPGA test results in the excel
* 12:23 – Mariane took screenshot of the FPGA results and we added them to the excel
* 12:46 – Updated the diagram to accommodate for final changes that took place
* 1:22 – Mariane and Shahd are working on the bonus as Lobna checks that the final diagram reflects the final code
* 2:47 – Agreed we need to add a MUX for PC+2 for compressed instructions
* 3:19 – Shahd is working on the report as Mariane continues to work on the bonus and Lobna updates the diagram and renames lines to further reflect the code
* 7:34– Mariane finished working on the bonus