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University of New Mexico

Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2011) Exam 2

Name: Date: Nov. 16, 2011

Note: Only calculator, pencils, and pens are allowed.

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1. (10 points) True or false:

(a) Higher noise margin is always desirable. (true)

(b) To decrease t_{pHL}, the NMOS threshold voltage must be increases. (false)

(c) When the input of a CMOS inverter is high, the leakage current will be determined by I_{OFF} of PMOS. (true) PMOS off

(d) In a CMOS inverter, the faster input rise time results in higher short-circuit power. (false)

(e) The propagation delay in a simple RC network is 0.69 times of its time-constant. (true)

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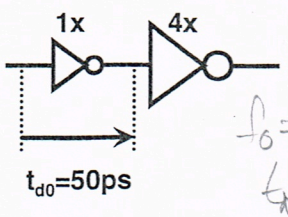
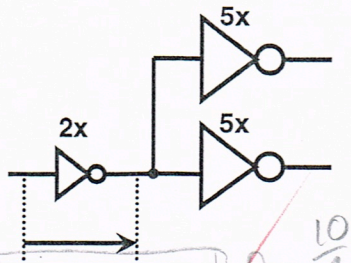
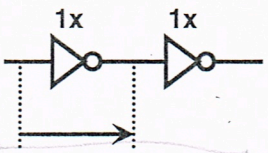
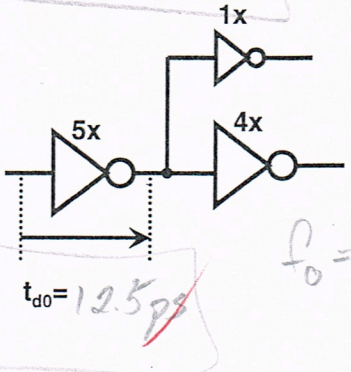
2. (15 points) Given the delay of a standard fanout-4 delay is 50ps (i.e. 1x inverter driving a 4x inverter), determine the delay in each of the following cases:









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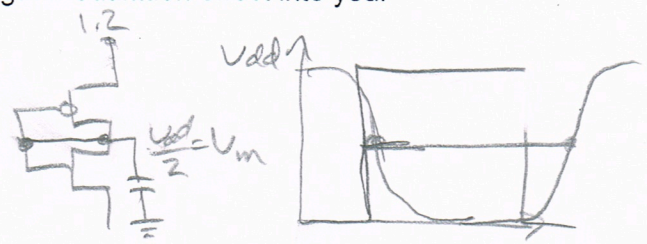
3. (10 points) Determine the $(W/L)_p$ of the PMOS transistor in a CMOS inverter such that the switching threshold voltage, V_M, becomes exactly $V_{DD}/2$. Assume that $K'_n=120uA/V^2$, $Vt_n=0.3V$, $\lambda_n=0.01V^{-1}$, $(W/L)_n=10$, $K'_p=50uA/V^2$, $Vt_p=-0.4V$, $\lambda_p=-0.02V^{-1}$ and $V_{DD}=1.2V$. Include the channel length modulation effect into your calculation.

$V_m = V_{dd}/2$

@ $V_m = V_i = V_o$



$$\frac{K_n'}{2}\left(\frac{W}{L}\right)_n (V_m - V_{tn})^2(1+\lambda_n V_m) = \frac{K_p'}{2}\left(\frac{W}{L}\right)_p (V_{dd}-V_m-V_{tp})^2(1+\lambda_p(V_{dd}-V_m))$$

$$K_n' \frac{W}{L_n}\left(\frac{V_{dd}}{2} - V_{tn}\right)^2(1+\lambda_n V_{dd}/2) = \left(\frac{W}{L}\right)_p =$$

$$K_p' \left(\frac{V_{dd}}{2} - V_{tp}\right)^2(1+\lambda_p V_{dd}/2)$$

$$\frac{120\mu(10)(0.6-0.3)^2(1+0.01(0.6))}{50\mu(0.6-0.4)^2(1+0.02(0.6))} = \boxed{53.7}$$

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4. (10 points) Calculate the short circuit current, I_{DDMax}, in the CMOS inverter of problem 3. Again, include the channel length modulation effect into your calculation.

$I_{sc} = I_{ds}$ @ V_m $\quad V_m = \frac{V_{dd}}{2}$

$$I_{dsp} = I_{dsn} = \frac{K_n'}{2}\frac{W}{L}\left(\frac{V_{dd}}{2} - V_{tn}\right)(1+\lambda_n \frac{V_{dd}}{2}) = \frac{1.08\times10^{-4}}{2} = \boxed{54\mu A}$$

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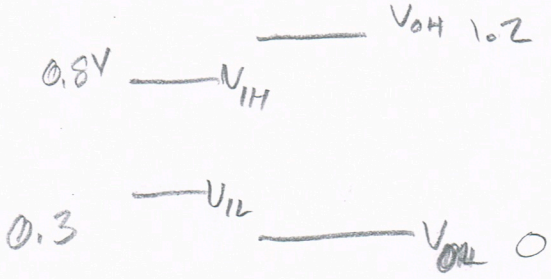
5. (10 points) The output of the CMOS inverter in problem 3 is connected to a novel Carbon Nanotube-based logic gate with V_{IL}=0.3V, and V_{IH}=0.8V. Sketch the noise margin rectangles and determine the low and high noise margin.



$NMH = V_{OH} - V_{IH} = 0.4$

$NML = V_{IL} - V_{OL} = 0.3$

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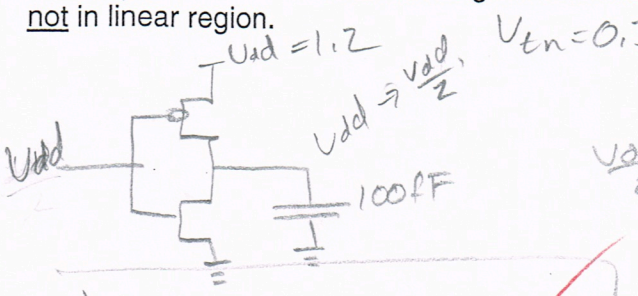
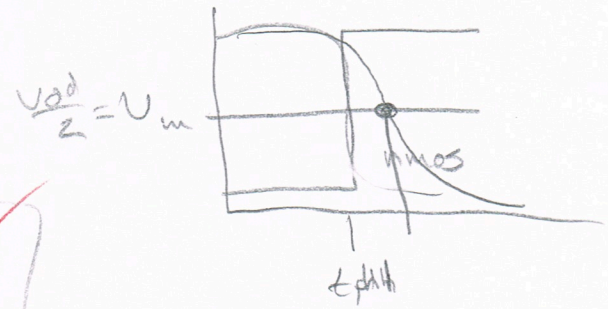
6. (15 points) The output of the CMOS inverter in problem 3 is connected to a 100fF load capacitor. Use the average current technique to find high-to-low propagation delay, t_{pHL}. Include the channel length modulation effect only in saturation region, not in linear region.





$$t_{phl} = \frac{C_L \Delta V}{I_{av\,NMOS}}$$

$$t_{phl} = \frac{100f\left(\frac{V_{dd}}{2}\right)}{\frac{1}{2}K_n\frac{W}{L}\left[\frac{(V_{gs}-V_{tn})^2}{2}(1+\lambda_n V_{ds}) + (V_{gs}-V_{tn})V_{ds} - \frac{V_{ds}^2}{2}\right]}$$

$$t_{phl} = \frac{100f(0.6)}{\frac{120\mu(10)}{2}\left[\frac{(1.2-0.3)^2}{2}(1+0.01(1.2)) + (V_{dd}-0.3)(V_{dd}/2) - \frac{V_{dd}^2}{8}\right.}$$

$$= \frac{100f(0.6)}{7.07\times10^{-4}} = 8.47\times10^{-11} = 84.8\text{ps}$$

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7. (10 points) Determine the dynamic power consumption in the CMOS inverter of problem 6, if a square wave pulse running at 1GHz frequency is applied to its input.

$$P = C_L V_{dd}^2 f = 100fF(1.2)^2(1G) = 1.44\times10^{-4} = \boxed{144\mu W}$$

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8. (10 points) Calculate the equivalent output resistance, R_{OHL}, of the inverter in problem 3 for the high-to-low transition. Use the results that you found in problem 6.

$$Q = C_L \Delta V = I_{av} \Delta t$$

$$\Delta t = \frac{C_L \Delta V}{I_{av}} = 0.7RC_L \Rightarrow \frac{t_{phl}}{C_L} = R \propto \boxed{8485\Omega}$$

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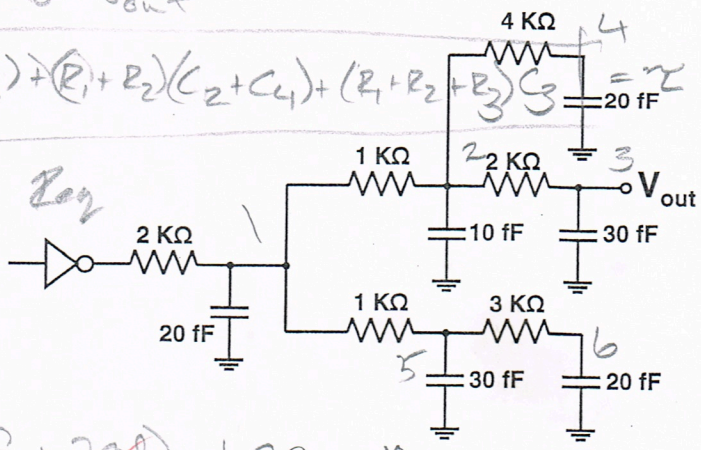
9. (10 points) The CMOS inverter of problem 3 is connected to an interconnect network shown below. Use the R_{oHL} found in problem 8 to find the high-to-low propagation delay, t_{PHL}.

Sum of all of C_L · Sum of all Resistors on path to V_{out}

$$R_1(C_1+C_5+C_6)+(R_1+R_2)(C_2+C_4)+(R_1+R_2+R_3)C_3 = \tau$$



R_{eq}

R_{eq} 848

$$(2k+R_{eq})(20f+30f+20f) = 1.99\times10^{-10}$$

$$+(2k+R_{eq}+1k)(10f+20f) = 1.15\times10^{-10}$$

$$+(2k+R_{eq}+1k+2k)(30f) = 1.75\times10^{-10}$$

$$= 4.89\times10^{-10} = 448ps = \tau$$

$t_p = 0.69\tau$

$t_{pHL} = 448ps \cdot 0.69 = \boxed{309ps}$