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# University of New Mexico

**Department of Electrical and Computer Engineering**

## ECE 321 – Electronics I (Fall 2011) Exam 1

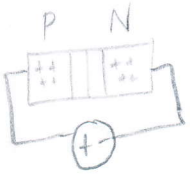
Name: Edgar Chavez Date: September 26, 2011

Note: Only calculator, pencils, and pens are allowed.

8

**1.** (10 points) True or false:

(a) Drain potential in PMOS is higher than the source potential. ( F ) ✓ PMOS - source = high




(b) The width of depletion region in a PN junction increases, by decreasing the N and P doping concentration. ( T ) ✓

(c) The diffusion current occurs because of applied electric field. ( T ) ✗ F

(d) The change of threshold voltage due to the change in the bulk potential is called "channel length modulation". ( F ) ✓

(e) The threshold voltage of a "depletion type" PMOS is positive. ( T ) ✓

10

**2.** (10 points) Consider the flowing logic circuit. Reduce this logic to minimum gates.

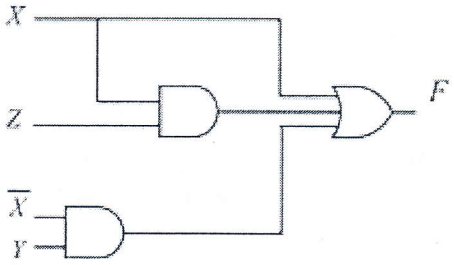
$X + XZ + \bar{X}Y = F$

$X(1+Z) + \bar{X}Y = F$

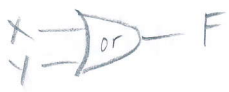
$X + \bar{X}Y = F$ ✓

$(X+\bar{X})(X+Y) = F$

$F = X + Y$




✓



15

**3.** (20 points) The voltage of a forward bias diode increases by 60mV. Compute the amount of the diode current increase due to this voltage change.

Hint: Assume the diode current equation can be approximated by $I_D \approx I_S \cdot e^{\frac{V_D}{V_{th}}}$

$I_D \approx I_S e^{V_D/V_{TH}}$ $\quad V_{D1} = 0 \Rightarrow I_{D1} \approx I_S$

$V_{D2} = 60mV \Rightarrow I_{D2} \approx I_S e^{60mV/V_{TH}}$

$\Delta I_D = I_{D2} - I_{D1} \approx I_S e^{60mV/V_{TH}} - I_S$

$\approx I_S (e^{60mV/V_{TH}} - 1)$

if $T = 300K \rightarrow V_{TH} = 26mV$ ✓

$\Delta I_D = I_S (e^{60mV/26mV} - 1) \approx 9.05 I_S$ ✓

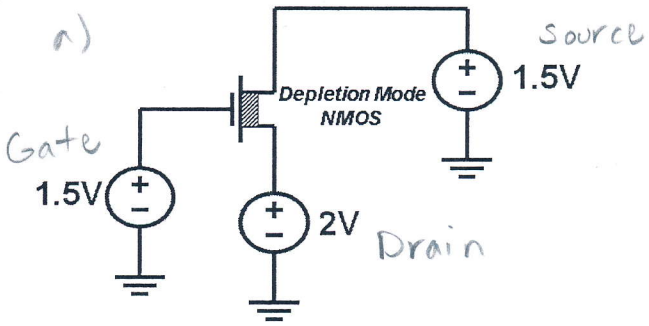
20

**4.** (20 points) In the circuit below, assume that the *depletion mode NMOS* has $K'_n = 100uA/V^2$, $(W/L)=10$, and $V_{tn}=-1V$. Ignore the body effect and channel length modulation.

(a) Identify Source, Gate, and Drain terminals
(b) Find the region of operation
(c) Determine $I_{DS}$

$V_{Tn} = -1 \Rightarrow |V_{Tn}| = 1V$

a)




$V_{GS} = 1.5 - 1.5 = 0V$

$V_{DS} = 2 - 1.5 = 0.5V$

$V_{DS} < V_{GS} - V_T$

$0.5 < 0 - (-1)$

b) $0.5 < 1 \Rightarrow$ linearity ✓

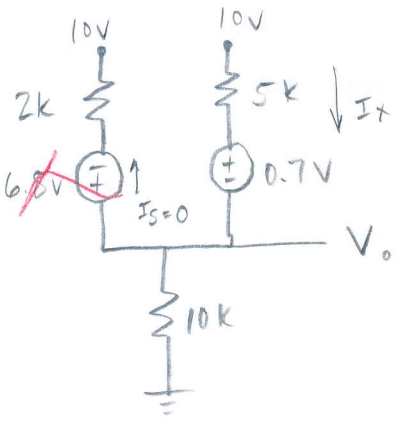
$I_{DS} = K'_n \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}\right]$

$I_{DS} = 100\,\mu A/V^2 \,(10) \left[(0+1)(0.5) - \frac{(0.5)^2}{2}\right]$ ✓

c) $I_{DS} = 375\,\mu A$

20

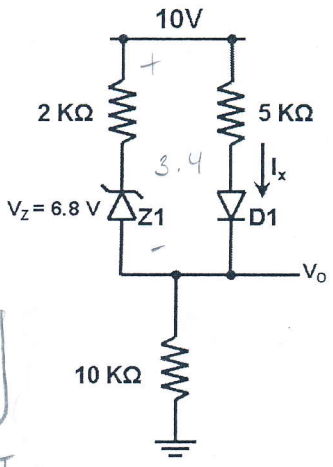
**5.** (20 points) Assume that the diode D1 has $V_\gamma$=0.7V and $I_S$=1nA and the Zener diode Z1 has $V_Z$=6.8V, $V_\gamma$=0.7V, and $I_S$=0. Determine $I_X$ and $V_O$.



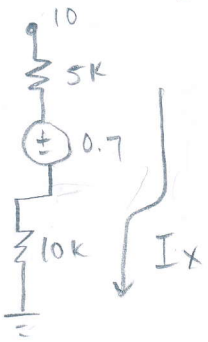

$I_{DZ} = I_{SZ}\, e^{V_D/V_{TH}}$

$I_{DZ} = 0\,(e^{V_D/V_{TH}})$

$I_{DZ} = 0\ A$ ✓




$10V\left(\frac{10}{15}\right) = 6.6$




$10V = I_X 5k + 0.7 + I_X 10k$

$10V = 15k I_X + 0.7$

$15k I_X = 9.3V$ ✓

$I_X = \frac{9.3}{15k} = 620\mu A$

$V_o = I_X 10k$

$= 620\mu A\,(10{,}000)$

$\approx 6.20\ V$ ✓

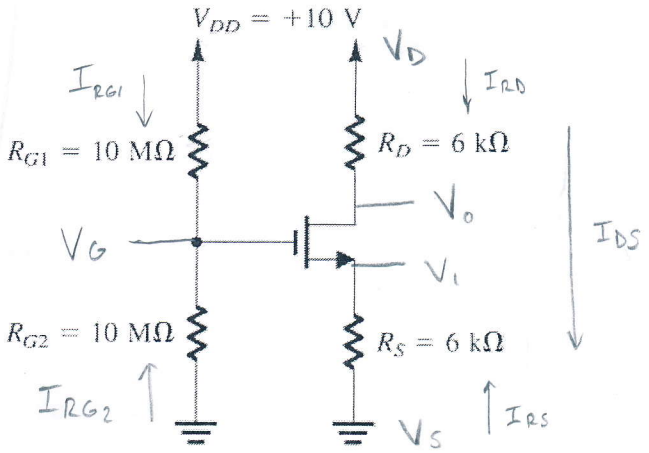
$M = 10^6$ 20

**6.** (20 points) Analyze the circuit to determine the voltages at all nodes and the currents thorough all branches. Let $V_{Tn}$=1V, $K'_n$=100 μA/V$^2$, and (W/L)=10.

$$V_G = 10\left(\frac{10M}{10M+10M}\right) = 5V$$

$$I_{RG1} = \frac{10-5}{10M} = \frac{5}{10M} = 500nA$$

$$I_{RG2} = \frac{0-5}{10M} = \frac{-5}{10M} = -500nA$$




$V_i = I_{DS}(6k)$

Assume saturation: $V_{DS} > V_{GS} - V_{Tn}$

$$I_{DS} = \frac{k'_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{Tn})^2$$

$V_{GS} = V_G - V_i = 5 - I_{DS}(6k)$ $\qquad V_{DS} = V_o - V_i$

$$I_{DS} = \frac{100\mu A/V^2}{2}(10)(5 - I_{DS}(6k) - 1)^2$$

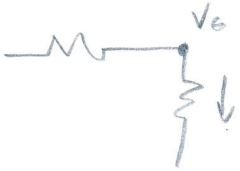
$I_{DS} = 500\mu A$ or $I_{DS} = 888\mu A$

IF $I_{DS} = 500\mu A \rightarrow V_i = 500\mu A(6k) = 3 \Rightarrow V_{GS} = 5-3 = 2V \Rightarrow V_o = 7V$

IF $I_{DS} = 888\mu A \rightarrow V_i = 888\mu A(6k) = 4.8 \Rightarrow V_{GS} = 5-4.8 = 0.2V \Rightarrow V_o = 9.3$

$I_{DS} = 888\mu A \rightarrow V_{GS} = 0.2V < V_{Tn}$

$I_{DS} = 500\mu A$ $\quad V_o = 7V$ $\quad V_i = 3V$



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# University of New Mexico

**Department of Electrical and Computer Engineering**

## ECE 321 – Electronics I (Fall 2011) Exam 2

Name: Edgar Chavez Date: Nov. 16, 2011

Note: Only calculator, pencils, and pens are allowed.

10

**1.** (10 points) True or false:

(a) Higher noise margin is always desirable. ( T )

(b) To decrease $t_{pHL}$, the NMOS threshold voltage must be increases. ( F )

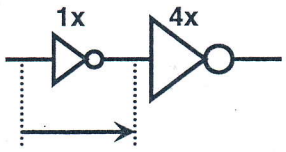
(c) When the input of a CMOS inverter is high, the leakage current will be determined by $I_{OFF}$ of PMOS. ( T )

(d) In a CMOS inverter, the faster input rise time results in higher short-circuit power. ( F )

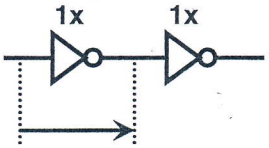
(e) The propagation delay in a simple RC network is 0.69 times of its time-constant. ( T )

15

**2.** (15 points) Given the delay of a standard fanout-4 delay is 50ps (i.e. 1x inverter driving a 4x inverter), determine the delay in each of the following cases:

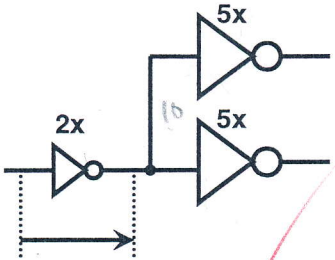



$t_{d0}$=50ps

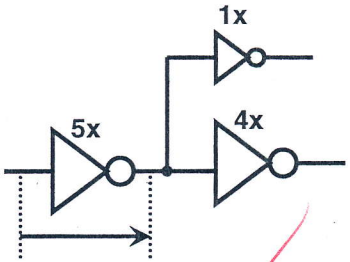



$t_{d0}$= 12.5ps

n ∝ tp



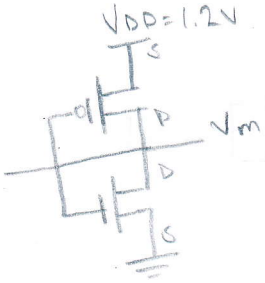

$t_{d0}$= 62.5ps




$t_{d0}$= 12.5ps

2

**3.** (10 points) Determine the $(W/L)_p$ of the PMOS transistor in a CMOS inverter such that the switching threshold voltage, $V_M$, becomes exactly $V_{DD}/2$. Assume that $K'_n=120uA/V^2$, $Vt_n=0.3V$, $\lambda_n=0.01V^{-1}$, $(W/L)_n=10$, $K'_p=50uA/V^2$, $Vt_p=-0.4V$, $\lambda_p=-0.02V^{-1}$ and $V_{DD}=1.2V$. Include the channel length modulation effect into your calculation.




Assume saturation:

$$|I_{DS}| = \frac{K'_p}{2}\left(\frac{W}{L}\right)_p (|V_{GS}| - |V_{Tp}|)^2 = \frac{50uA/V^2}{2}\left(\frac{W}{L}\right)_p (\quad ?\quad )$$

Since $\left(\frac{W}{L}\right)_n = 10$ then $\left(\frac{W}{L}\right)_p \approx 2\left(\frac{W}{L}\right)_n = 20$

2

**4.** (10 points) Calculate the short circuit current, $I_{DDMax}$, in the CMOS inverter of problem 3. Again, include the channel length modulation effect into your calculation.

$$I_{DDMax} = I_{SC} = I_{av} \cdot V_{DD} = P_{SC}$$

$I_{av} = 462\mu A$ ?

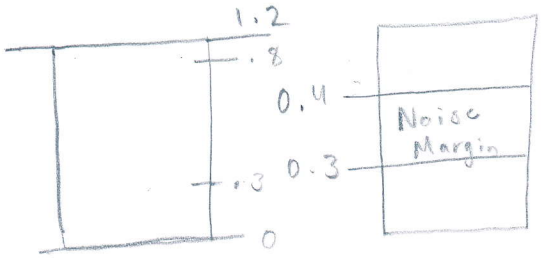
$= 554\mu$

10

**5.** (10 points) The output of the CMOS inverter in problem 3 is connected to a novel Carbon Nanotube-based logic gate with $V_{IL}$=0.3V, and $V_{IH}$=0.8V. Sketch the noise margin rectangles and determine the low and high noise margin.

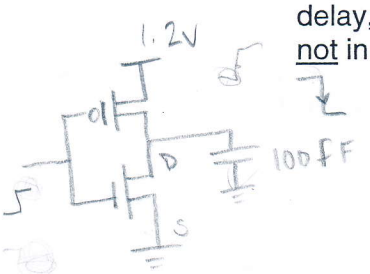
$NM_H = V_{OH} - V_{IH}$ $\quad NM_L = V_{IL} - V_{OL}$

$1.2 - 0.8 = 0.4$ $\quad = 0.3 - 0 = 0.3$




15

**6.** (15 points) The output of the CMOS inverter in problem 3 is connected to a 100fF load capacitor. Use the average current technique to find high-to-low propagation delay, $t_{pHL}$. Include the channel length modulation effect only in saturation region, not in linear region.




$$t_{PHL} = \frac{C_L (V_{DD}/2)}{I_{av}}$$

PMOS: OFF

NMOS: ON $\quad V_{GS} = 1.2 \quad V_{DS} = V_{DD} = 1.2 \Rightarrow$ saturation

(A) $I_{DS_1} = \frac{K'_n}{2}\left(\frac{W}{L}\right)_n (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS})$

$= \frac{120\mu A}{2}(10)(1.2 - 0.3)^2 (1 + 0.01(1.2)) = 492\mu A$

(B) $V_{GS} = 1.2 \quad V_{DS} = V_{DD}/2 = 0.6 \Rightarrow$ linear

$I_{DS_2} = K'_n \left(\frac{W}{L}\right)_n \left[(V_{GS} - V_{Tn}) V_{DS} - \frac{V_{DS}^2}{2}\right]$

$= 120\mu A (10)\left[(1.2 - 0.3)(0.6) - \frac{(0.6)^2}{2}\right] = 432\mu A$

$I_{av} = \frac{492\mu A + 432\mu A}{2} = 462\mu A$

$t_{PHL} = \frac{(100fF)(1.2/2)}{462\mu A} = 129.87\,ps$

10

**7.** (10 points) Determine the dynamic power consumption in the CMOS inverter of problem 6, if a square wave pulse running at 1GHz frequency is applied to its input.

$$\text{Dynamic Power} = V_{DD}^2 C_L f$$
$$= (1.2)^2 (100FF)(1GHz)$$
$$= 144\mu W$$

10

**8.** (10 points) Calculate the equivalent output resistance, $R_{OHL}$, of the inverter in problem 3 for the high-to-low transition. Use the results that you found in problem 6.

$$R_{OHL} = \frac{V_{DD}/2}{0.69 I_{av}} = \frac{1.2/2}{0.69 I_{av}}$$

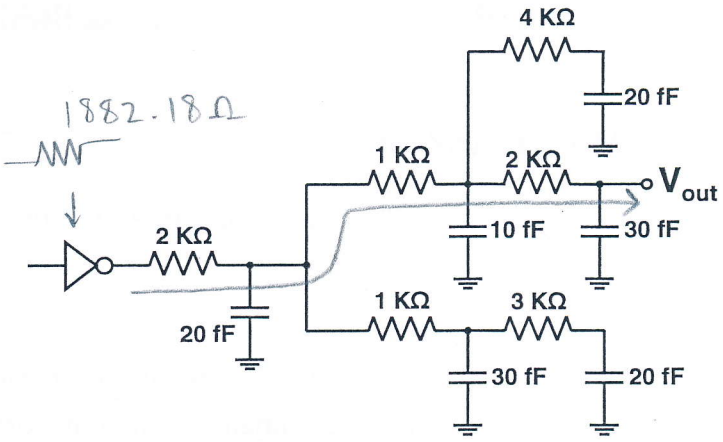
$I_{av}$ from problem 6 = 462 μA

$$R_{OHL} = \frac{0.6}{0.69(462\mu A)} = 1,882.18\,\Omega$$

10

**9.** (10 points) The CMOS inverter of problem 3 is connected to an interconnect network shown below. Use the $R_{oHL}$ found in problem 8 to find the high-to-low propagation delay, $t_{PHL}$.

$t_{PHL} = 0.69\tau$




$\tau = 20fF(2k + 1882.18) + 10fF(3k + 1882.18) + 30fF(5k + 1882.18)$
$+ 30fF(2k + 1882.18) + 20fF(2k + 1882.18)$
$+ 20fF(3k + 1882.18)$
$= 624.68\ ps$

$t_{pHL} = 0.69\ (624.68\ ps)$
$= 431.03\ ps$