97/100

University of New Mexico
Department of Electrical and Computer Engineering

ECE 321L – Ele[redacted] **Exam #1**

Nar[redacted] Date: September 26, 2018

Note[redacted]llowed.

10 **1.** (10 points) True or false: voltage P:S>D

(a) A diode in forward bias can be modeled as a current source. (F) ✓

(b) The source voltage is higher than the drain voltage in a PMOS. (T) ✓

(c) The unit for channel length modulation parameter (λ) is V^{-1}. (T) ✓

(d) Increasing the reverse bias of a diode increases its parasitic capacitance. (F) ✓

(e) Electrons are minority carriers in a P-type semiconductor. (T) ✓

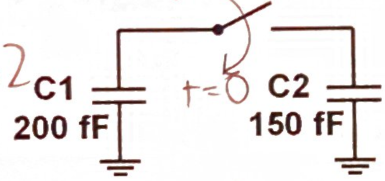
Holes are majority

15 **2.** (15 points) In the following circuit, the initial voltage of C1 is 5V and C2 is completely discharged. At time t=0 the switch closes. What is the final voltage of C1 or C2 after closing the switch?

$f = \times 10^{-15}$

$V_{i_1} = 5V @ C1$

$V_{i_2} = 0V @ C2$



$Q = CV$ ✓

$Q_i = C_1V_1 + C_2V_2$

$Q_f = V_f(C_1 + C_2)$ ✓

$Q_i = (200f)(5V) + \cancel{(150f)(0)}$

$Q_i = 1000fV$

$Q_i = Q_f$

$1000fV = V_f(200f + 150f)$

$1000fV = V_f(350f)$

$V_f = \frac{1000fV}{350f}$ ✓

$\boxed{V_f = 2.857V}$

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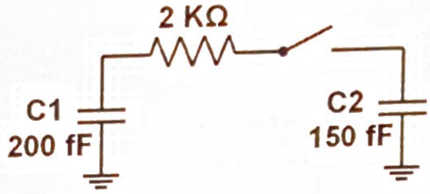
3. (15 points) Now assume that there is an additional 2K resistor in the circuit of problem 2, as shown below. Considering the same conditions in problem 2, what is the final voltages of C1 and C2 after closing the switch?
Also, how much energy is consumed in the 2KΩ resistor after the switch closes?



$$E = \frac{1}{2}CV^2$$

$$E_1 = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2$$

$$E_f = E_1$$

$$E_1 = \frac{1}{2}(200f)(5^2 V) + \cancel{\frac{1}{2}(150)(0)^2}$$

@ $t = 0^-$

$$E_1 = 2500f$$

$$\boxed{E = 2.5pJ}$$

Need $t = 0^+$

$t = 0^+ \begin{cases} E_{c_1} = \frac{1}{2}(200)(2.85 \\ E_{c_2} = \frac{1}{2}(150)(2.85 \end{cases}$

Take diff:
$2.5 - 1.428 = 1.07pJ$

15

$\frac{10N_A \cdot 10N_D}{n_i^2}$ $\frac{n_i^2}{N_A \cdot N_D}$

4. (15 points) The doping concentration of both N and P sides of a diode increases by factor of 10X each. Compute the amount of increase in the built-in potential due to this doping concentration change.

Hint: The equation for the built-in potential in a PN junction is $V_{bi} = V_{th}Ln(\frac{N_A \cdot N_D}{n_i^2})$,

where V_{th} is ~26mV.

$N'_A = 10N_A$
$N'_D = 10N_D$

$$V'_{bi} - V_{bi} = \Delta V_{bi}$$

$$(26 \times 10^{-3}) \ln\left[\frac{10N_A \cdot 10N_D}{n_i^2}\right] - (26 \times 10^{-3}) \ln\left[\frac{N_A \cdot N_D}{N_i^2}\right]$$

$$(26 \times 10^{-3})\left[\ln\left(\frac{10N_A \cdot 10N_D}{n_i^2}\right) - \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)\right] \text{ (log rules)}$$

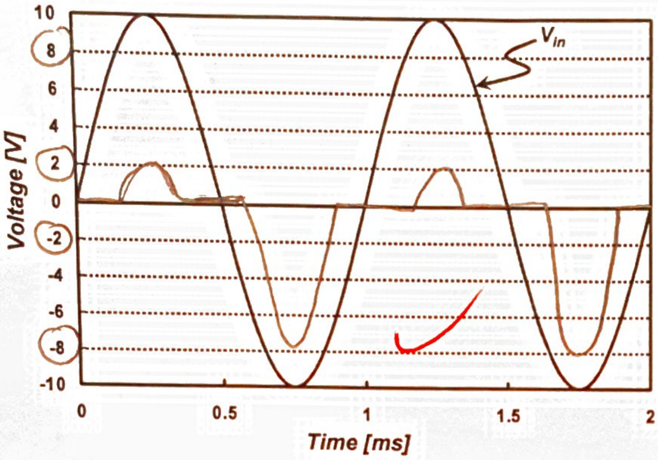
$$(26 \times 10^{-3})\left(\ln\left[\frac{\frac{10N_A \cdot 10N_D}{n_i^2}}{\frac{N_A \cdot N_D}{n_i^2}}\right]\right) = (26 \times 10^{-3})(\ln(100))$$

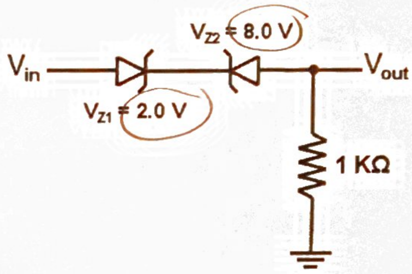
$$= 0.1197$$

$$\approx \boxed{120mV}$$

10

5. (10 points) Assume that the input voltage (V_{in}) in the following circuit is a sine wave shown in the diagram below. Draw the output voltage (V_{out}) on the wave diagram. Explain the state of zener diodes at each region. Assume that the forward bias voltage and the reverse bias current of zener diodes are negligible ($V\gamma \approx 0V$, $I_S=0$).





$V_{DS} \overset{?}{\gtrless} V_{GS} - V_T$

15

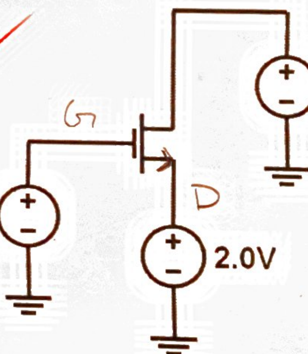
6. (15 points) In the circuit below, assume that the NMOS has K'_n=100uA/V², (W/L)=10, and V_T=1V. Ignore the channel length modulation.

(a) Identify Source, Gate, and Drain terminals.

(b) Find the region of operation.

(c) Determine I_{DS}.

D > S in Nmos



(a) Drawn on Circuit

(b) $V_{GS} = V_G - V_S = 3 - 1 = 2$

$V_{DS} = 2 - 1 = 1$

$1 \gtrless 2 - 1 \quad (V_{DS} \lesseqgtr V_{gs} - V_T)$

$\Rightarrow \quad 1 = 1$

∴ It can be either Linear or Saturated.

(c) $I_{DS} = K_n'\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$

$I_{DS} = (100\mu)(10)\left[(2-1)\,1 - \frac{1^2}{2}\right]$

$I_{DS} = (100\mu)(10)(0.5) = \frac{1000\mu}{2} = 500\mu$ $\times 10^{-6}$

$\boxed{I_{DS} = 5 \times 10^{-4} A \text{ OR } \cancel{.05 mA}}$

20

7. (20 points) A power supply is designed using a bridge diode (full wave rectifier). The transformer is 120 V / 24 V and the filter capacitor is 5,800 μF. Assume V_{ON}=0.7V for the diodes. If the ripple voltage at the load is 2V, then determine:

(a) The peak voltage at the load.

(b) The average DC voltage at the load ($V_{average}=V_{Peak}-V_{ripple}/2$).

(c) The average DC current at the load.

(d) The resistance of the load.

(e) The average load power dissipation.

$V_p = 24\sqrt{2}$

a) $V_{peak} = \boxed{33.941V}$

$V_{DC} = V_p - \frac{V_{rip}}{2}$

$V_{DC} = 33.941 - 1$

b) $32.54 - 1 = \boxed{32.941V}$

c) $C = \frac{I}{f(V_R)} = I = C(f)(V_R) = (5800\mu)(120)(2)$

$= 1.392A$

d) $R_L = \frac{V_P}{V_R}\left(\frac{1}{fC}\right) = \left(\frac{33.941}{2}\right)\left(\frac{1}{(120)(5800\mu)}\right)$

$= \boxed{24.38\Omega}$

e) $P = 32.941(1.392) =$

$= \boxed{45.853W}$