University of New Mexico

Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2018) — Final Exam

Name: _____ Date: Dec. 10, 2018

Note: Only calculator, pencils, and pens are allowed.

1. (10 points) True or false:

(a) A diode is forward bias if its current flows from Anode to Cathode. ( )

(b) A bridge rectifier is a half-wave rectifier that contains four diodes. ( )

(c) In a PMOS the Drain has higher potential that the Source. ( )

(d) Due to DIBL effect, increasing the Drain voltage results in an increase in threshold voltage of an NMOS. ( )

(e) Because of the threshold voltage roll-off, the threshold voltage of a long channel NMOS is higher than that of shorter channel NMOS. ( )

(f) The fanout of a 2X inverter driving two 1X inverters is 1. ( )

(g) Setup time is the amount of time that the data must be stable after the rising edge of the clock. ( )

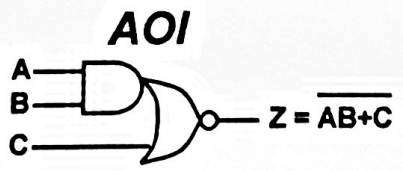
(h) Hot electrons are the high energy electrons that get stuck into the gate oxide close to the Source side. ( )

(i) The longest path in a VLSI circuit is called critical path. ( )

(j) The hold time constraint in a digital system can be relaxed by reducing the clock frequency. ( )

2. (5 points) Draw the logic gate implementation of an AOI gate, ***using NAND gates only***.

Hint: Start with the circuit diagram below and convert all gates to NAND gates.

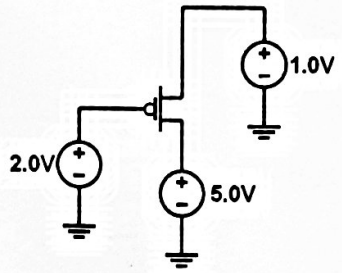


3. (10 points) In the circuit configuration below:

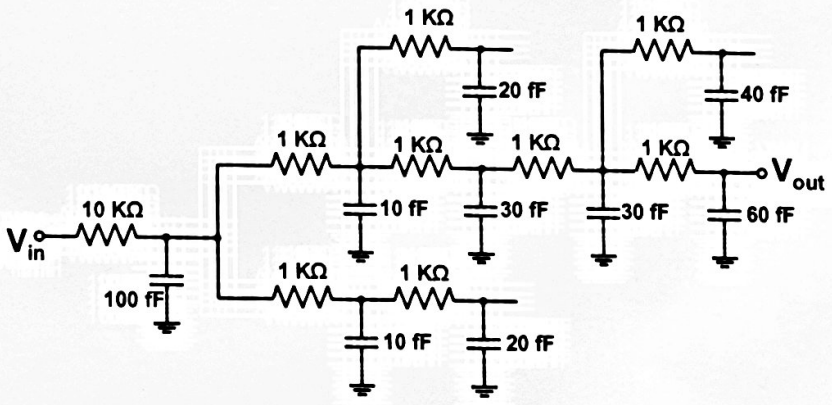
(a) Identify Drain and Source terminals assuming that the device is a PMOS.

(b) Identify the region of operation for the PMOS.

(c) Determine the drain current if $V_{Tp} = -0.4v$, $K'_p = -65\mu A/v^2$, $(W/L) = 20$, and $\lambda_p = -0.2v^{-1}$.



4. (10 points) The following RC network is the equivalent circuit of an interconnect network in a VLSI chip. Using Elmore delay, compute the **propagation delay** from V_{in} to V_{out}.

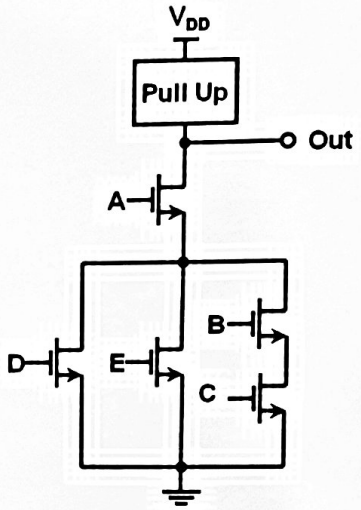


5. (10 points) Consider the given pull-down network for a complex CMOS gate shown below.

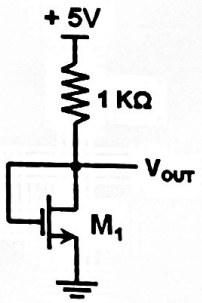
(a) Draw the dual pull up network.

(b) Write the Boolean function representing the gate.

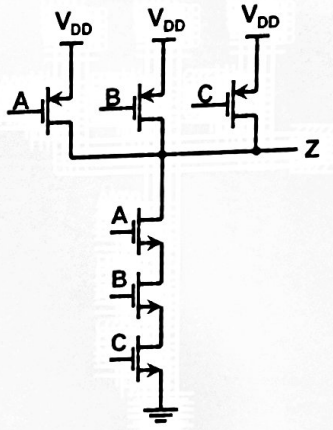
(c) Size all transistors so that it has the same delay of a standard inverter (i.e. 1X NMOS and 2X PMOS).



6. (10 points) In the following circuit, find V_{out}. Assume that $(W/L)_n=20$, $V_{DD}=5$ V, $K'_n=100$ uA/V^2, $V_{tn}=0.5$ V.



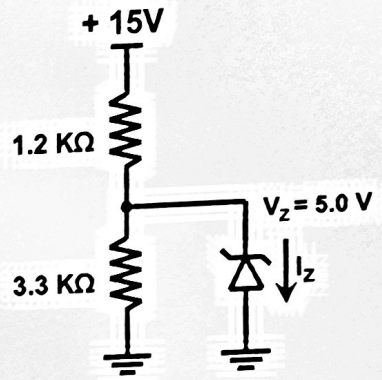
7. (10 points) Determine the switching threshold voltage, V_M, of the three input NAND gate when all the inputs are tied together. Assume that $(W/L)_n$=15, $(W/L)_p$=10, V_{DD}=1.2 V, K'_n= 95 uA/V^2, V_{tn}= 0.3 V, K'_p= 50 uA/V^2, and V_{tp}= -0.4 V in the 100nm technology node.



8. (5 points) Determine the maximum I_{DD} current for the three input NAND gate of problem 7.

9. (10 points) Find the current of the Zener diode, I_Z, in the following circuit.

Hint: Assume that the Zener diode is in breakdown condition.

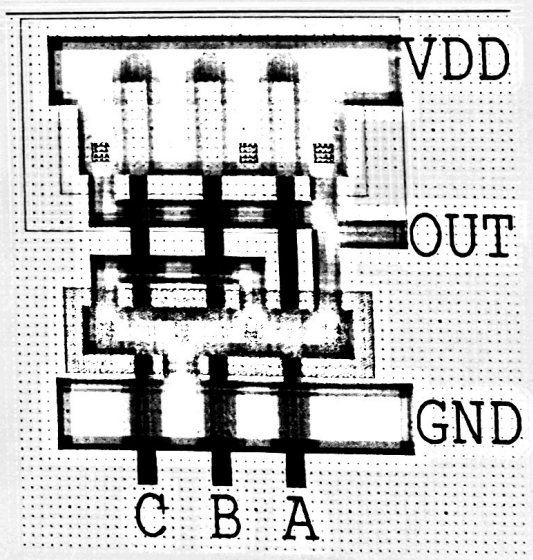


10. (10 points) The layout of a logic gate is shown below.

(a) Draw the transistor schematic.

(b) What logic function does this perform?

(c) This layout is not complete. What is missing in this layout?



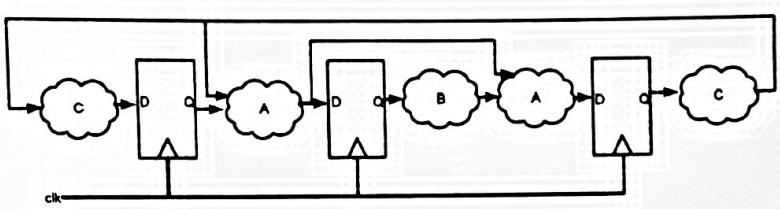
11. (10 points) Consider the following sequential circuit with 3 edge-triggered flip-flops and logic blocks A, B, and C. Assume that t_{SU} = 3ns, t_{hold}= 4ns, and t_{C2Q} = 2ns.

(a) Identify all possible paths from Q to D of any flip-flop in this circuit. For logic block A, assume that the delay is the same for both inputs.

(b) If $T_{Logic,A}$ = 3ns, $T_{Logic,B}$ = 4ns, and $T_{Logic,C}$ = 3ns, identify the longest and the shortest path delays.

(c) What is the maximum clock frequency at which the circuit can operate correctly?

(d) Does this circuit satisfy the hold time constraint? Why?



12. (5 bonus points) In this course, you have spent several hours to design the layout of a 2-input multiplexer from scratch. Give 3 important things that you learned by working on this project.