University of New Mexico

Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2018) Exam #2

Name: _____ Date: Nov. 5, 2018

Note: Only calculator, pencils, and pens are allowed.

1. (10 points) Fill in the blank:

(a) To decrease t_{pHL}, the NMOS threshold voltage must be _____.

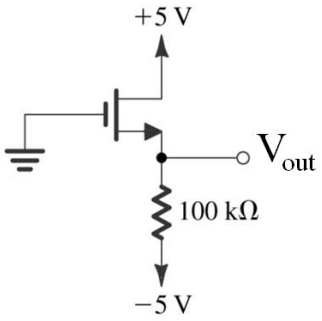
(b) A 10% reduction in power supply voltage reduces the dynamic power dissipation by _____.

(c) By definition rise time is the time it takes for the output to go from _____ to _____.

(d) The propagation delay in an RC circuit, when R=15KΩ and C=12PF is _____.

(e) The dynamic power of an inverter driving a 10PF capacitor at 1GHz when V_{DD}=3.3V is _____.

2. (15 points) For the following NMOS circuit, find V_{out}. Assume that K'_n=100uA/V^2, (W/L)=5, V_T=0.8V, and λ=0.

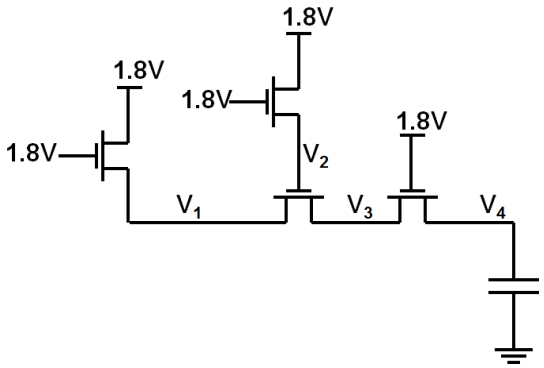


3. (15 points) We would like to design a CMOS inverter such that the switching threshold voltage, V_M, becomes $V_{DD}/2$. Determine the (W/L) ratio of PMOS if the (W/L) ratio of NMOS is 10. Let V_{DD}=5V, V_{Tn}=1.2V, K'_n=100 μA/V^2, λ_n=0.1 V^{-1}, V_{Tp}=-1V, K'_p=60 μA/V^2, λ_p=-0.2 V^{-1}. Include the channel length modulation effect into your calculations.

4. (10 points) Determine the peak power supply current, I_{DDMax}, of the inverter that you designed in Problem 3.

5. (20 points) The slope of the VTC of a CMOS inverter is g=12 and its switching threshold voltage, V_M, is 1.5V. If V_{DD}=3.3V, determine V_{OH}, V_{OL}, V_{IL}, V_{IH}, NMH, and NML of this inverter.

6. (15 points) Assume that the voltage of all nodes in the following circuit start at 0V. Determine the final voltage of nodes V_1, V_2, V_3, and V_4. Let V_{tn}=0.8V and ignore body effect.



7. (15 points) We would like to design a CMOS inverter such that it gives a symmetric rise and fall propagation delay, *i.e.* $t_{PHL}=t_{PLH}$. Determine the (W/L) ratio of the PMOS if (W/L) ratio of the NMOS is 10. Let $V_{DD}=5V$, $V_{Tn}=1.2V$, $K'_n=100\ \mu A/V^2$, $\lambda_n=0.1\ V^{-1}$, $V_{Tp}=-1V$, $K'_p=60\ \mu A/V^2$, $\lambda_p=-0.2\ V^{-1}$. Include the channel length modulation effect into your calculations for saturation current only.

Hint: You don't need the value of the load capacitance, C_L, to solve this problem.