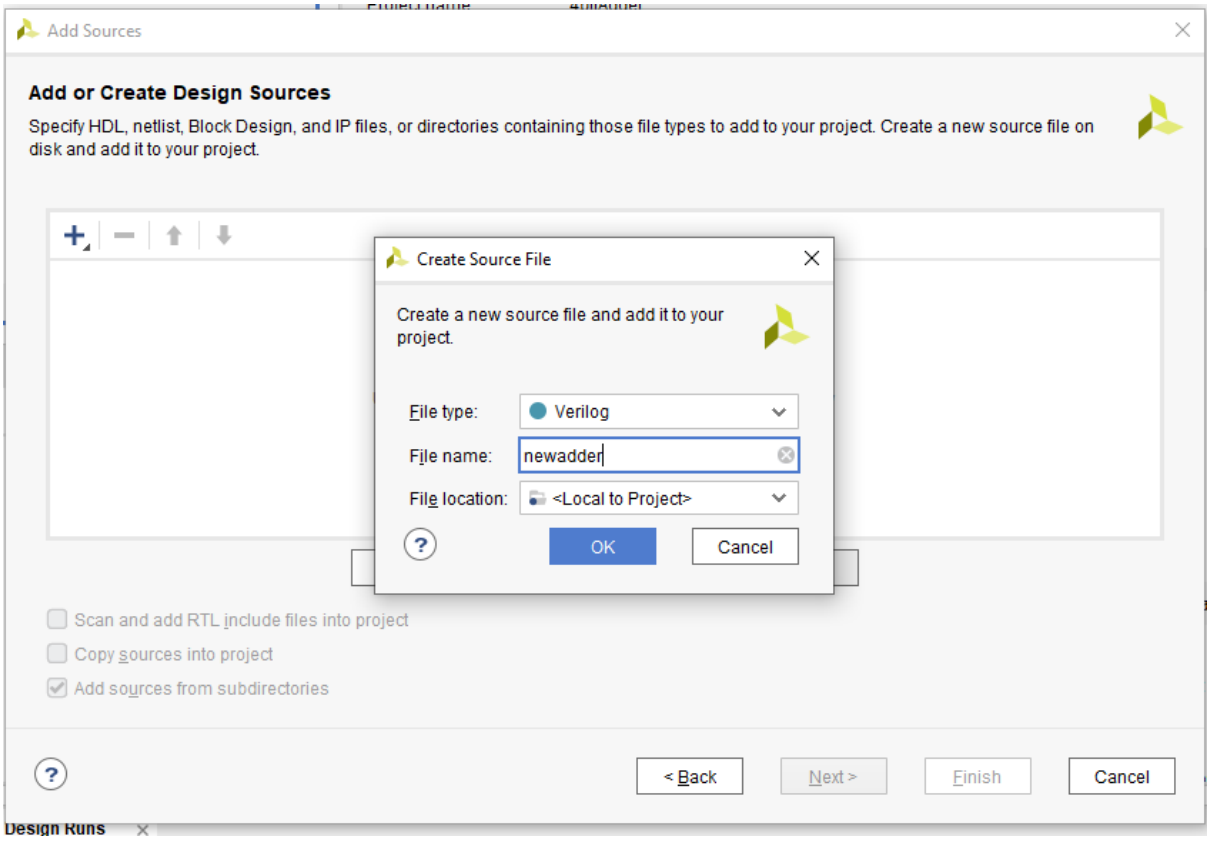
4-Bit Adder

- Created the new project
- Added Sources

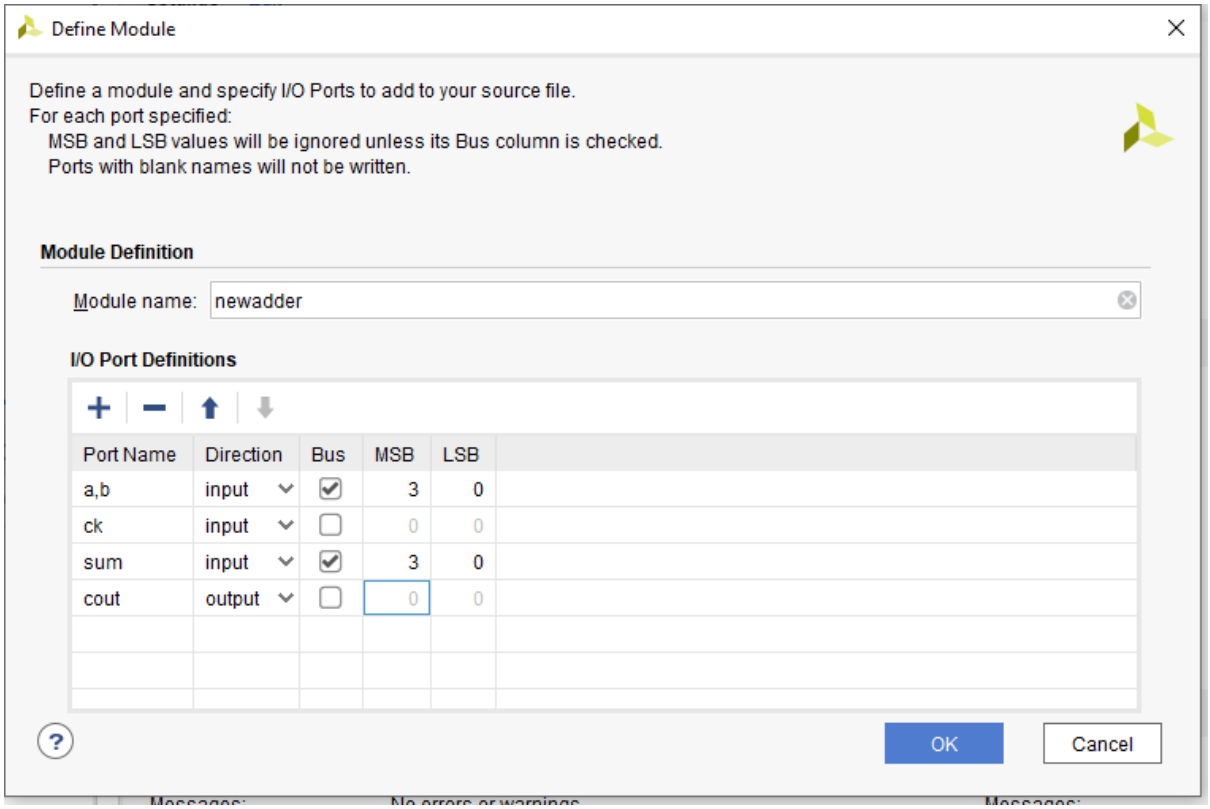


- Defined modules

  module name: new adder

  Port name: Input : a=> msb=3, b, clk

  Output : s(sum) => msb=3, cOut (carry out)



Below is the created design adder in Verilog

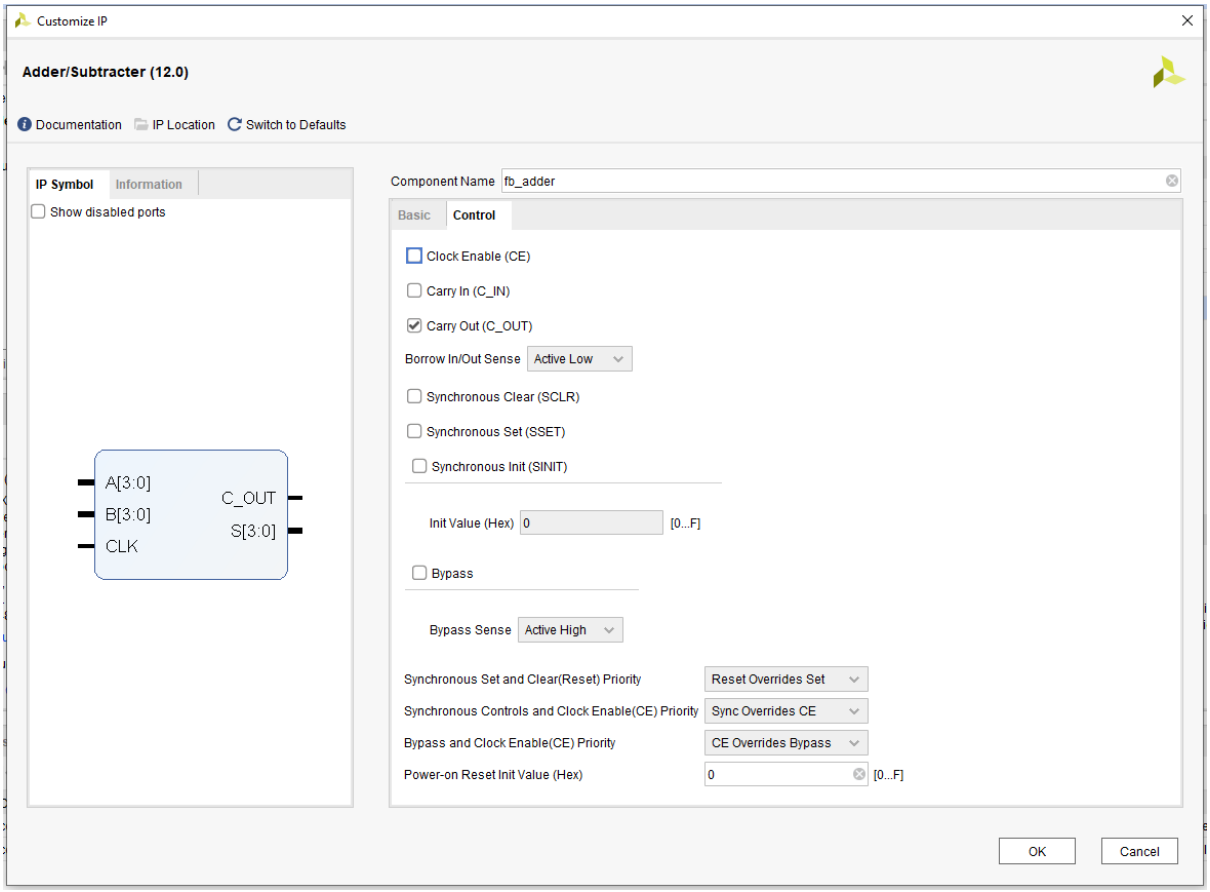
Project Summary | newadder.v

D:/Microblaze_FPGA/LABS/fb_adder/fb_adder.srcs/sources_1/new/newadder.v

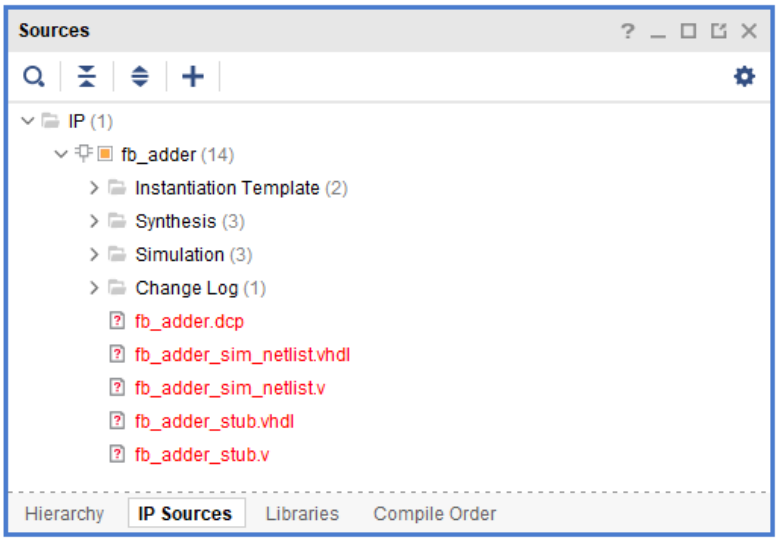
```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 01/30/2024 12:09:48 PM
7  // Design Name:
8  // Module Name: newadder
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module newadder(
24     input [3:0] a,b,
25     input ck,
26     output [3:0] sum,
27     output cout
28     );
29 endmodule
30
```

- Then opened the IP catalog which is already exist in the vivado

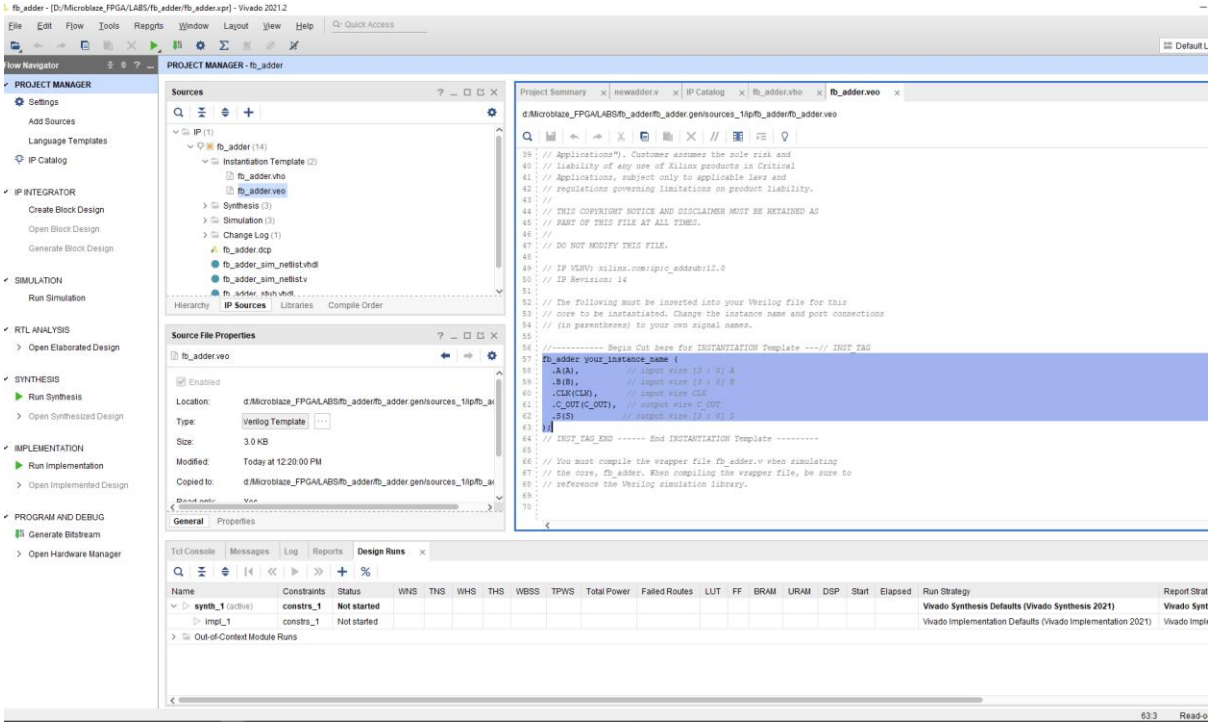
  Changed the types as below picture. (in control tag deselect CE and Enable C_OUT)

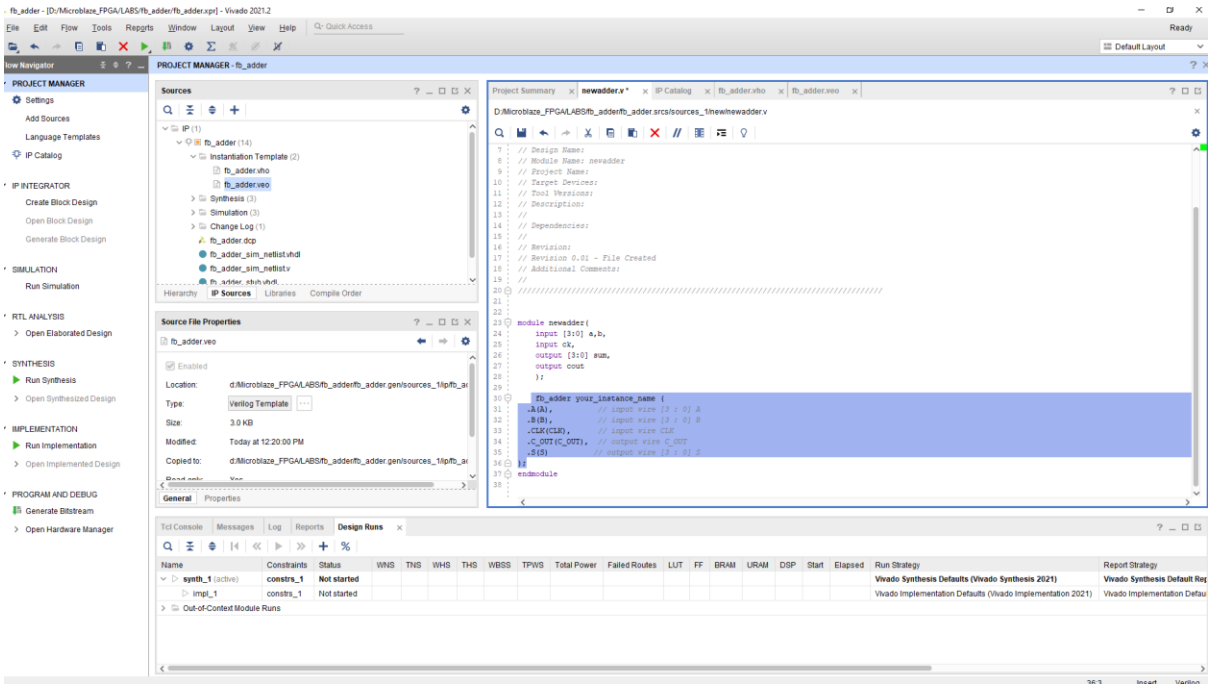


- Then it will create output, the can Generate the output product
- Then we can design can be founded in IP sources

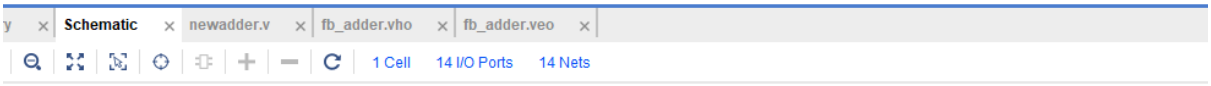


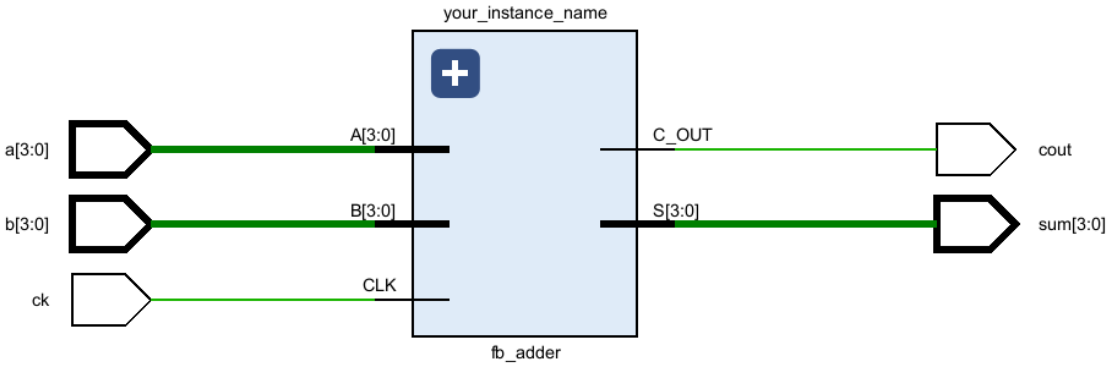
- Now copeid the component to the newadder code.



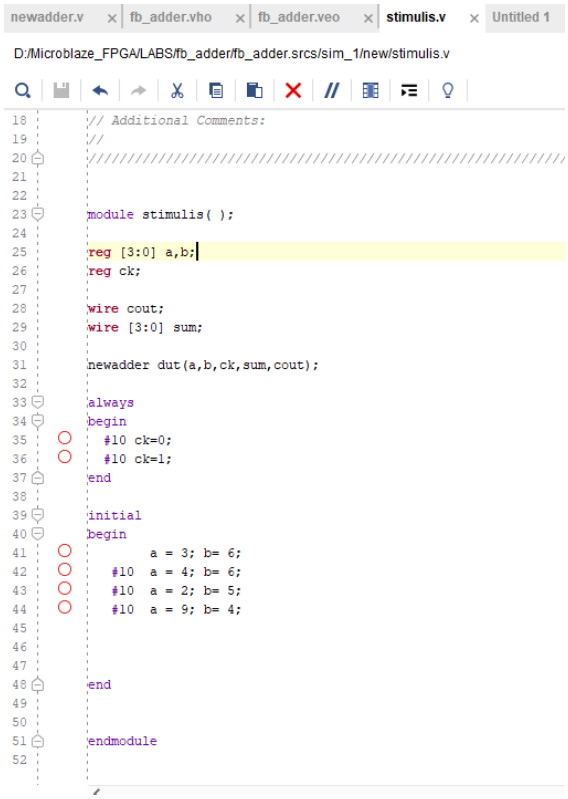


- Rename to cout,ck,sum
- The clicked elaborated design and the schematic is created there

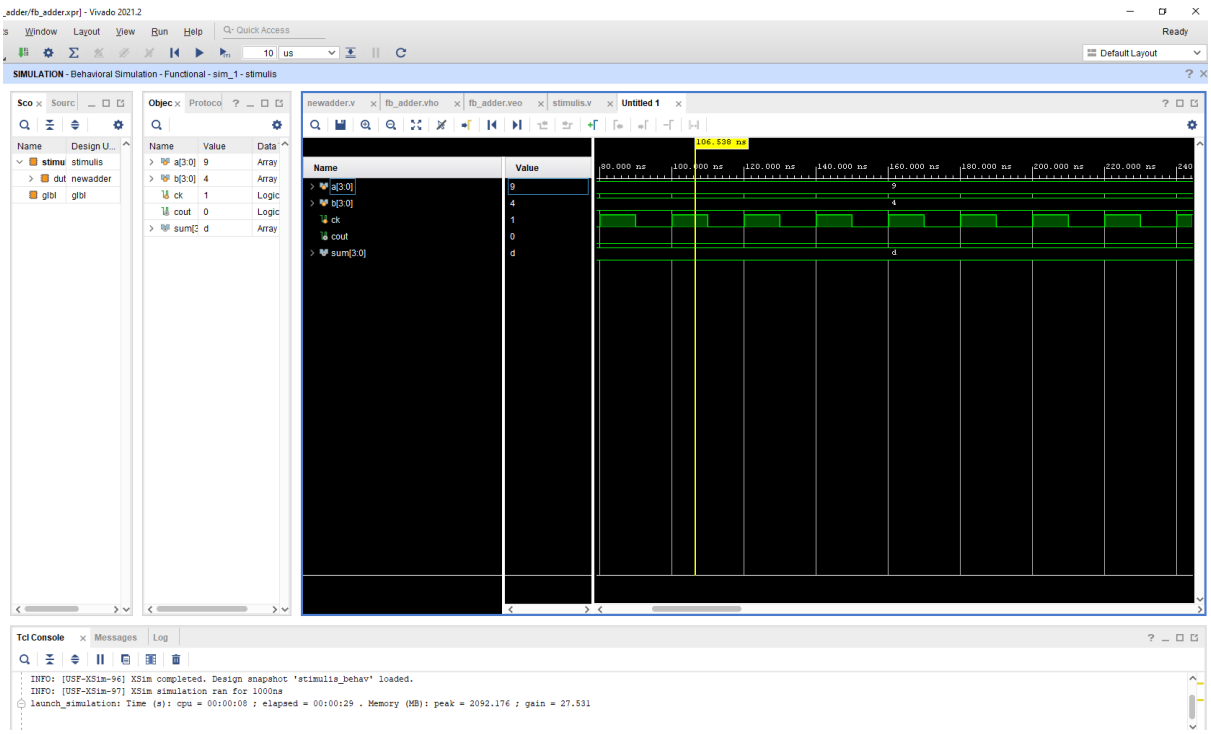




- This design later can be verified with a testbench



- Finally ran the simulation and the lab is successful.



- Additionally checked the synthesis. It was successful

```
23      module stimulis( );
24
25      reg [3:0] a,b;
26      reg ck;
27
28      wire cout;
29      wire [3:0] sum;
30
31      newadder dut(a,b,ck,sum,cout);
32
33      always
34      begin
35        #10 ck=0;
36        #10 ck=1;
37      end
38
39      initial
40      begin
41              a = 3; b= 6;
42        #10   a = 4; b= 6;
43        #10   a = 2; b= 5;
44        #10   a = 9; b= 4;
45
46
47
```