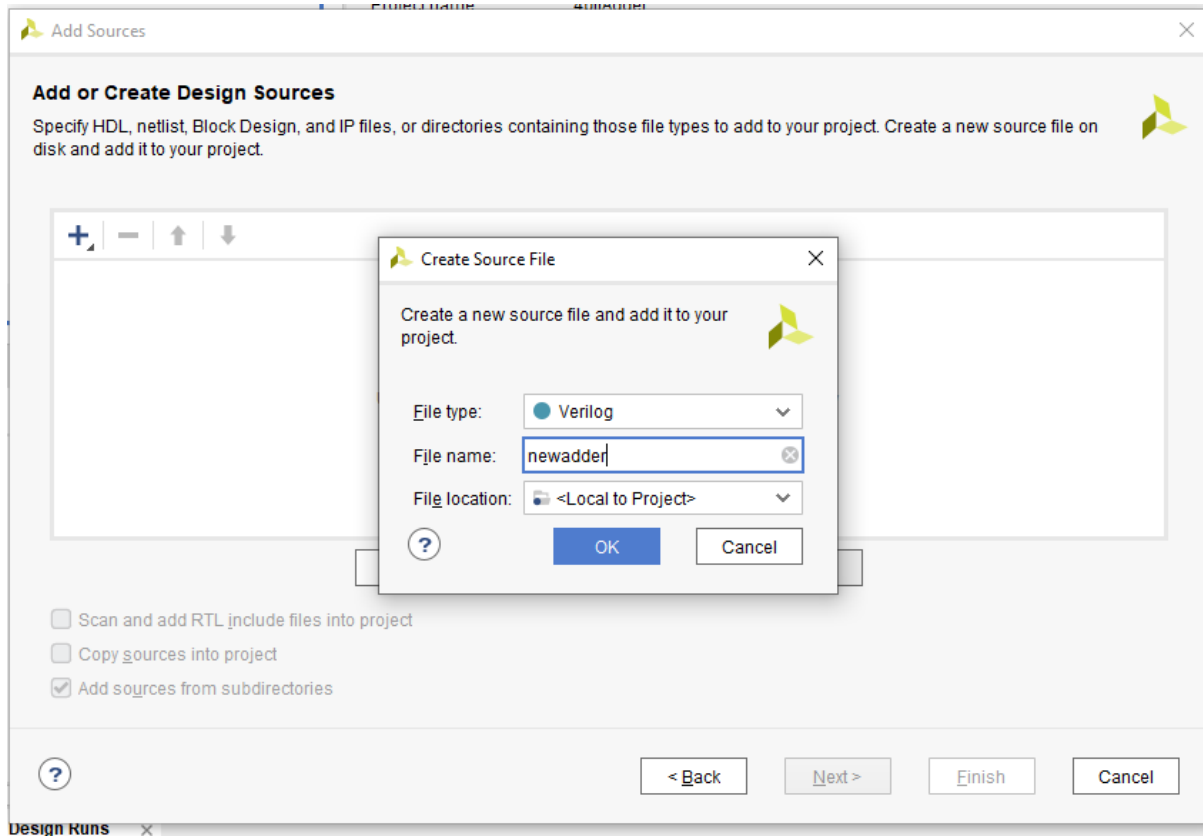


# 4-Bit Adder

- Created the new project
- Added Sources



- Defined modules

module name: new adder

Port name: Input : a=> msb=3, b, clk

Output : s(sum) => msb=3, cOut (carry out)

Define a module and specify I/O Ports to add to your source file.  
For each port specified:  
MSB and LSB values will be ignored unless its Bus column is checked.  
Ports with blank names will not be written.

**Module Definition**

Module name:

**I/O Port Definitions**

Port Name	Direction	Bus	MSB	LSB
a,b	input	<input checked="" type="checkbox"/>	3	0
ck	input	<input type="checkbox"/>	0	0
sum	input	<input checked="" type="checkbox"/>	3	0
cout	output	<input type="checkbox"/>	0	0

OK Cancel

Below is the created design adder in Verilog

Project Summary × newadder.v ×

D:/Microblaze\_FPGA/LABS/fb\_adder/fb\_adder.srscs/sources\_1/new/newadder.v

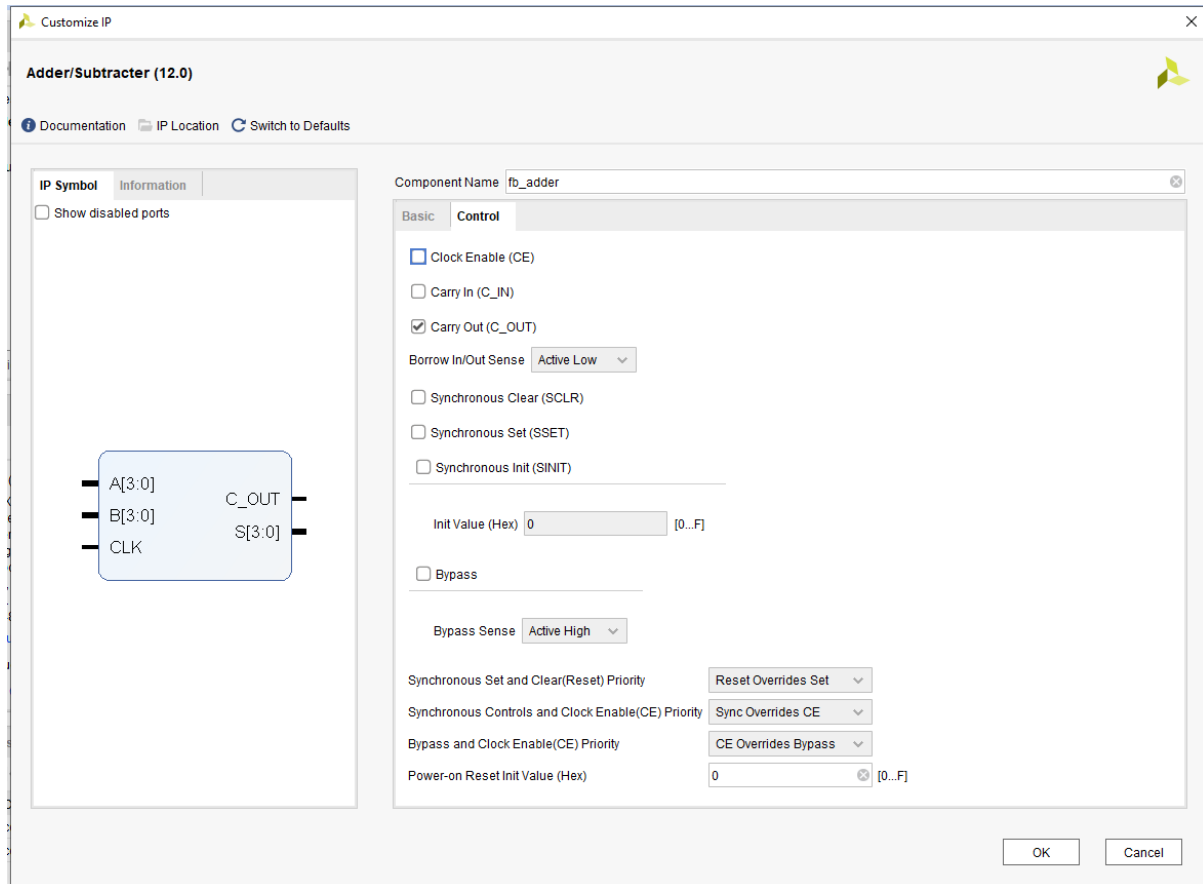
```

1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 01/30/2024 12:09:48 PM
7  // Design Name:
8  // Module Name: newadder
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22
23 module newadder(
24     input [3:0] a,b,
25     input ck,
26     output [3:0] sum,
27     output cout
28 );
29 endmodule
30

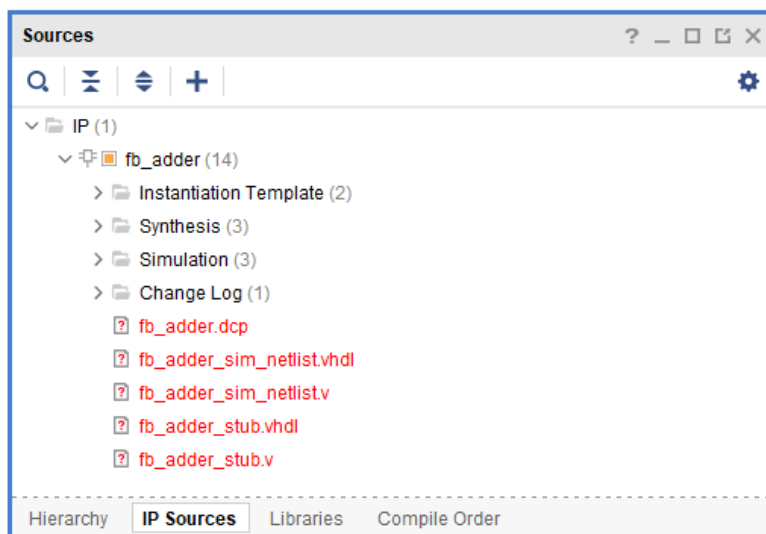
```

- Then opened the IP catalog which is already exist in the vivado

Changed the types as below picture. ( in control tag deselect CE and Enable C\_OUT)



- Then it will create output, the can Generate the output product
- Then we can design can be founded in IP sources



- File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Project Manager - tb\_adder

Project Manager

  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
  - IP INTEGRATOR
    - Create Block Design
    - Open Block Design
    - Generate Block Design
  - SIMULATION
    - Run Simulation
  - RTL ANALYSIS
    - Open Elaborated Design
  - SYNTHESIS
    - Run Synthesis
    - Open Synthesized Design
  - IMPLEMENTATION
    - Run Implementation
    - Open Implemented Design
  - PROGRAM AND DEBUG
    - Generate Bitstream
    - Open Hardware Manager

Sources

IP (1)

  - tb\_adder (14)
    - Instantiation Template (2)
      - tb\_adder.vho
      - tb\_adder.vio
    - Synthesis (3)
      - Simulation (3)
        - Change Log (1)
          - tb\_adder.dcp
          - tb\_adder\_sim\_netlist.vhdl
          - tb\_adder\_sim\_netlist
          - tb\_adder\_synth.vhdl

Hierarchy IP Sources Libraries Compile Order

Source File Properties

tb\_adder.vio

Enabled

Location: d:\Microblaze\_FPGA\LABS\fb\_adder\fb\_adder\gen\sources\_1\tpfb\_3i

Type: Verilog Template

Size: 3.0 KB

Modified: Today at 12:20:00 PM

Copied to: d:\Microblaze\_FPGA\LABS\fb\_adder\fb\_adder\gen\sources\_1\tpfb\_3i

General Properties

Project Summary

newaddiv x IP Catalog x tb\_adder.vho x tb\_adder.vio x

d\Microblaze\_FPGA\LABS\fb\_adder\fb\_adder\gen\sources\_1\tpfb\_3i\adder.vio

```

39 // Applications. Customer assumes the sole risk and
40 // liability of any use of Xilinx products in Critical
41 // Applications, subject only to applicable laws and
42 // regulations governing limitations on product liability.
43 //
44 // THIS COPYRIGHT NOTICE AND DISCLAIMER MUST BE RETAINED AS
45 // PART OF THIS FILE AT ALL TIMES.
46 //
47 // DO NOT MODIFY THIS FILE.
48 //
49 // IP VENDOR: xilinx.com:ip:ic_adder:v1.0
50 // IP Revision: 14
51 //
52 // The following must be inserted into your Verilog file for this
53 // core to be instantiated. Change the instance name and port connections
54 // (in parentheses) to your own signal names.
55 //
56 //----- Begin Cut here for INSTANTIATION Template -----// INST TAG
57 //
58 // Adder: your_instance_name {
59 //   .A(A),           // input wire [3 : 0] A
60 //   .B(B),           // input wire [3 : 0] B
61 //   .CLR(CLR),       // input wire CLR
62 //   .C_OUT(C_OUT),   // output wire C_OUT
63 //   .S(S),            // output wire [1 : 0] S
64 // }
65 // INST_TAG_END ----- End INSTANTIATION Template -----
66 //
67 // You must compile the wrapper file tb_adder.vho when simulating
68 // the core, tb_adder. When compiling the wrapper file, be sure to
69 // reference the Verilog simulation library.
70 //

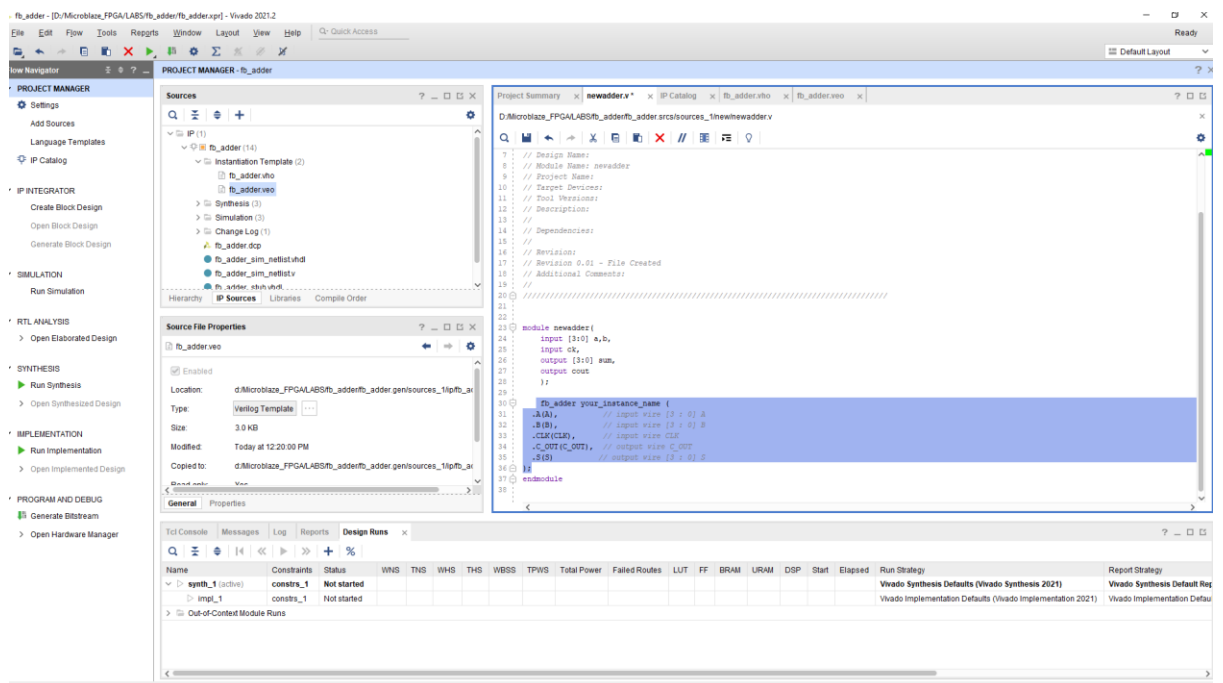
```

Tcl Console Messages Log Reports Design Runs x

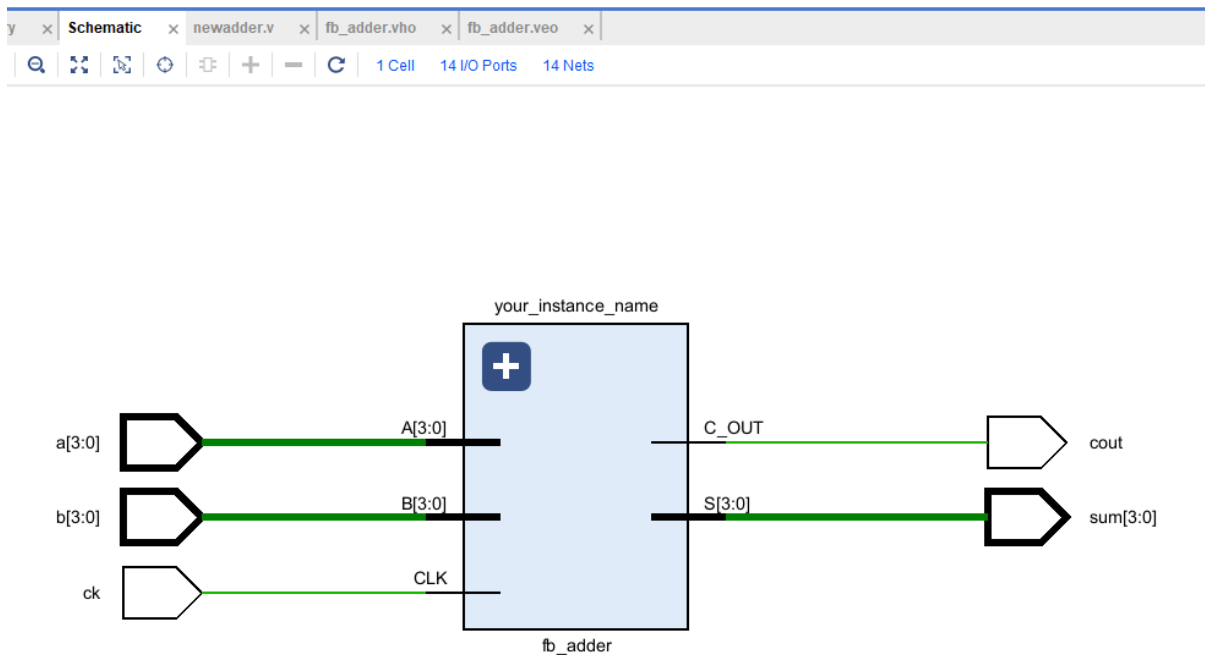
Q Z F I4 << >> >> %

Name	Constraints	Status	VNS	TNS	WHS	THS	WSSS	TPVS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strat
synth_1 (active)	constrs_1	Not started																Vivado Synthesis Defaults (Vivado Synthesis 2021)	Vivado Synth
impl_1	constrs_1	Not started																Vivado Implementation Defaults (Vivado Implementation 2021)	Vivado Impl
Out-Of-Content Module Runs																			

63.3 Read



- Rename to cout,ck,sum
- The clicked elaborated design and the schematic is created there



- This design later can be verified with a testbench

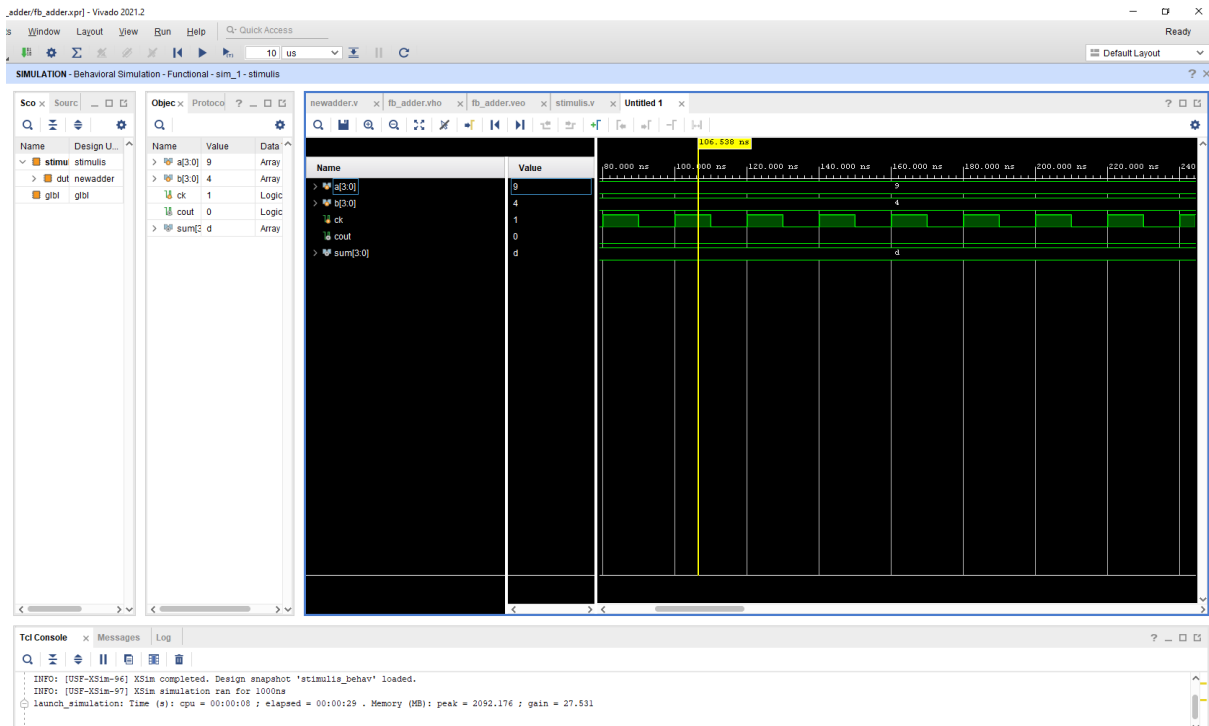
```

newadder.v x fb_adder.vho x fb_adder.v eo x stimulus.v x Untitled 1
D:/Microblaze_FPGA/LABS/fb_adder/fb_adder.srcs/sim_1/new/stimulus.v

18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21
22
23 module stimulus( );
24
25     reg [3:0] a,b;
26     reg ck;
27
28     wire cout;
29     wire [3:0] sum;
30
31     newadder dut(a,b,ck,sum,cout);
32
33     always
34     begin
35         #10 ck=0;
36         #10 ck=1;
37     end
38
39     initial
40     begin
41         a = 3; b = 6;
42         #10 a = 4; b = 6;
43         #10 a = 2; b = 5;
44         #10 a = 9; b = 4;
45
46
47     end
48
49
50
51 endmodule
52

```

- Finally ran the simulation and the lab is successful.



- Additionally checked the synthesis. It was successful

```

23 module stimulus( );
24
25 reg [3:0] a,b;
26 reg ck;
27
28 wire cout;
29 wire [3:0] sum;
30
31 newadder dut(a,b,ck,sum,cout);
32
33 always
34 begin
35     #10 ck=0;
36     #10 ck=1;
37 end
38
39 initial
40 begin
41     a = 3; b= 6;
42     #10 a = 4; b= 6;
43     #10 a = 2; b= 5;
44     #10 a = 9; b= 4;
45
46
47

```

