DESIGN REVIEW CHECKLIST
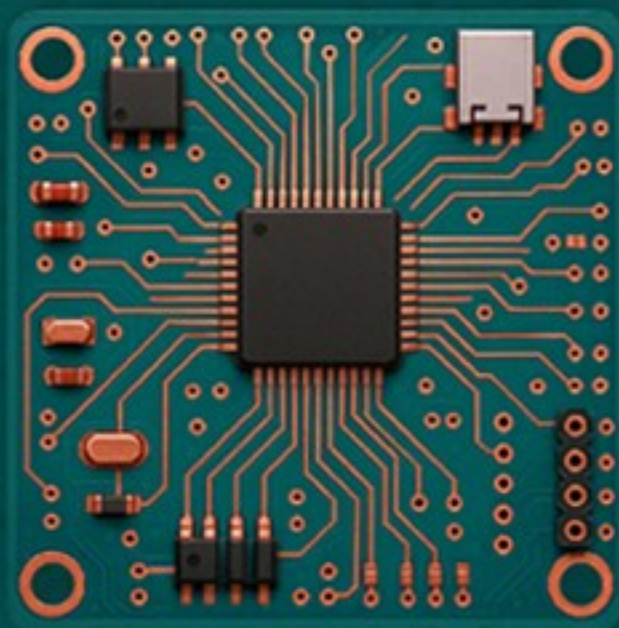
Schematic Circuit

✅ Ensure that there are no missing net ties and schematic ports across all schematic sheets.

✅ Ensure that design rules matching the PCB manufacturer's capabilities have been implemented.

✅ Ensure that all component decoupling capacitors be clearly identified, with a proper note about placement close to the supply pins of the processor.

✅ Add appropriate notes regarding:

    (a) trace width for high current traces

    (b) trace length matching for high-speed traces with matching propagation delay requirements.

    (c) controlled impedance traces, include the expected impedance of such traces.

    (d) traces carrying low noise signals. Indicate that they are to be separated from high current traces or traces carrying fast signals.

    (e) trace separation clearances for high voltage trace. Indicate if physical barriers such as PCB slots are needed.

✅ Properly identify passive components with specific characteristics such as high power or precision resistors, low temperature coefficient, or low ESR capacitors and others

✅ Unused pins on IC's should be confirmed to be no net connection, or pulled up or pulled down.

✅ Check all schematic capture compilation warnings. Do not ignore any unless there is a good reason for doing so.

✅ Ensure the IC outputs such as I2C SDA or SCL have proper pull-up resistors.

- ✔ Ensure the IC outputs such as I2C SDA or SCL have proper pull-up resistors.

- ✔ Ensure that clamp diodes and transient suppressors have been included in all externally exposed connections.

- ✔ If there are different types of Ground, eg. Signal ground or Power ground, make sure to properly label each ground with its type.

- ✔ Identify magnetic components, such as power inductors, that could cross-couple. Make a note about properly spacing, or orienting, them.

- ✔ Identify high heat generating components and temperature sensitive components, and add a note that they are to be properly physically separated.

- ✔ Identify circuit sections that need to be shielded, and indicate the type of shielding, such as cans, needed.

- ✔ Indicate the need of guard rings around very sensitive low-level signal input pins.

- ✔ Do not place high voltage and low voltage lines adjacent to each other on connector pins on the schematic.

- ✔ Use multiple connector pins for carrying high current, taking into account the current carrying capability of each pin of the selected connector.

- ✔ If using PCB heatsink or on-board heatsinks, specify keep-out area.

- ✔ Specify Do-Not-Populate (DNP) components.

- ✔ Add appropriate test points to critical nodes.

- ✔ Specify test point surface treatment, if required.

- ✔ Specify surface treatment, such as gold plating of a given thickness, for

- ✓ Sufficient clearances between high voltage traces.

- ✓ Trace widths are sufficient for traces carrying large currents.

- ✓ Low noise traces do not run too close to high-current traces or high-speed digital traces.

- ✓ For high-speed traces, ensure that line lengths are properly matched. The higher end layout packages have tools to do this.

- ✓ For high-speed traces also run simulations to ensure that there are no violations, including the effects of vias on signal propagation.

- ✓ Consider the effect of ground loops for designs without a proper ground plane.

- ✓ Be aware of the placement and orientation of magnetic components, if any, to avoid cross coupling.

- ✓ For very low-level signals, make sure that the appropriate guard rings are in place.

- ✓ Depending on the frequency of the signal, the typical FR4 substrate may not be suitable, and a low loss, but more expensive, substrate should be considered.

- ✓ Ensure that any RF lines have the proper complex impedance (typically 50 ohms). This includes confirming that a ground layer is underneath the trace (microstrip) and commonly on both sides as well (coplanar waveguide).

- ✓ On-board antennas have the proper ground clearances on all layers.

- ✓ Ground layers have sufficient stitching vias especially near any RF circuits.

- ✓ On-board chip antennas are placed according to the manufacturer's recommendations.

- ✔ If the design includes multiple on-board antennas be sure they are placed so as to maximize their distance to prevent cross interference.

- ✔ Switching power regulators are carefully layed out according to the manufacturer's datasheet.

- ✔ Power supply pins on any IC's have decoupling capacitors placed nearby.

- ✔ No footprint errors it's best to print out the layout at scale, and then physically lay all of the components on the printout to ensure the leads match up properly.

- ✔ Test points are included on all signal traces which aren't easily accessed (i.e. signals between leadless packages).

- ✔ No blind or buried vias are used unless absolutely required. Their use will significantly increase the board cost.

- ✔ Final board dimensions match correctly with the enclosure design.

- ✔ Any crystal connections are kept as short as possible.

- ✔ All components, connectors, jumpers, and test points are properly labeled in the silkscreen layer.

- ✔ No signal traces have 90-degree bends

- ✔ Signal traces don't unnecessarily jump between different board layers. This can also be a sign of auto-routing, which rarely produces a quality design.

- High-current traces are primarily routed on the outside layers.

- ✔ Silkscreen layer includes the proper board part number and the current revision.

- ✅ If required for assembly, confirm that the design includes the necessary fiducial.

- ✅ Polarities are marked for polarized components like some capacitors.

- ✅ Pin 1 is marked on all integrated circuits.

- ✅ Digital and analog sections are kept separated with grounds connected at a single point.

- ✅ Generate a 3D model of the PCB, and make sure that there is no interference with other parts of the device assembly.

- ✅ Design rules match the capabilities of the specific PCB manufacturer.