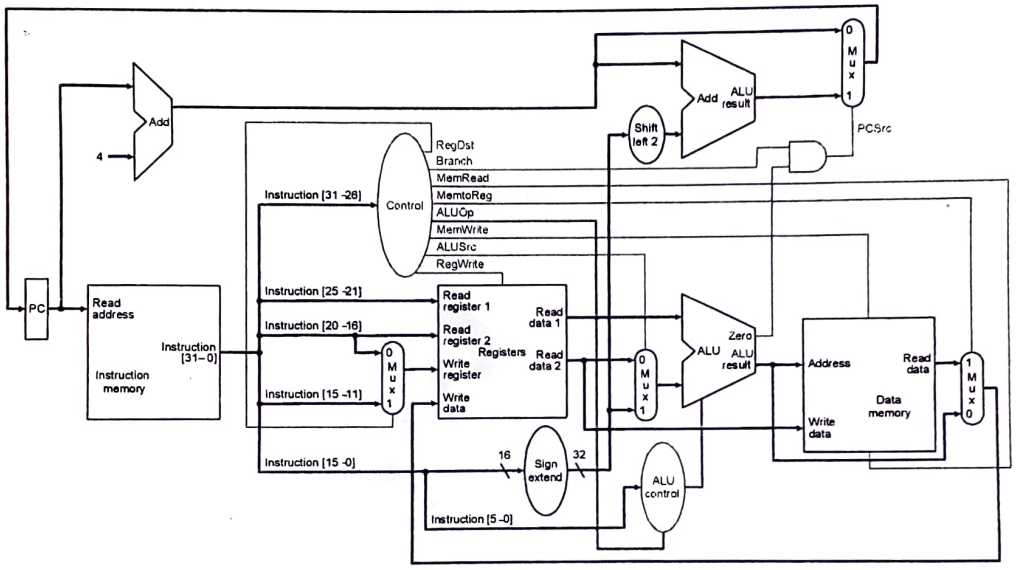
CS 4100: Computer Architecture
Fall 2021, Final Examination
13:20-15:20, Jan. 10, 2022

1. (10%) Consider a pipeline having 4 stages with duration 45, 35, 65 and 55 ns. Let the latch delay be 5 ns. Please calculate: (a) the clock cycle time of the pipeline design (b) the clock cycle time for non-pipeline single cycle implementation.

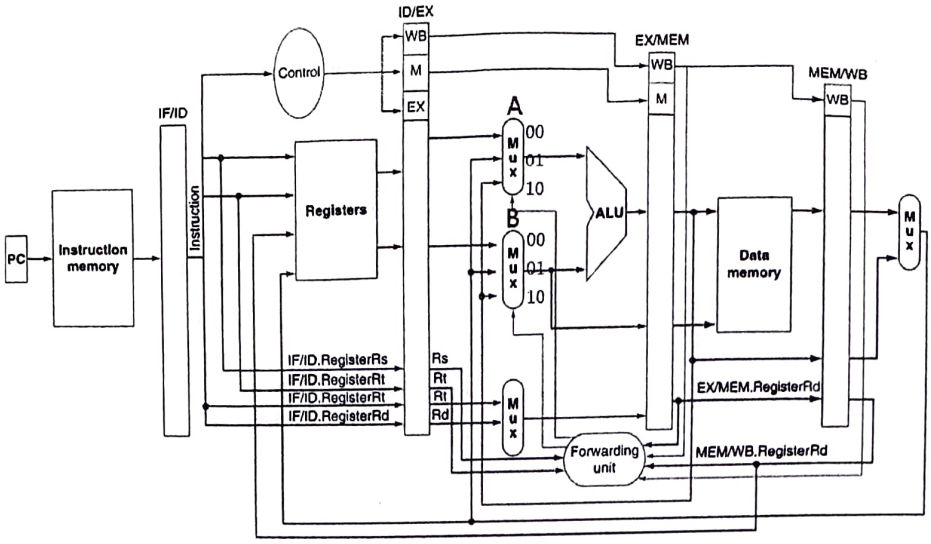
2. (15%) [SINGLE-CYCLE PROCESSOR] Consider the single-cycle data-path shown in the following. Let registers s1 = 5 and s2 = 6. Give the values of the control signals (i.e., ALUSrc, PCSrc, MemRead, MemToReg, MemWrite, RegDst, RegWrite) when executing (a) lw $t4, 20($t3) (b) beq $s1, $s2, loop (c) add $s3, $s3, $s4?



3. (10%) Consider three branch prediction schemes: predicting not taken, predicting taken, and dynamic prediction. Assume that they have no penalty when predicting correctly and 2 cycles when making wrong prediction. Assume that the average predict accuracy of the dynamic predictor is 85%. Which predictor is the best choice for the following cases? (A) Branches are taken 80% (B) Branches are not taken 90% (C) Branches are not taken 13%.

4. (10%) (6%) Explain what memory hierarchy is and (4%) why it works?

5. (10%) We need page table to implement the page translation in virtual memory system. (a) what are the two problems of page table if we implement it simply in main memory. (b) for each problem, name one strategy to solve the problem.



6. (15%) [PIPELINE DESIGN] Given a 5-stage pipelined data-path shown as above where register-read is performed at the second stage, ALU computation the third stage, memory read/write the fourth stage and register write the fifth stage. Consider the following code segment:

IF ID EX MEM WB

```
addi $s0, $s1, 10
sub  $s1, $s2, $s3
lw   $s4, 4($s1)
addi $s5, $s4, -10
```

IF ID EX MEM WB

IF ID EX MEM WB

IF ID EX MEM WB

IF ID EX MEM WB

(a) (5%) Without forwarding: Solve the data hazards by inserting NOP.

(b) (10%) With forwarding: Indicate in which cycle each of the following conditions is true for the 5-stage pipelined processor:

(i) Forward from EX/MEM pipeline register to ALU input

(ii) Forward from MEM/WB pipeline register to ALU input

7. (8%) True or false. Justify your answer.

(a) DRAM is used to build cache.

(b) Cache miss is handled by software while page fault by hardware.

(c) On write miss, write back policy will always fetch the block, while write through policy may or may not fetch the block.

(d) Increasing clock rate of CPU will also improve CPU cycles of memory stalls in a pipeline design.

8. (10%) The Average Memory Access Time equation (AMAT) has three components: hit time, miss rate, and miss penalty. For each of the following cache optimizations, indicate which component of the AMAT equation is improved.

hit time + miss rate × miss penalty

(a) Using a second-level cache

(b) Using a direct-mapped cache

(c) Using a 4-way set-associative cache

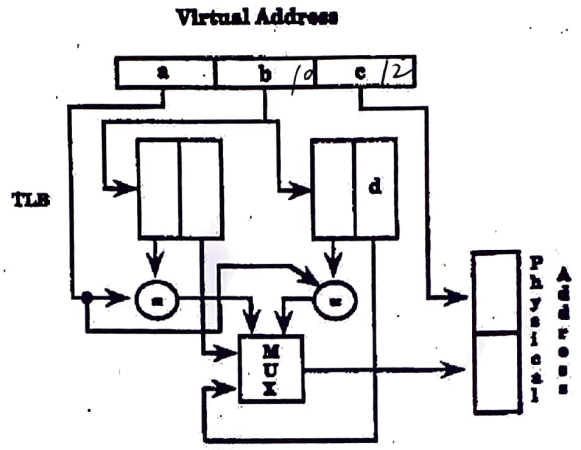
(d) Using a larger cache

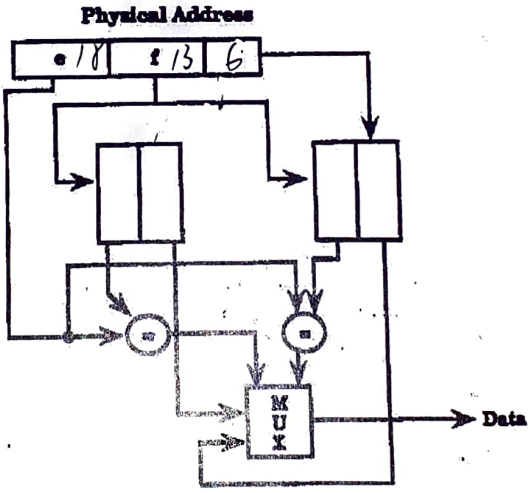
(e) Using larger blocks

9. (12%) [MEMORY DESIGN] Note: B= Byte

Virtual address 34 bits
TLB 2-way set associative with 512 total entries
4KB page size
Physical address 36 bits
Total data cache size = 512 KB
Data cache block size = 64B
2-way set associative data cache

Let the memory be byte addressable. Show the size of the labeled fields, a, b, c, d, e, f.





Cache