Computer Architecture

Fall, 2022

Week 11

2022.11.21

組別： _____

簽名： _____

◆ [group2]

Please choose the correct answer

√ a. One step of designing a pipeline is to partition datapath into many stages

√ a. Pipeline uses additional registers to store some data and control signal

a. Pipeline rate limited by ~~fastest~~ longest stage

√ a. Structural hazard means to attempt to use the same resources in two different ways at the same time

√ a. Pipeline increases the throughput of entire processor

~~√~~ X a. Some functional unit can be used at the ~~different~~ same stage for all instructions

Ans:

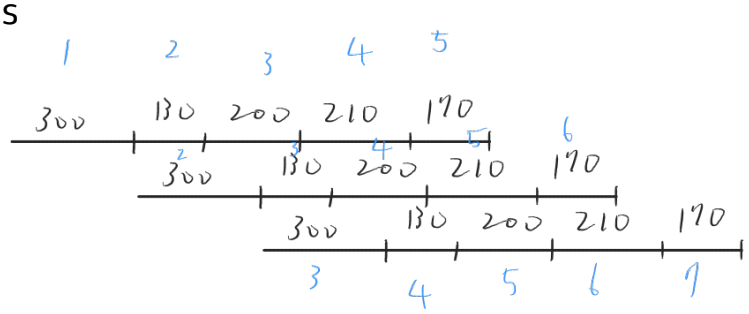
◆ [group6]

There is a processor A have following latency for each stage ：

processor \ stage	Ins. fetch	Reg / Dec	Execution	Memory access	Write back
A	300 ps	130 ps	200 ps	210 ps	170 ps

Please give the answer of single cycle time and execution time for following instructions

lw $1,100($0)
lw $2,200($0)
lw $3,300($0)



1. A is a non-pipeline processor
2. A is a pipeline processor

Answer :

1、 (300+130+200+210+170) x3 = 3036 ps

2、 300+300+300+210+210+210+170 = 1700 ps

300x7 = 2100 ps

clock time 固定

◆ [group14]

Please write the logic equation of the following control signals using the given opcode(op[5:0]).

	add/sub	lw	sw	beq
op	00 0000	10 0011	10 1011	00 0100
1.MemWrite	0	0	1	0
2.ALUsrc	0	1	1	0

ans:

1、Memwrite: sw = $op5 \cdot op4' \cdot op3 \cdot op2' \cdot op1 \cdot op0$

2、ALUsrc: lw + sw = $op5 \cdot op4' \cdot op3' \cdot op2' \cdot op1 \cdot op0$

+ $op5 \cdot op4' \cdot op3 \cdot op2' \cdot op1 \cdot op0$

◆ [group13]

Please choose the correct answers.

(A) Pipeline can increase throughput for a list of instructions.

(B) Pipeline can decrease response time for a single instructions.

(C) ALUSrc can be presented by binary logic equation as

ALUSrc = op5·op4'·op3'·op2'·op1·op0 (lw) +op5·op4'·op3·op2'·

op1·op0 (sw)

(D) The speedup is limited by the time of the slowest stage.

(E) Consider a pipelined processor with K stages. Now we want to execute N instructions. The number of clock cycles we need is (K -1) +N.

(F) Allowing jumps, branches, and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance.

Ans: A、C、D、E

B. Response time for each instruction does not decrease because pipeline doesn't help latency of single task

F. The structural hazards may happen

◆ [group12]

Datapath can be partitioned into several stages. Please organize the steps with correct order for 4 instructions and calculate the total number of stages for each instruction.

(a) Instruction fetch
(b) Instruction decode
(c) Write the data back to the register file
(d) Execution
(e) Read/write data in Data Memory

1. Load abdec
2. R-type abdec
3. Beq abd
4. Store abde

Ans.

◆ [group4]

Please select the correct statement

a. ALUop requires 2 bits, 00, 01, 10 for R-type, lw/sw, beq respectively.
b. ALUctr2 = ALUop0 + ALUop1*func2*func1*func0'
c. We don't care MemtoReg when the instruction is sw or beq, since RegWrite is 0.
d. RegDst = op5'*op4'*op3'*op2'*op1'*op0'
e. To add jump instruction, it doesn't need an extra control.

Ans:

◆ [group9]

Please select all correct answers, and explain if it is false

(a) we can increase the throughput by pipelining because the latency of each instruction is shortened 不會變

(b) the concept behind pipeline is to increase hardware utilization

(c) in order to divide our MIPS datapath into 5 stages, adding 4 pipeline registers to original structure is needed

(d) CISC is usually easier to pipeline compared to RISC

(e) it will take at least N-1 clocks to fill our pipeline with N stages

false

(f) one of the possible solutions of structural hazard is duplicating the resource

(g) pipeline with more stages always has better performance

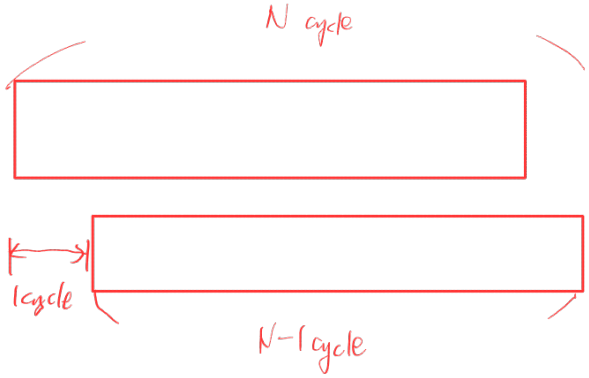
(h) there are always multiple instructions in pipeline

single

ANS:

(d) CISC 指令較複雜

(e)



(f) 不一定 可能 cycle 變長

(h) 不一定