Computer Architecture

Fall, 2022

Week 5

2022.10.17

組別：_________

簽名:____

◆ [group2]

The execution of the procedure needs to follow accurate steps. There are six steps showing below, please organize the steps with correct order.

(a)Putting the result values in the registers that caller is able to access
(b)Transferring control to the procedure
(c)Performing the main task of the procedure
(d)Putting parameters in the registers where the procedure can access
(e)Returning control to the place where procedure was called
(f)Acquiring storage for procedure (saving the values of $s0 to $s7 in memory)

Ans：

d→b →f→c→ a→ e

◆ [group14]

Instructions	Memory Location	opcode	rs	rt	rd	shamt	funct
					immediate / offset		
			address				
lw $t0, 0($s0)	59996	35	19	9	0		
Loop: andi $t1, $t0, 1	60000	8	9	8	1		
add $s1, $s1, $t1	60004	0	17	9	17	0	32
srl $t0, $t0, 1	60008	(a)	0	9	9	(b)	2
beq $t0, $t0, Exit	60012	4	9	9	(C)		
j Loop	60016	2	(d)				
Exit: sw $t0, 4($s0)	60020	43	16	8	(E)		

Assume Loop at location 60000, fill in the blank a,b,c,d,e.

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Loop: andi $t1, $t0, 1	60000	8	9	8	1		
add $s1, $s1, $t1	60004	0	17	9	17	0	32
srl $t0, $t0, 1	60008	0	0	9	9	1	2
beq $t0, $t0, Exit	60012	4	9	9	1		
j Loop	60016	2	15000				
Exit: sw $t0, 4($s0)	60020	43	16	8	4		

◆ [group1]

1. Please select the correct options.
   - a. "~~jr~~ jal label" copies the address of the next instruction into the register $ra and then jumps to the address label.
   - b. Stack is used from low to high address.
   - ✓ c. Hardware will translate complex instructions to simpler microoperations.(Complex instruction set)
   - ✓ d. For nested calls, caller needs to save its return address and any arguments and temporaries after the call on the stack.
   - ✓ e. Immediate can not specify the entire address in PC since there are 32 bits in PC and only 16 bits for immediate.
   - f. Sign extension for E7 from ~~16~~ 8 bits to ~~32~~ 16 bits will be ~~EE~~ FF E7.
   - g. If program counter is at 7999999Ch, we can use jump instruction jump to 80000004h.
   - ✓ h. The last two bits of word aligned address are always 00 because a word is 4-bytes.

2^4 0x7999999C

2^4 0x80000004

看前1个bit 不一樣,不能跳到別區的記憶体

Ans：c, d, e, h

◆ [group5]

Suppose the program counter (PC) is at address 0x0000 0000. Please choose the impossible statement. a b c d e f

0010 1111 1111 1111 1100

2 15 15 15 12

(1) Is it possible to use one single branch-on-equal (beq) MIPS instruction to get to address 0x0002 fffc?

(2) Same to question (1) except that the address is changed to 0xffff ff00. Sign extension 在 ± 2^{17} 內

(3) Is it possible to use one jump (j) MIPS instruction to get to address 0x00030000?

(4) Same to question (3) except that the address is changed to 0x0fff ff00.

Ans: (1) , 18 bit 超過 ± 2^{17} 範圍

◆ [group13]

In MIPS , what’s the difference among “ j ” , ” jr ” , “ jal “ ? What’s their instruction format?

Ans:

Ans: j (jump) : jump directly to a given label without any condition.

jal (jump and link) : store the following address of instruction in $ra and jump to target memory

jr (jump register) : jump to the address in register which is usually $ra (return address register)

```
 j   label
jal  label
jr   $register
```

◆ [group3]

Which of the following statements are true?　Explain why if it's false

只能跳同一区的memory 只能跳 2^{26}　前4个bit 侷限於目前的PC地址

a. We can jump to every word in memory with j instruction, but we can't if use beq instruction.

√ b.

opcode	rs	rt	immediate
beq	\$s1	\$s2	$16_{(10)}$

執行時PC已经指到下一个instruction

Assume PC point to the next instruction .

For this beq instruction, if \$s1==\$s2, PC jump to PC+16*4

√ c. For the following MIPS code:

```
Loop:beq     $t1, $t2, Exit
     addi    $t1, $t1, 1
     j    Loop
Exit:
```

18 bit $\pm 2^{17}$

Immediate value of beq in first line is $2_{(10)}$　$+2^{17}-4 \sim -2^{17}$　2'compliment

~~d.~~ With beq instruction, we can jump $\pm 2^{17}$ bytes from PC

~~e.~~ If we need to use three registers in a function, the instruction

addi \$sp, \$sp, ~~12~~ −12

has to be done before we save the three registers.

Ans:　b, c

a. j can't jump every word in memory, it can only jump 2^{26} words from PC

d. $+2^{17}-4 \sim -2^{17}$　2' complement

e. addi \$sp, \$sp, -12

◆ [group7]

Consider the following program, assuming $s1 is multiple of 4, choose the correct options.

```
1784            bne $s1, $s2, Else
1788            add $s0, $s1, $s2
1792            j Exit
1796 Else: lh    $s0, 0($s1)
1800 Exit:
```

√ (a) if $s1 ≠ $s2, and the value stored at memory address $s1 is

sign extension → 1000

0x00008A43, then $s0 = 0xFFFF8A43 after executing the program.

~~(b)~~ the immediate of the instruction at location 1784 is ~~3~~. 2

~~(c)~~ the jump target of the instruction at location 1792 is ~~1800~~. $\frac{1800}{4}$

(d) if the program concludes the procedure body of a non-leaf procedure, then only $s0, $s1, and $s2 need to be stored on stack.

還有 return address 和 argument

√ (e) The program used two types of addressing mode, which are PC-relative addressing and pseudodirect addressing.

Ans：a ,e