Computer Architecture

Fall, 2022

Week 13

2022.12.05

組別：_____

簽名：_____

◆ [group1]

Please select the correct options and explain the incorrect ones.

√ a. To reduce the delay of the taken branch, we can move branch execution earlier in the pipeline.

√ b. Dynamic pipeline scheduling allows the CPU to execute instructions out of order to avoid stalls but commit results to registers in order.

~~c.~~ Interrupts and exceptions arise within the CPU and from external I/O controllers respectively.
exceptions Interrupts

d. When an exception happens in a pipeline, ~~we flush all instructions in the pipeline.~~
offending 後的指令flush 掉

e. Exceptions are handled by the system control coprocessor in all instruction set architectures.
不一定，只有MIPS

Ans:

d. If restartable → take corrective action, use EPC to return to program
Otherwish → Terminate program, Report error using EPC

◆ [group11]

Select the correct statements.

√ A. A superscalar processor is a CPU that implements instruction-level parallelism.

B. We can reduce the delay of a taken branch by moving branch execution earlier from MEM to ~~IF~~. ID

√ C. Since the stall could be unpredictable, we solve this issue by using the concept of dynamic scheduling.

D. As long as an exception happens in a pipeline, it still has to complete all the instructions which have entered the pipeline.

E. A superscalar processor ~~tends to~~ mainly use compiler scheduled code. (If wrong, you should explain your answer.) stall 不是 predictable, can always schdule around branches Different implementation of ISA have different, latencies and hazards

√ F. Both pipelining and static multiple issue employ instruction level parallelism.

√ G. Compiler reordering instructions to execute is an example of the static multiple issue technique.

H. Hardware can reorder instructions, while the compiler can look ahead for instructions to execute.

Ans: D. If restartable → take corrective action, use EPC to return to program

Otherwish → Terminate program, Report error using EPC

◆ [group13]

which following statement(s) are/is right?

√ A. In order to reduce the amount of penalty of flush, we move the execution of branch to ID in pipeline.

B. There are two kinds of unexpected events, exception arising from an external I/O controller and interrupt from CPU.

C. With the prediction, we don't need to know the target address of branch.

√ D. In MIPS, exceptions managed by a System Control Coprocessor(CP0).

√ E. In the process of handling the exceptions, we need to save PC of offending(or interrupted) instruction at first, save indication of the problem secondly and jump to handler at 8000 00180 ~~before jump to OS~~.

F. In the process of handling the exceptions, we don't restart the program even if the program is restartable in OS.

G. Pipelining is independent of the technology.

√ H. ~~If we want to increase ILP(instruction-level parallelism), there are more stages.~~

Ans: If there are more stages, we want to increase ILP

B. There are two kinds of unexpected events, exception arising from CPU and interrupt from an external I/O controller.

C. We still need to calculate the target address of branch in prediction.

F. In the process of handling exceptions, we would restart the program if the program is restartable.

G. Pipeline is dependent on the technology.

◆ [group10]

Choose the correct answers and also explain if it is false.

√ 1. Branch prediction is more important when pipelines are longer.

2. In the dynamic prediction method, when branch prediction fails, we need to flush the pipeline and ~~keep the prediction unchanged.~~ flip prediction

3. With dynamic prediction, we don't need additional cycles for a taken branch. 1 cycle penalty for a taken branch

4. Compiler schedule applies to many situations including branches. compiler 可以 predict where to jump

√ 5. In the static multiple issue, the compiler groups instructions into "issue packets" and the group of instructions that can be issued on a single cycle.

6. In the static multiple issue,there is ~~no~~ dependency in a packet and between packets. no dependencies with a packet

7. In MIPS with static dual issue, it puts load/store instruction ~~before~~ after ALU/branch in two issue packets.

√ 8. In dynamic multiple issue, it allows the CPU to execute instructions out of order to avoid stalls.

Ans:

◆ [group14]

Consider exception handling for an overflow error. Arrange following handling steps in the correct order:

(A) Complete previous instructions
(B) Prevent destination register from being clobbered
(C) Flush the problematic instruction and subsequent instructions
(D) Set Cause and EPC register values
(E) Transfer control to the exception handler

Ans: B → A → C → D → E
同時做

◆ [group4]

For the following MIPS code, how many times the flush pipeline will take? Suppose ~~it uses the dynamic branch prediction,~~ and the predict branch always taken.

```
Start:
        addi   $t0,   $0,   7
Loop:
        Beq    $t0   $0   Continue
        addi   $t0   $t0   -1
        j   Loop
Continue:
        //other code
        ...
```

flush
7→6
6→5
5→4
4→3
3→2
2→1
1→0

Ans.

- [group9]

  By MIPS convention, an exception, also called a trap, is an unexpected event from internal, and an interrupt is from external. Fill in the table below:

  Ans:

Type of event	From where?	MIPS terminology
I/O device request	external	interrupt
Invoke the operating system from user program	Internal	exception
Arithmetic overflow	Internal	exception
Using an undefined instruction	Internal	exception
Hardware malfunction	either	exception or interrupt