1. Please choose the correct answers.
2. Pipeline can increase throughput for a list of instructions.
3. Pipeline can decrease response time for a single instructions.
4. ALUSrc can be presented by binary logic equation as

ALUSrc = op5‧op4’‧op3’‧op2’‧op1‧op0 (lw) +op5‧op4’‧op3‧op2’‧op1‧op0 (sw)

1. The speedup is limited by the time of the slowest stage.
2. Consider a pipelined processor with K stages. Now we want to execute N instructions. The number of clock cycles we need is (K -1) +N.
3. Allowing jumps, branches, and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance.

Ans:

1. (C) (D) (E) are correct.
2. Response time for each instruction does not decrease because pipeline doesn’t help latency of single task.

(F) The structural hazards may happen.

1. Assume that individual stages of the datapath have the following latencies: IF:300ps ID:400ps EX:350ps MEM:500ps WB:100ps

(1) What is the clock cycle time in a pipelined processor? What is the clock cycle time in a single-cycle processor?

(2) What is the total latency of a lw instruction in a pipelined processor? What is the total latency of a lw instruction in a single-cycle processor?

(3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

Ans :

(1) Pipelined:500ps single-cycle:1650ps

(2) Pipelined:2500ps single-cycle:1650ps

(3) Spilt MEM stage, new clock cycle time is 400ps