1.Given a miss penalty = 40, D-cache miss rate = 4%, I-cache miss rate = 7%, with Load & stores are 40% of instructions. Please compute the actual CPI with base CPI of 4.

Answer:

Miss cycle/ instruction:

I-cache = 0.07 \* 40 = 2.8

D-cache = 0.4 \* 0.04 \* 40 = 0.64

Actual CPI = 4 + 0.64 + 2.8 = 7.44

2. The following diagram is a 2-way set associative cache. Please fill in the blank by using LRU replacement.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Block address | Cache index | Hit / miss | Cache content after access | | | |
| Set 0 | | Set 1 | |
| 0 |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |
| 6 |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |
| 7 |  |  |  |  |  |  |
| 8 |  |  |  |  |  |  |
| 7 |  |  |  |  |  |  |

Ans:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Block address | Cache index | Hit / miss | Cache content after access | | | |
| Set 0 | | Set 1 | |
| 0 | 0 | Miss | Mem[0] |  |  |  |
| 1 | 1 | Miss | Mem[0] |  | Mem[1] |  |
| 6 | 0 | Miss | Mem[0] | Mem[6] | Mem[1] |  |
| 5 | 1 | Miss | Mem[0] | Mem[6] | Mem[1] | Mem[5] |
| 0 | 0 | Hit | Mem[0] | Mem[6] | Mem[1] | Mem[5] |
| 7 | 1 | Miss | Mem[0] | Mem[6] | Mem[7] | Mem[5] |
| 8 | 0 | Miss | Mem[0] | Mem[8] | Mem[7] | Mem[5] |
| 7 | 1 | Hit | Mem[0] | Mem[8] | Mem[7] | Mem[5] |