1. Which statements are right?

1. The clock period is determined by the shortest delay of combinational logic.
2. The instruction having the longest delay among lw, sw, add, beq is lw.
3. The control point is the select input of MUXs.
4. All of control signals can be determined just by controller.
5. The steps to design a processor:

Step1: Analyze instruction set(datapath requirements).

Step2: Select set of datapath components and establish clocking methodology.

Step3: Analyze implementation of each instruction to determine setting of control points effecting register transfer.

Step4: Assemble the control logic.

Ans: B, C

A. The clock period is determined by thelongest delay of combinational logic.

D. All of control signals can be determined just by controller except PCSrc and ALUOp.

1. There is 5 steps but 4 steps. And the right order of these steps is shown below:

Step1: Analyze instruction set(datapath requirements).

Step2: Select set of datapath components and establish clocking methodology.

Step3: Assemble datapath meeting the requirements.

Step4: Analyze implementation of each instruction to determine setting of control points effecting register transfer.

Step5: Assemble the control logic

2. Which statements below are true?

1. Instruction count is only determined by ISA.
2. Instruction execution flow: Instruction fetch->Register access->ALU competition->PC+4
3. CPU divides into two parts, one is the datapath, and the other one is control path.
4. In sequential components for datapath, the register is identical to the D Flip Flop.

Ans: B, C

A. Instruction count is determined by ISA and compiler.

1. In sequential components for datapath, the register is similar to the D Flip Flop, except for the N-bit input and output, and the Write Enable input, which means the content of the register content is updated at the clock tick ONLY if the Write Enable signal is asserted (1).