13th team

which following statement(s) are/is right?

1. In order to reduce the amount of penalty of flush, we move the execution of branch to ID in pipeline.
2. There are two kinds of unexpected events, exception arising from an external I/O controller and interrupt from CPU.
3. With the prediction, we don’t need to know the target address of branch.
4. In MIPS, exceptions managed by a System Control Coprocessor(CP0).
5. In the process of handling the exceptions, we need to save PC of offending(or interrupted) instruction at first, save indication of the problem secondly and jump to handler at 8000 00180 before jump to OS.
6. In the process of handling the exceptions, we don’t restart the program even if the program is restartable in OS.
7. Pipelining is independent of the technology.
8. If we want to increase ILP(instruction-level parallelism), there are more stages.

ans:A, D, E, H

B. There are two kinds of unexpected events, exception arising from CPU and interrupt from an external I/O controller.

C. We still need to calculate the target address of branch in prediction.

F. In the process of handling the exceptions, we would restart the program if the program is restartable.

G. Pipelining is dependent on the technology.

Which following statements are true? ADE

1. We move branch execution earlier in the pipeline to reduce the delay of taken branch.
2. By using static branch prediction, in the deeper and superscalar pipelines, the branch penalty is minor.
3. By using dynamic branch prediction, it won't take any cycle penalty for a taken branch to calculate the target address.
4. When exceptions and interrupts happen, they are hard to deal and usually sacrifice the performance hard.
5. In MIPS, we use cause register to save the indication of the exceptions, and we represent undefined opcode by 0, overflow by 1(assuming 1-bit to represent)

ans:A, D, E