Computer Architecture

**Fall, 2022**

**Week 9**

**2022.11.14**

**組別：＿＿＿＿＿　簽名：＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿＿**

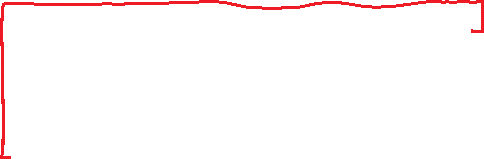
**Group12**

Please explain how the following instruction work with the figure below.

(You only need to explain how each block work, and explain what signal should be chosen for each MUX.)

Code: sub $s0, $s1, $s2

F0519



**Ans:**



**Group1**

Please select the correct options.

a. "Write control" determines when data is updated.

b. The CLK input is a factor only during write operation

c. opcode (Op[5-0]) is always in bits 31-26.

d. The signal of RegWrite is 0 when the instruction is "add".

e. Every logical register transfer starts by fetching the instruction, read registers, then use ALU is following the design principle of simplicity and regularity helps



f. Adding PC and relative address only needs to do sign extend to 32 bits on relative address.

g. The first step of instruction execution is reading registers from the register file.

h. The longest delay determines the clock period.

**Ans:**



**Group3**

Which of the following statement is true:

(A) We can read and write memory and registers whenever we want.

(B) We should set the clock period according to the instruction with the least combinational logic dely.

(C) The PC is updated after fetching instructions.

(D) We need to have many datapath components, then we construct instruction set



**Ans:**



**Group13**

Which statements are right?

1. The clock period is determined by the shortest delay of combinational logic.
2. The instruction having the longest delay among lw, sw, add, beq is lw.
3. The control point is the select input of MUXs.
4. All of control signals can be determined just by controller.
5. The steps to design a processor:

Step1: Analyze instruction set(datapath requirements).

Step2: Select set of datapath components and establish clocking methodology.

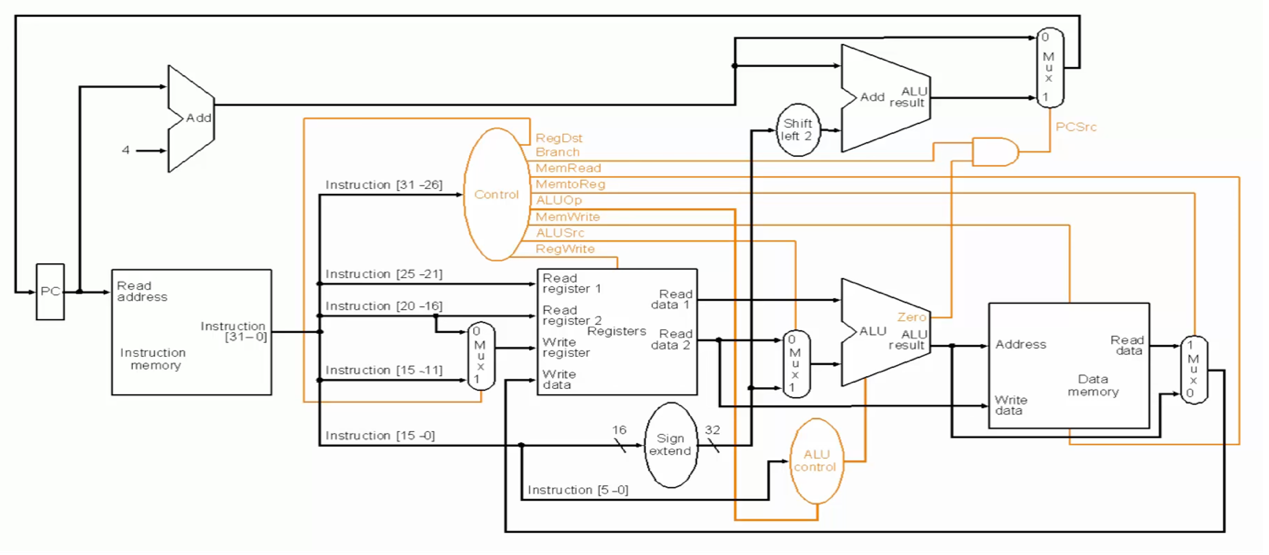
Step3: Analyze implementation of each instruction to determine setting of control points effecting register transfer.

Step4: Assemble the control logic.

**Ans:**



**Group10**

Please set the control signals in the following table. (Refer to the image)

(X means don’t care)

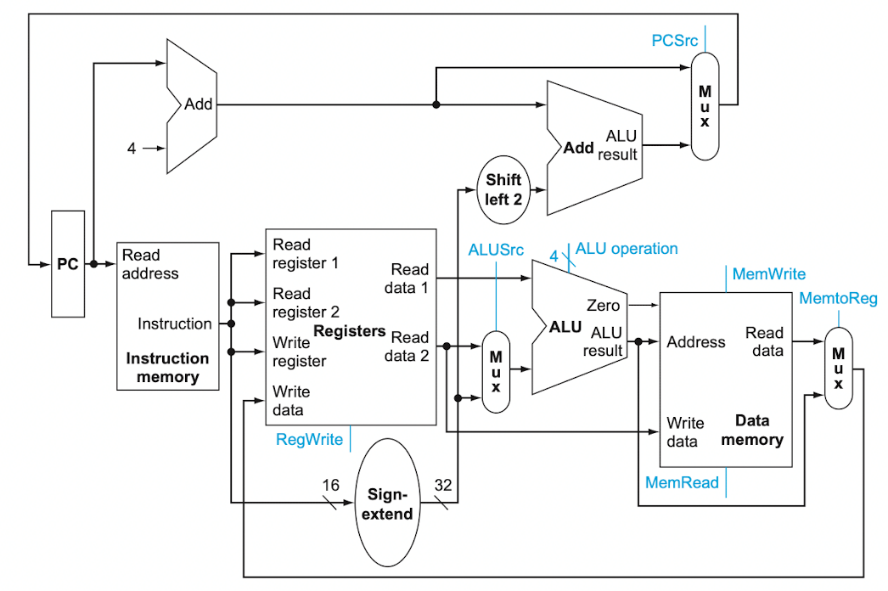
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | RegDst | ALUSrc | MemtoReg | RegWrite | MemRead | MemWrite | Branch |
| add |  |  |  |  |  |  |  |
| lw |  |  |  |  |  |  |  |
| sw | X |  | X |  |  |  |  |
| beq | X |  | X |  |  |  |  |

**Ans:**

**Group11**

Problems in this exercise assume that logic blocks needed to implement a processor's datapath have the following latencies:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| I-Mem | Add | Mux | ALU | Regs | D-Mem | Sign-extend | Shift Left 2 |
| 200ps | 70ps | 20ps | 90ps | 90ps | 250ps | 15ps | 10ps |

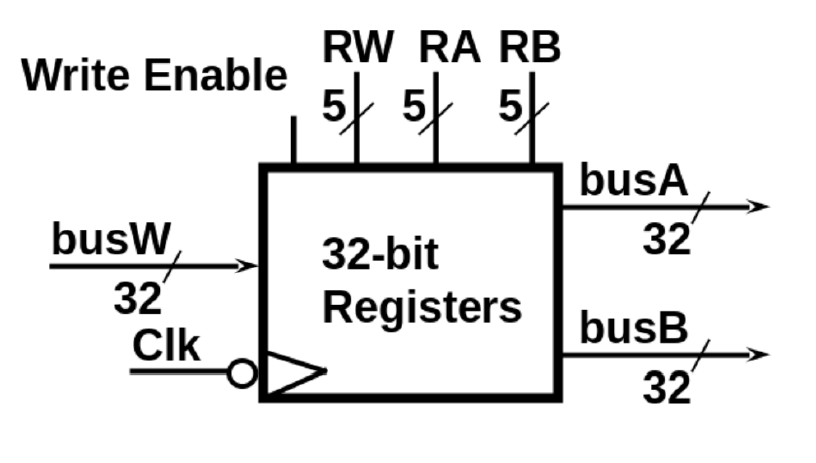
Consider a datapath for a processor that only has one type of instruction: **unconditional PC-relative branch**. (always true, always branches) What would the cycle time be for this datapath?

**Ans:**



**Group2**

Fred using the instruction add $s0, $s1, $s2 and $s0 = 100, $s1 = 45, $s2 = 31.

What are the values of RW, RA, RB in binary and busW, busA, busB in hexadecimal respectively? (Given that $s0 = $16)



**Ans:**

