IMS1400

High Performance 16K x 1 Static RAM

inmos™

FEATURES

- 35, 45 and 55ns Chip Enable access
- Maximum active power 660mW
- Maximum standby power 110mW
- Single 5 volt ± 10% supply
- $\overline{E}$ ($\overline{CE}$) power down function
- TTL compatible inputs and output
- Fully static—no clocks for timing
- Three-state output

DESCRIPTION

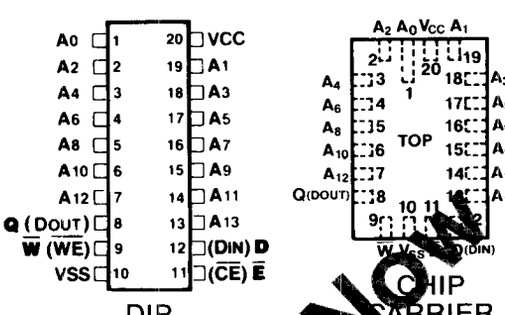
The INMOS IMS1400 is a high performance 16K x 1 bit static RAM having access times of 35, 45 and 55ns and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary N-MOS technology.

The IMS1400 features fully static operation requiring no external clocks or timing strobes, equal access and cycle times, full TTL compatibility and operation from a single +5V ± 10% power supply. Additionally, a Chip Enable ($\overline{E}$) function is provided that can be used to place the IMS1400 into a low power standby mode, reducing power consumption to less than 110mW.

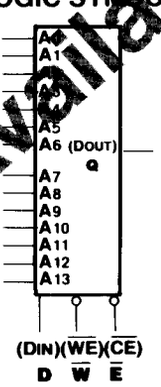
The IMS1400 is packaged in a 20-pin, 300 mil DIP, and is also available in a 20-pin chip carrier, making possible high system packing densities.

The IMS1400 is a high speed VLSI RAM intended for applications that demand superior performance and reliability.

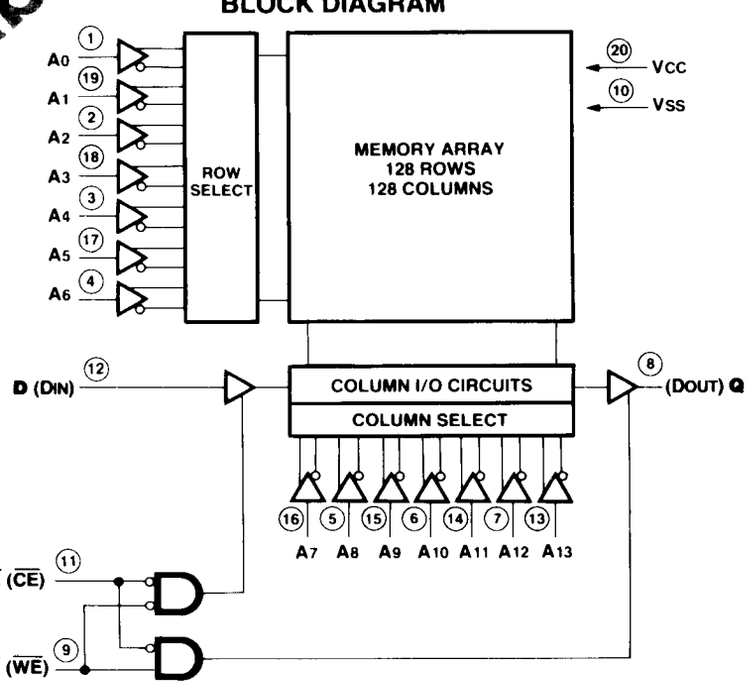
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

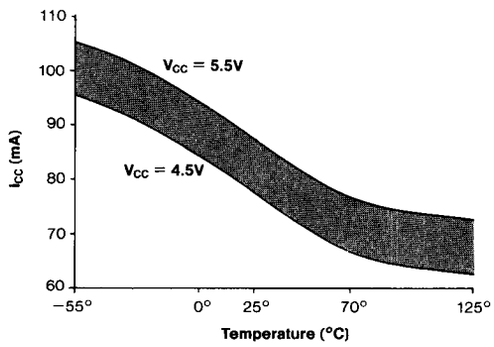
A0 - A13	ADDRESS INPUTS	VCC	POWER (+5V)
W ($\overline{WE}$)	WRITE ENABLE	VSS	GROUND
E ($\overline{CE}$)	CHIP ENABLE		
D (DIN)	DATA INPUT		
Q (DOUT)	DATA OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temp (Ceramic Package) −65°C to 150°C
Storage Temp (Plastic Package) . . −55°C to 125°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TYPICAL DYNAMIC I_{CC} VS TEMPERATURE



DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.5		0.8	V	All Inputs
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

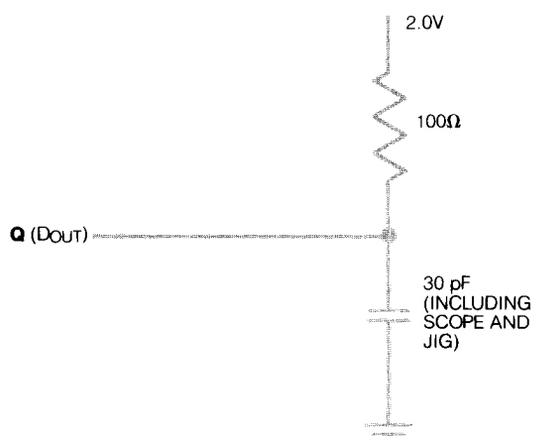
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC_2}	V_{CC} Power Supply Current (Standby)		20	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 16mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

FIGURE 1. OUTPUT LOAD



CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

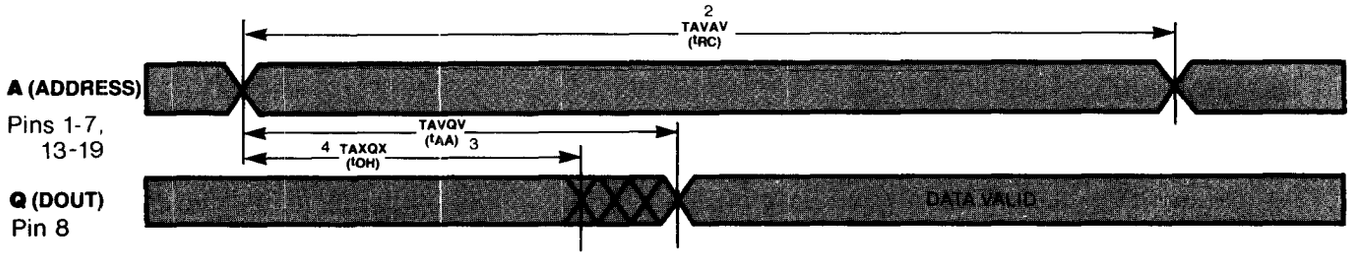
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

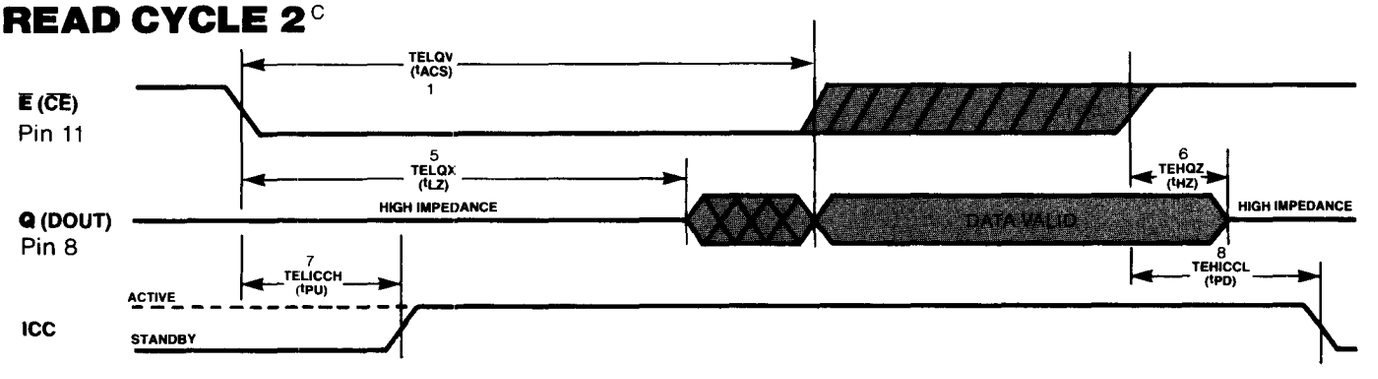
NO.	SYMBOL		PARAMETER	1400-35		1400-45		1400-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	TELQV	t_{ACS}	Chip Enable Access Time		35		45		55	ns	
2	TAVAV	t_{RC}	Read Cycle Time	35		40		50		ns	c
3	TAVQV	t_{AA}	Address Access Time		35		40		50	ns	d
4	TAXQX	t_{OH}	Output Hold After Address Change	3		3		3		ns	
5	TELQX	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	TEHQZ	t_{HZ}	Chip Disable to Output Disable	0	25	0	25	0	30	ns	f
7	TELICCH	t_{PU}	Chip Enable to Power Up	0		0		0		ns	
8	TEHICCL	t_{PD}	Chip Disable to Power Down	0	45	0	45	0	55	ns	
		t_T	Input Rise and Fall Times		50		50		50	ns	e

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



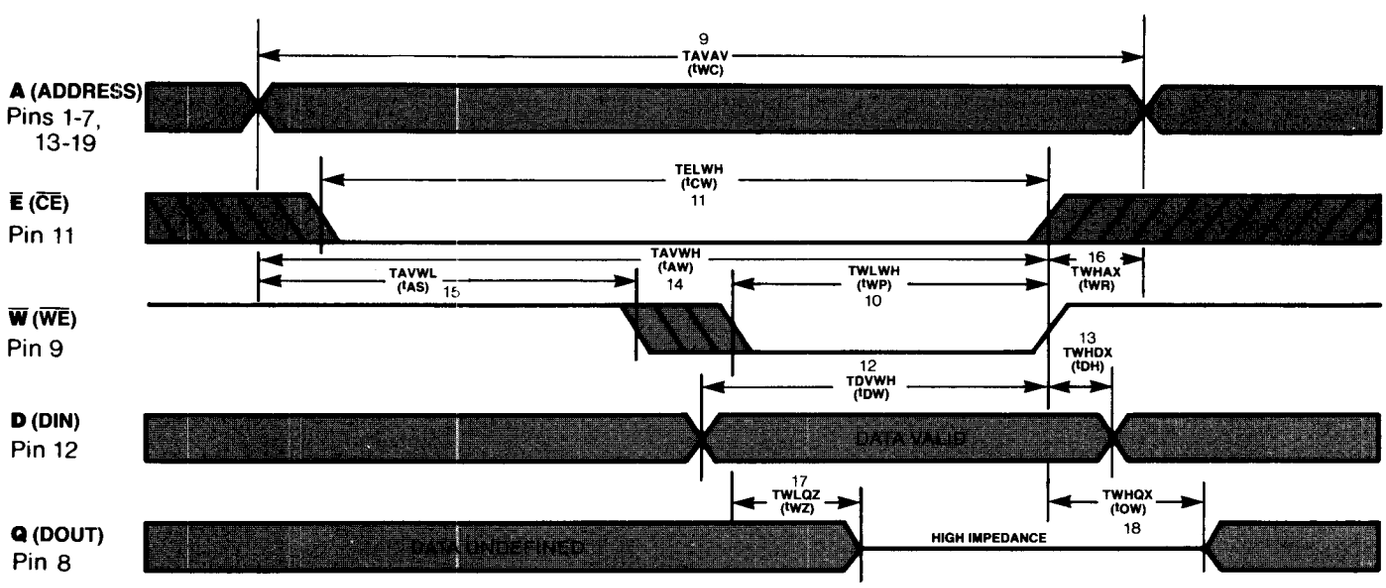
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400-35		1400-45		1400-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	TAVAV	t_{WC}	Write Cycle Time	35		40		50		ns	
10	TWLWH	t_{WP}	Write Pulse Width	20		20		25		ns	
11	TELWH	t_{CW}	Chip Enable to End of Write	35		40		50		ns	
12	TDVWH	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
13	TWHDX	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	TAVWH	t_{AW}	Address Set-up to End of Write	35		40		50		ns	
15	TAVWL	t_{AS}	Address Set-up to Beginning of Write	10		10		15		ns	
16	TWHAX	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	TWLQZ	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f
18	TWHQX	t_{OW}	Output Active After End of Write	0	25	0	25	0	30	ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes low with $\overline{W}$ low, output remains in high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 1



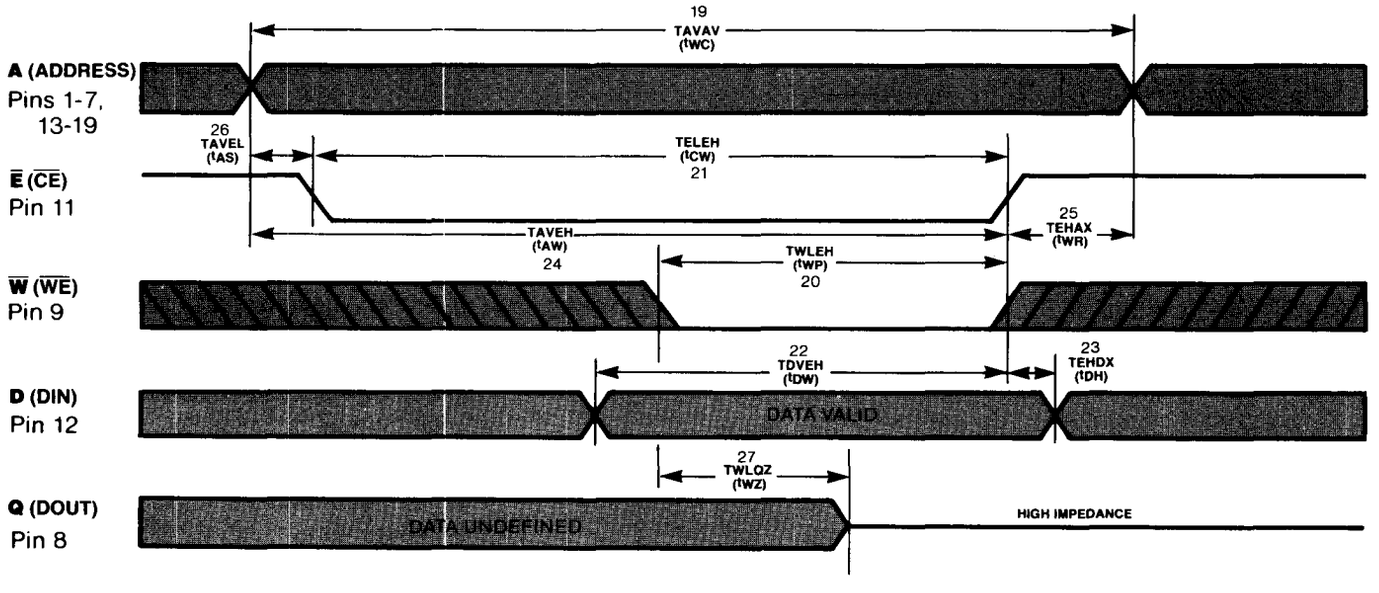
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400-35		1400-45		1400-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	TAVAV	t_{WC}	Write Cycle Time	35		40		50		ns	
20	TWLEH	t_{WP}	Write Pulse Width	20		20		25		ns	
21	TELEH	t_{CW}	Chip Enable to End of Write	35		40		50		ns	
22	TDVEH	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
23	TEHDX	t_{DH}	Data Hold After End of Write	5		5		5		ns	
24	TAVEH	t_{AW}	Address Set-up to End of Write	35		40		50		ns	
25	TEHAX	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	TAVEL	t_{AS}	Address Set-up to Beginning of Write	−5		−5		−5		ns	
27	TWLQZ	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1400 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), fourteen address inputs, a data in (D_{IN}) and a data out (D_{OUT}).

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms, the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select one memory cell out of 16,385. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than 1/6 of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the input (D_{IN}) is written into the selected cell, and the output (D_{OUT}) is in high impedance.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, D_{OUT} becomes active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, D_{OUT} remains in the high impedance state.

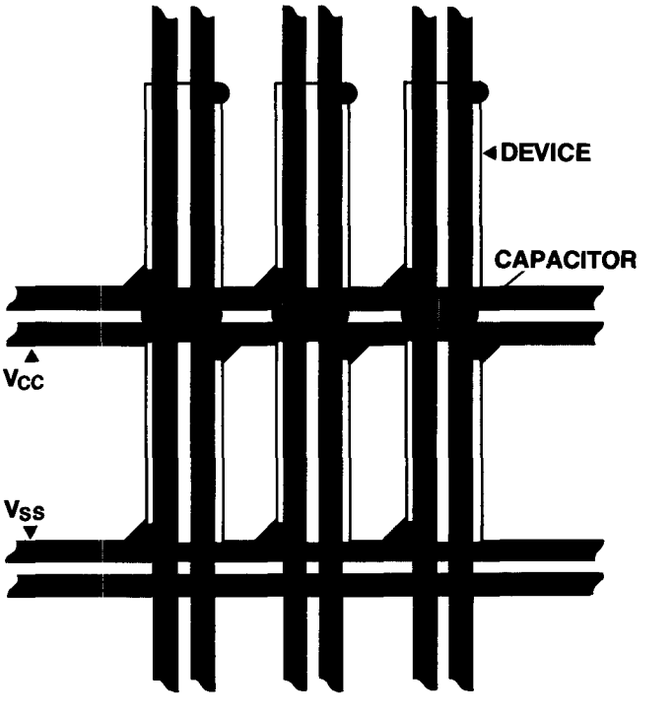
APPLICATION

To ensure proper operation of the IMS1400 in a system environment, it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Also, to prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver-termination combination close to the memory array.

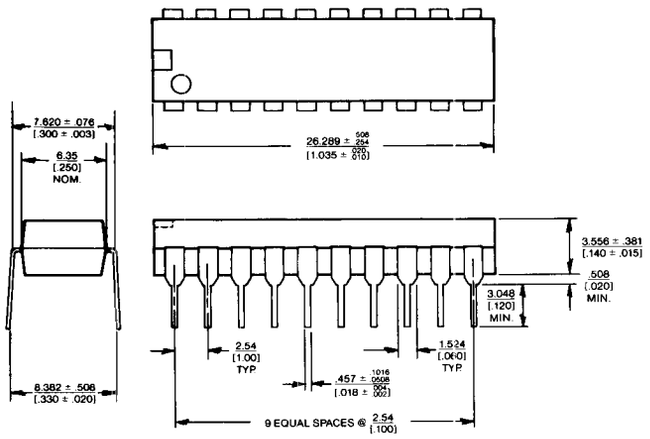
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

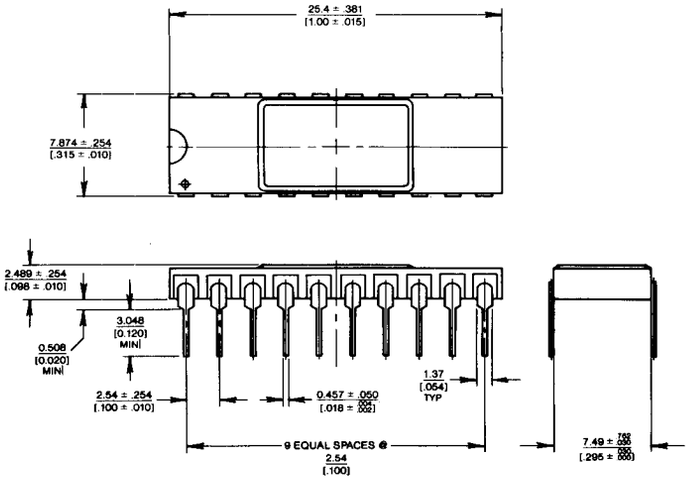
The use of proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are some of the most important, yet basic rules to be followed.

The rules are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

IMS1400

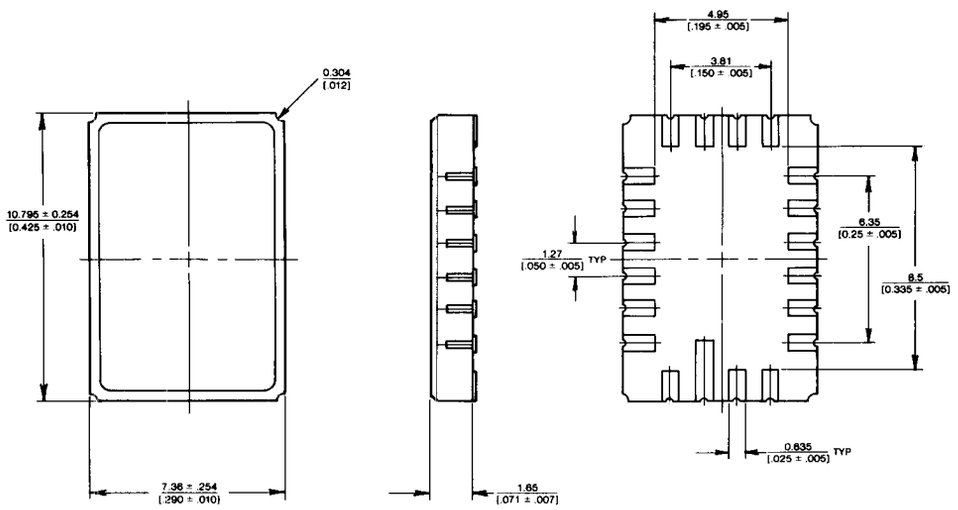
20 PIN PLASTIC DUAL-IN-LINE





20 PIN CERAMIC DUAL-IN-LINE

20 PIN CHIP CARRIER



DIMENSION NOTE:
Top Number in Millimeters
Bottom Number in Inches

TM

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1400	35ns	PLASTIC DIP	IMS1400P-35
	35ns	CERAMIC DIP	IMS1400S-35
	35ns	CHIP CARRIER	IMS1400W-35
	45ns	PLASTIC DIP	IMS1400P-45
	45ns	CERAMIC DIP	IMS1400S-45
	45ns	CHIP CARRIER	IMS1400W-45
	55ns	PLASTIC DIP	IMS1400P-55
	55ns	CERAMIC DIP	IMS1400S-55
	55ns	CHIP CARRIER	IMS1400W-55

inmos™

INMOS Limited • Whitefriars • Lewins Mead • Bristol BS1 2NP • United Kingdom • Phone Bristol (0272) 290861 • TLX: 444723
INMOS Corporation • P.O. Box 16000 • Colorado Springs • Colorado • 80935 • USA • Phone (303) 630 4000 • TWX 910 920 4904
INMOS SARL • Immeuble Monaco • 7 rue le Corbusier • SILIC 219 • 94518 Rungis Cedex • France
INMOS GmbH • Untere Haupstrasse 7 • 8057 Eching • West Germany • Phone Munich (089) 319 10 28 • TLX: 522645