PRELIMINARY SPECIFICATION

GM71C1000

1048576 WORDS x 1 BIT
CMOS DYNAMIC RAM

Description

The GM71C1000 is the new generation dynamic RAM organized 1048576 x 1 Bit. GM71C1000 has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C1000 offers Fast Page Mode as a high speed access Mode. Multiplexed address inputs permit the GM71C1000 to be packaged in a standard 18 pin DIP, 20 SOJ and ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL

Features

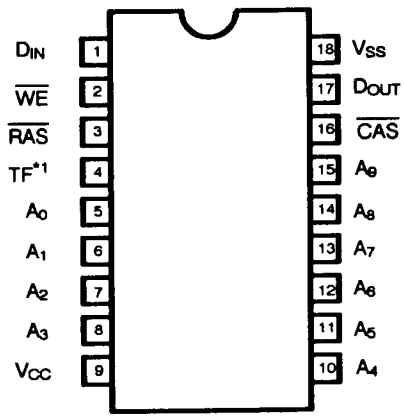
- 1,048,576 x 1 Bit organization
- Fast access time and cycle time : 80/100/120 (Max)
- Single Power Supply of 5V ±10% with a built-in V_{BB} generator

PARAMETER		GM71C1000(ns)		
		-80	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	80	100	120
t_{AA}	Column Address Access Time	40	45	55
t_{CAC}	$\overline{CAS}$ Access Time	25	25	30
t_{RC}	Cycle Time	160	190	220
t_{PC}	Fast Page Mode Cycle Time	55	55	65

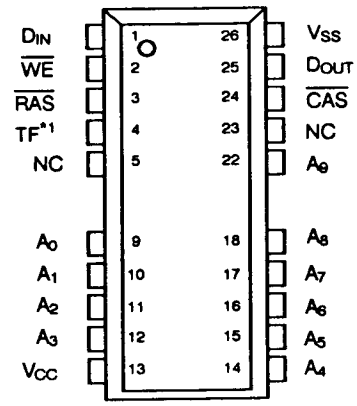
- Low Power
  385mW MAX. Operating (GM71C1000-80)
  330mW MAX. Operating (GM71C1000-10)
  275mW MAX. Operating (GM71C1000-12)
  11mW MAX. Standby
- Read-Modify-Write, $\overline{RAS}$-only refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh and Fast page Mode Capability
- All input and output TTL compatible
- 512 refresh cycle/8ms
- Industry standard 18 pin Plastic DIP/20(26) SOJ/20 ZIP

Pin Configuration

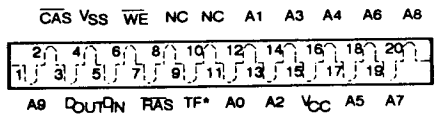
18 PLASTIC DIP (TOP VIEW)



20(26) Lead SOJ Package



20 Lead Plastic ZIP



Pin Description

$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{OUT}	Data Output
D_{IN}	Data Input
V_{CC}	+5V Supply
V_{SS}	0V Supply
TF*1	Test Function

Note) *1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} +0.5V.

Recommended Operating Conditions

(T_A = 0°C to 70°C)

V_{CC} Supply Voltage	4.5 ~ 5.5V
V_{IH} Input High Voltage	2.4 ~ 6.5V
V_{IL} Input Low Voltage	-2.0 ~ 0.8V

Ordering Information

Type NO.	Access Time	PKG
GM71C1000-80 GM71C1000-10 GM71C1000-12	80 ns 100 ns 120 ns	300 MIL 18 PIN PLASTIC DIP
GM71C1000SJ-80 GM71C1000SJ-10 GM71C1000SJ-12	80 ns 100 ns 120 ns	300 MIL 26 (20) PIN PLASTIC SOJ
GM71C1000Z-80 GM71C1000Z-10 GM71C1000Z-12	80 ns 100 ns 120 ns	400 MIL 20 PIN PLASTIC ZIP

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature (plastic)	-55°C to 125°C
Voltage on any Pin Except V_{CC} Relative to V_{SS}	-1.0V to 7.0V
Voltage on V_{CC} relative to V_{SS}	-1.0V to +7.0V
Data Output Current	50mA
Power Dissipation	1.0W

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC Electrical Characteristics : (V_{CC} = 5V ±10%, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	–	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN)	80 100 120	-	70 60 50	mA	1, 2
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} ; D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current (t_{RC} = t_{RC} MIN)	80 100 120	-	60 50 45	mA	2
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN)	80 100 120	-	50 50 40	mA	1, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V), D_{OUT} = High-Z		-	1	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = Min)	80 10 12		60 50 40	mA	
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	80 10 12		5 5 5	mA	
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V)		-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		-10	10	µA	

Note) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ±10%, f = 1MHz, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
C_{I_1}	Input Capacitance (Address, Data Input)	-	5	pF	1
C_{I_2}	Input Capacitance (Clocks)	-	5	pF	1
C_O	Output Capacitance (D_{OUT})	-	7	pF	1, 2

* Note 1. Capacitance is sampled and not 100% tested.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

Electrical Characteristics And Recommended AC Operating Conditions (V_{CC} = 5V ±10%, T_A = 0 ~ 70°C) (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C1000-80		GM71C1000-10		GM71C1000-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read/Write Cycle Time	160	-	190	-	220	-	ns	
t_{RWC}	Read-Modify-Write Cycle Time	190	-	220	-	255	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	55	-	65	-	ns	
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	85	-	100	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	-	120	ns	2, 3
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	3, 4
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	3, 5
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	25	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000	120	10000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	-	10000	-	10000	-	10000	ns	13
t_{RSH}	$\overline{RAS}$ Hold Time (Read or Write Cycle)	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000	30	10000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	22	55	25	75	25	90	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	17	40	20	55	20	65	ns	9
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	12	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	45	-	55	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	10	-	10	-	10	-	ns	10

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) Unit : nS (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C1000-85		GM71C1000-10		GM71C1000-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{REF}	Refresh Period (512 cycle)	-	8	-	8	-	8	ns	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{CWD}	$\overline{CAS}$ to Write Delay Time	25	-	25	-	30	-	ms	10
t_{RWD}	$\overline{RAS}$ to Write Delay Time	80	-	100	-	120	-	ns	10
t_{AWD}	Column Address to Write Delay	40	-	45	-	155	-	ns	10
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ Before $\overline{RAS}$ Refresh	20	-	20	-	25	-	ns	
t_{CSR}	$\overline{CAS}$ to Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	10	-	10	-	10	-	ns	
t_{ACP}	Access Time from $\overline{CAS}$ precharge	-	50	-	50	-	60	ns	14
t_{RHCP}	$\overline{RAS}$ Hold Time from CAS precharge	50	-	50	-	60	-	ns	

Notes

*1. AC measurements assume t_T = 5ns.
*2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
*4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
*5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
*6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
*7. Transition times are measured between V_{IH} and V_{IL}.
*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the psecified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \leq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle : if $t_{RWD} \leq t_{RWD}$ (min), $t_{CWD} \leq t_{CWD}$ (min) and $t_{AWD} \leq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell ; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
*11. These parameters are referenced to CAS leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
*12. An initial pause of 100 µs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
*13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycle.
*14. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

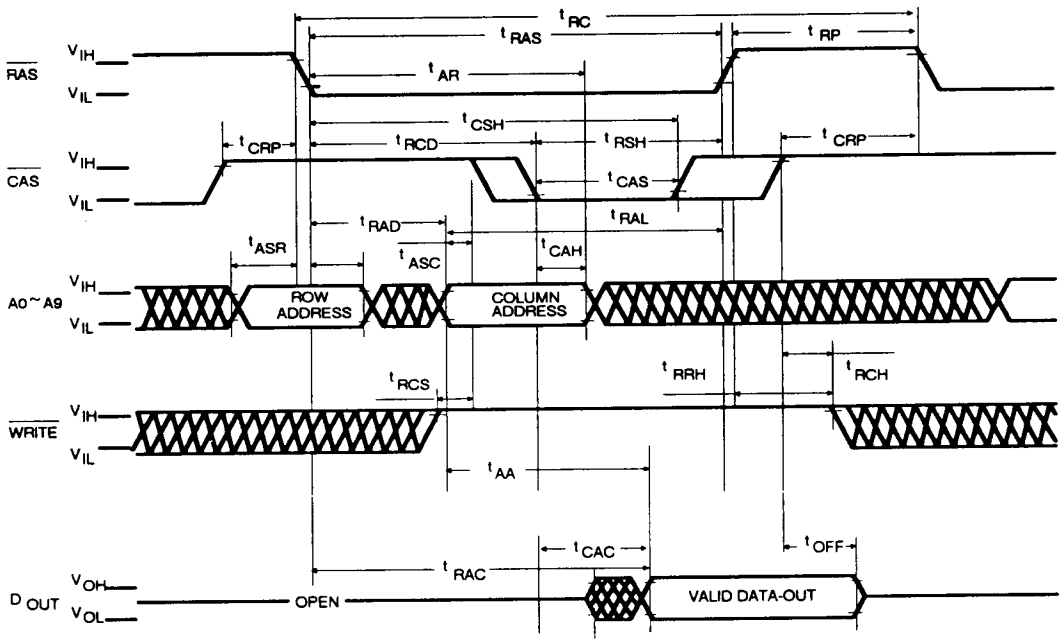


FIGURE 1. READ CYCLE

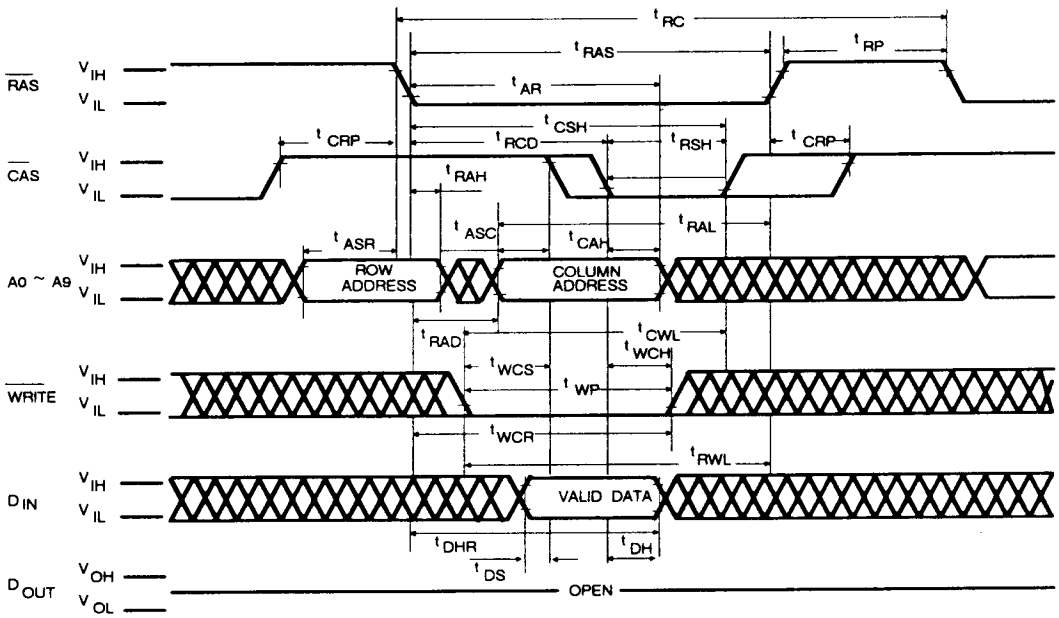


FIGURE 2. EARLY WRITE CYCLE

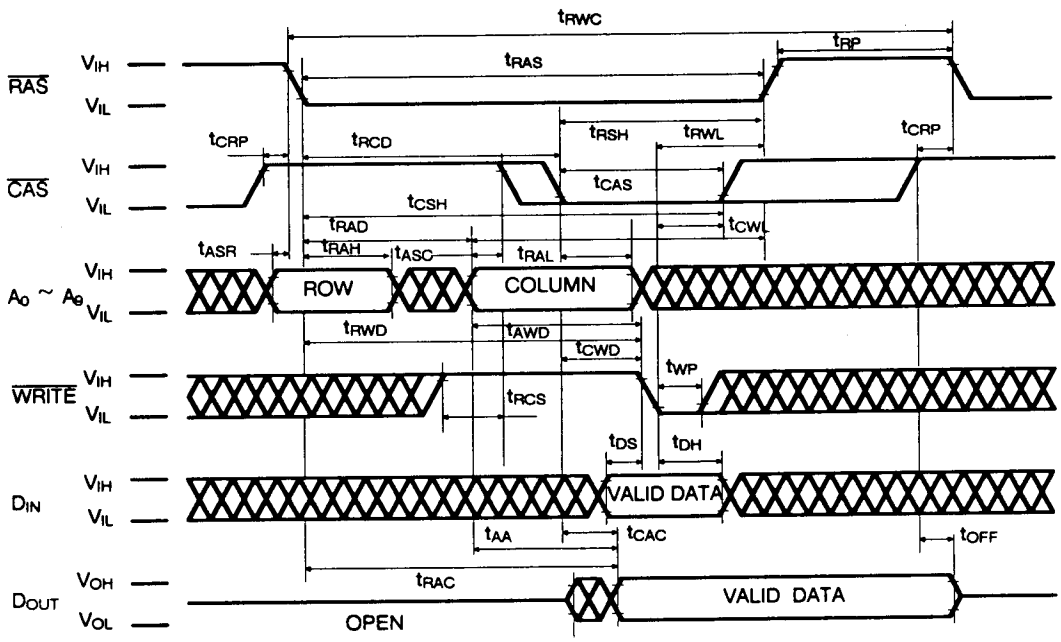


FIGURE 3. READ-MODIFY-WRITE CYCLE

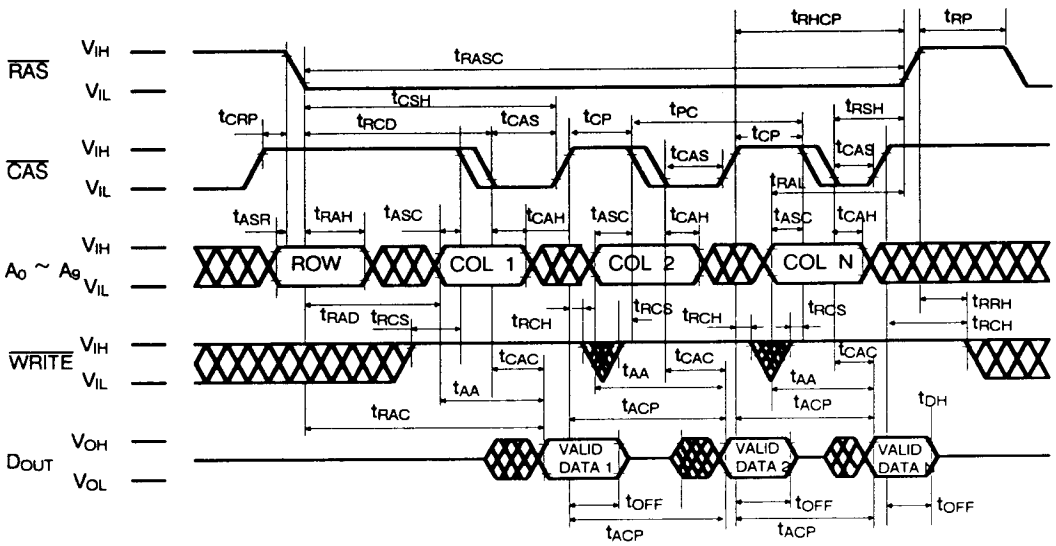


FIGURE 4. FAST PAGE MODE READ CYCLE

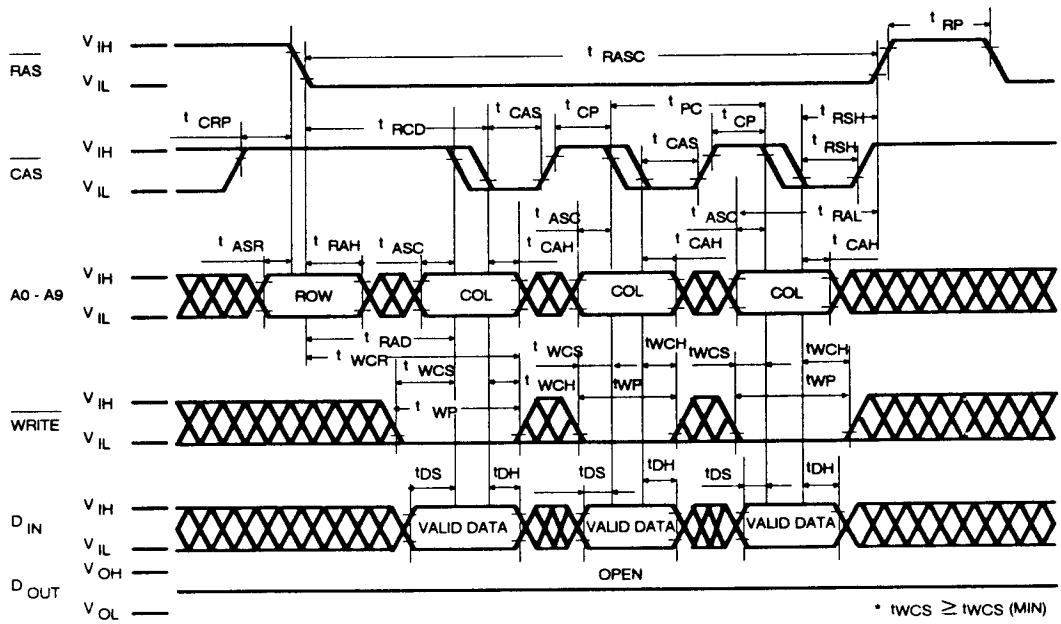


FIGURE 5. FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

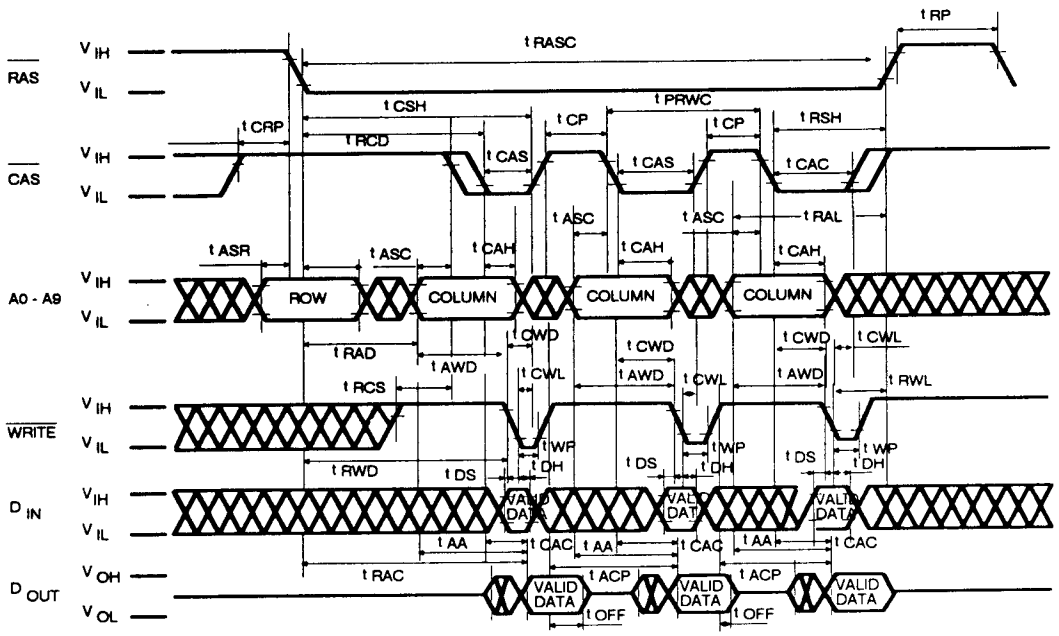


FIGURE 6. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

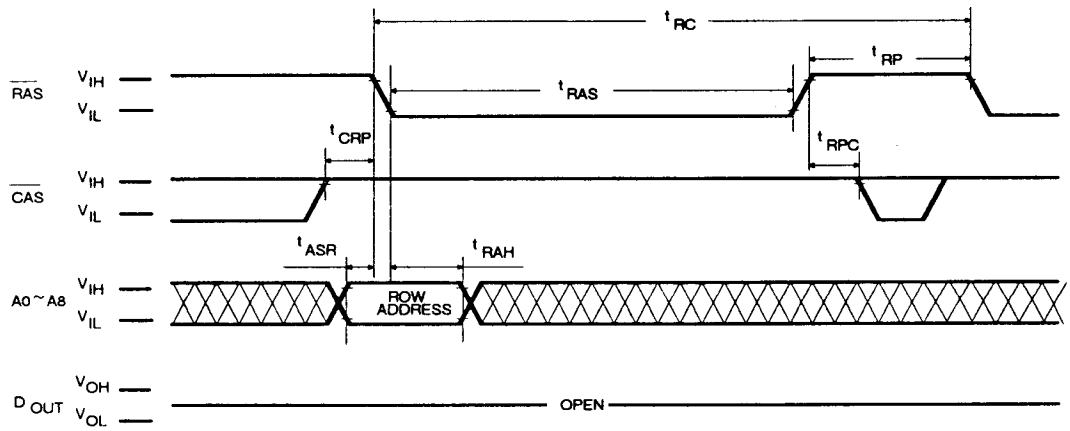


FIGURE 7. $\overline{RAS}$ ONLY REFRESH CYCLE

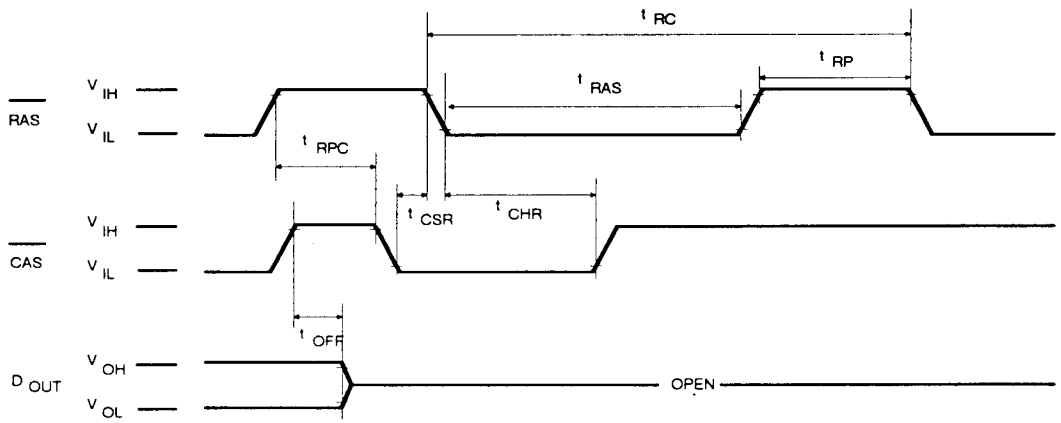
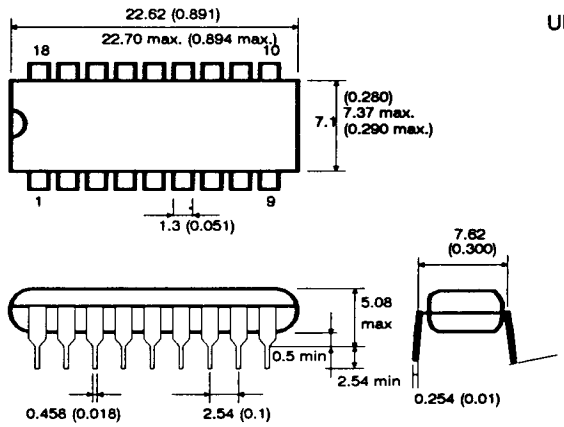


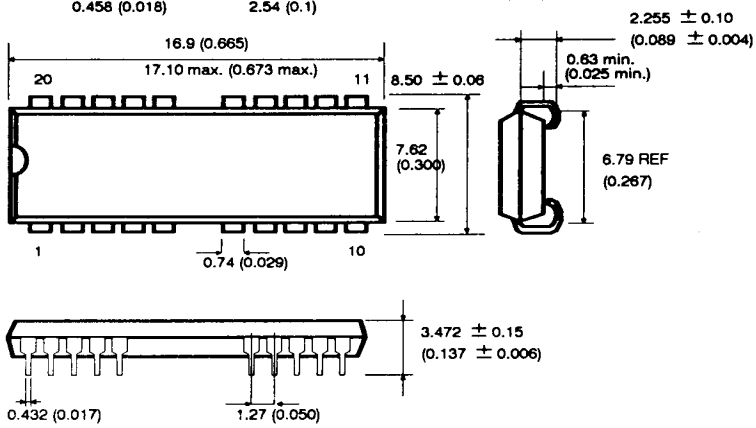
FIGURE 8. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

18 PLASTIC DIP

UNIT : mm (inches)



20 SOJ



20 ZIP