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| A-Z80 CPU User’s Guide |
| An FPGA project recreating the Z80 |
| *© 2014 Goran Devic* |

12/14/2014

# Revision History

|  |  |  |
| --- | --- | --- |
| Date | Revision | Change |
| 2014-12-14 | 1.0 | Initial revision |

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# Introduction

A-Z80 is a conceptual implementation of the venerable Zilog® Z80 processor targeted to synthesize and run on a modern FPGA device. It differs from the existing Z80 implementations in that it is designed from the ground-up through the schematics and low-level gates.

This design is capable of mimicking the actual Z80 CPU and it illustrates its inner workings.

The A-Z80 implementation strives to be internally structurally identical to the original Z80. Using this approach the model achieves a full cycle accuracy and has identical behavior for all documented and undocumented features (\*) not by explicitly hard-coding them but by mimicking their actual design.

Various *Zilog Z80* references are widely available so the CPU itself will not be covered in this document.

You can read more about the conception and implementation of the A-Z80 on its home website: [www.baltazarstudios.com](http://www.baltazarstudios.com) .

This document focuses on the structure and mechanics of working with the project; it should help you understand it and incorporate it into your designs.

# Project directory structure

A-Z80 project can be downloaded at OPENCORES as a SVN repo <http://opencores.org/project,a-z80> and also on Bitbucket: <https://bitbucket.org/gdevic/a-z80> .

The following table describes its hierarchical directory structure:

|  |  |  |
| --- | --- | --- |
| Directory | Sub-directory | Description |
| cpu |  | Contains all core files of the A-Z80 CPU |
|  | alu | Arithmetical and Logical Unit files |
|  | bus | Various bus-related files |
|  | control | Control unit files |
|  | registers | Register block files |
|  | toplevel | A-Z80 top level interfaces and projects |
| docs |  | Documentation and schematic images |
| host |  | Two implementations using the A-Z80 on Altera DE1 FPGA |
|  | basic | Basic computer containing UART mainly for testing and verification |
|  | zxspectrum | Sinclair ZX Spectrum implementation |
| resources |  | General project resources and scripts |
| tools |  | Building and testing utilities and misc. files |
|  | Arduino | Software for Arduino Mega dongle to interface with a Z80 |
|  | dongle | Dongle and simulation scripts and golden files |
|  | z80\_pla\_checker | Windows utility to test and create A-Z80 PLA tables |
|  | zmac | Z80 test and verification assembler files |

# Environment

This is a minimal set of tools needed to compile various parts of the project:

* Altera Quartus II Web Edition (Free)
* ModelSim (Altera edition) – needed only for module simulation (Free)
* Python 2.7 – needed only to change and compile CPU modules. All necessary files needed to include A-Z80 sources in your own project are included (Free)
* Microsoft Visual Studio 2010 SP1 – needed only to recompile the z80\_pla\_checker tool yourself. This is normally not needed since the sources and precompiled executable are checked in with the project.

This project is developed and tested on a Windows 7 OS. Your mileage may vary on Linux.

All designs are tested on an Altera FPGA DE1 board: <http://www.altera.com/education/univ/materials/boards/de1/unv-de1-board.html>



This board has a **Cyclone II EP2C20F484C7** FPGA alongside a number of useful peripherals including a 512 KB SRAM bank, PS/2 keyboard, UART and a VGA connector. Projects can easily be ported to similar boards since Verilog (and SystemVerilog) files that comprise A-Z80 and other add-on designs in this package are synthesizable for other vendors (such as Xilinx) and their tool chains.

# Simulation

## Module simulations

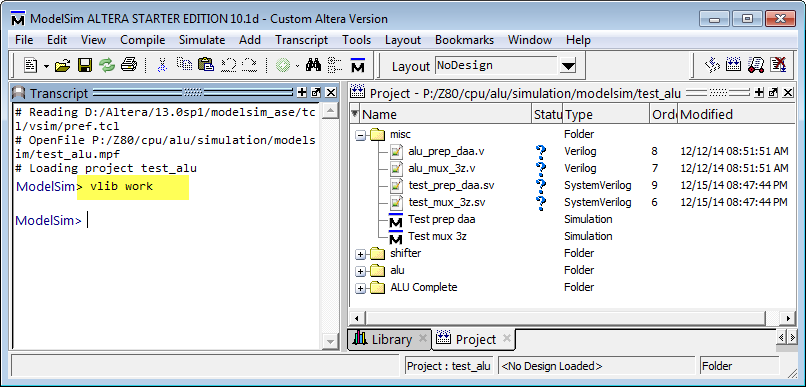
If you start making any changes to the core A-Z80 files, you should run one or more simulations to verify the correctness of your modifications.

Each module in the “**cpu**” directory contains a ModelSim simulation project that verifies the functionality of one or more of its blocks. Before opening any project in ModelSim, run “**modelsim\_setup.py**” script located in the project root directory. That script will set up relative file mappings to enable project to reside anywhere on your drive.

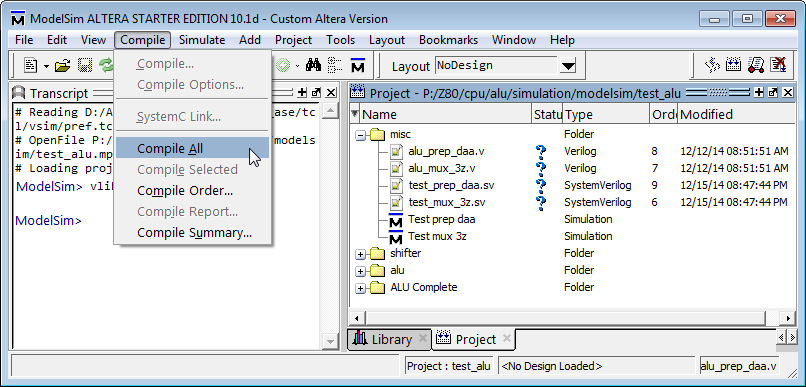
If you have installed and configured ModelSim properly, double-clicking on any **\*.mpf** file will open a project in the ModelSim UI.

In this particular example we will illustrate setting up and starting a simulation of a specific logic block in the **alu** module.

**Important:** Before you can compile any simulation bench, you need to create a library by typing “**vlib work**” as shown:



Next, select “**Compile->Compile All**” to compile all files that are part of a module simulation.



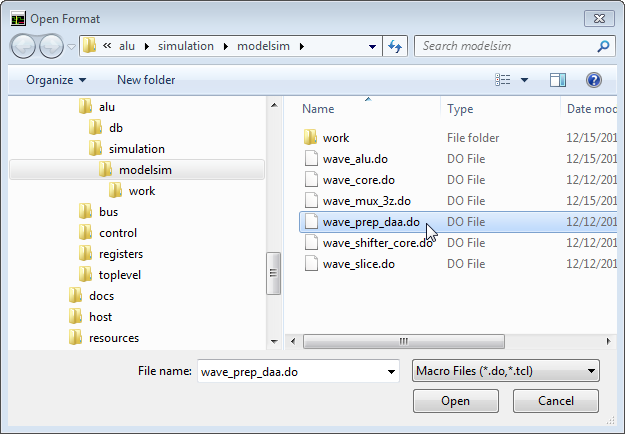
Each project has one or more *simulation configurations*; each configuration tests a specific block of logic. In addition, each configuration has its own wave file which you can load before you run a simulation. Wave files are customized for a specific test and a handy way to quickly see all relevant signals.

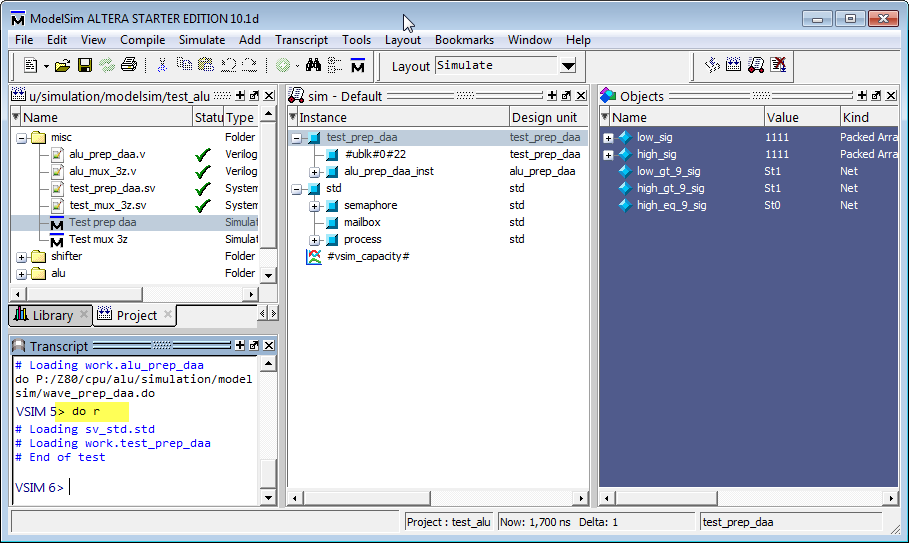
In this example, we will run “Test prep daa” configuration. DAA is a Z80 instruction that adjusts accumulator for a decimal operation. It requires calculating the adjustment addend based on the result of a previous operation. Hence, this test is written to verify the correctness of that calculation.

Each test configuration is run by a main test file that is always written in a *System Verilog* language with the extension **\*.sv**. A file that runs the “Test prep daa” configuration is “**test\_prep\_daa.sv**”.

Double-click on the “Test prep daa” configuration and your simulation should be loaded.

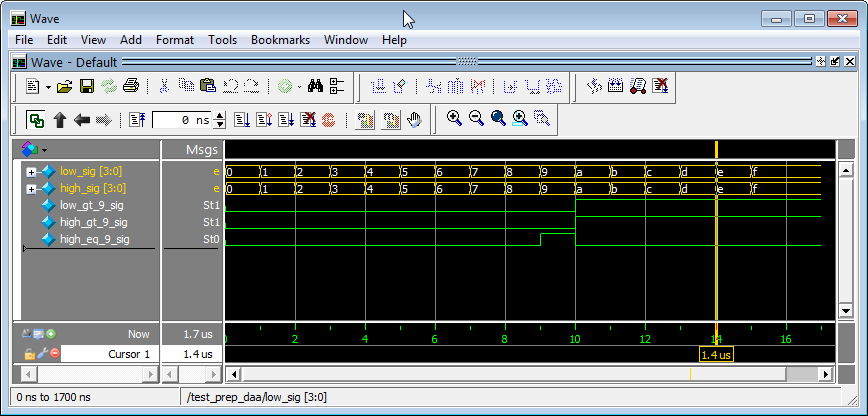
Open the wave window if it is not already visible and select File->Open to load a wave file as shown:





A shortcut is provided to run a simulation: each ModelSim directory contains a small file with the name “r” that contains command “**restart -f ; run -all**”. Run, or rerun, a test simply by typing “**do r**” as shown above.

After running this particular example, you should see a waveform of the DAA preparation block:



Although this is a very simple example, it illustrates a method of running simulations on other configurations and modules. The pattern of configurations, file and waveform names is the same.

Each main test file (for example “**test\_prep\_daa.sv**” contains a set of **assert()** statements to verify signal correctness. The asserts will fail if the signals take unexpected values and your simulation will stop.

Most simulations run for the predetermined number of clocks. The exceptions are top-level simulations (in the directory “**cpu\toplevel\simulation\modelsim**”) and a basic host simulation (in the directory “**host\basic\simulation\modelsim**”). These simulations need to be stopped manually since they simply continue to execute given Z80 executable code.

## Top-level simulations

The two top-level simulations are designed to load an arbitrary Z80 assembly code and execute it. A simple unidirectional UART model is provided so the Z80 software can write to the ModelSim console. The UART model will simulate the behavior of a synthesized serial port. When the same design is synthesized in the FPGA, the same Z80 code will write text messages through the physical serial port.

|  |  |
| --- | --- |
| Module | Simulation project |
| Toplevel | cpu\toplevel\simulation\modelsim\test\_top.mpf |
| Basic host | host\basic\simulation\modelsim\test\_host.mpf |

Those two simulation configurations can run any Z80 code, and several sample tests can be found in the directory “**tools\zmac**” along with the ZMAC assembler and a few batch scripts that simplify the compilation and the test setup.

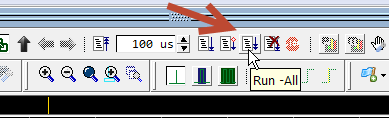
For this example, we will compile and run “Hello, world” test. Its source file is “**tools\zmac\hello\_world.asm**”. (Z80 test files are roughly based on the CP/M and its BDOS interface for text printing)

Two MS DOS batch files are used to compile and run any of the tests in that folder (you can also create and run your own tests as well):

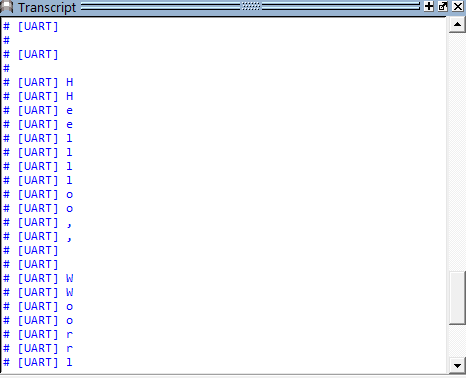
|  |  |
| --- | --- |
| Batch file | Description |
| tools\zmac\make\_modelsim.bat | Compiles and generates executable code for a ModelSim test at “cpu\toplevel\simulation\modelsim\test\_top.mpf”, for “test\_top” configuration. |
| tools\zmac\make\_fpga.bat | 1. Compiles and generates executable code in Intel HEX file format to be included into the target FPGA data file for basic host “host\basic\ host\_board.qpf” 2. Also generates executable code for the basic host ModelSim test at “host\basic\simulation\modelsim\ test\_host.mpf” |

You can simply drag and drop an assembly source file (\*.asm) onto one of the batch files and it will compile them and copy them into proper directories after which you only need to recompile a relevant project.

Drag and drop “**hello\_world.asm**” onto the “**make\_modelsim.bat**” and start a top level simulation (“**test\_top**” configuration). Shortly you should see the output.



After you see the text being written to the UART, you can stop the simulation.



# Verification

## Fuse tests

Fuse is a set of tests to verify Z80 at the individual instruction level. Written for software emulator designers, it contains a fairly complete set of input and output states for each instruction.

Files that are used for this verification are subset of the Fuse emulator source code: <http://fuse-emulator.sourceforge.net> . You can find them in the “**cpu\toplevel\fuse**” directory.

They are simple text files describing individual instruction’s tests and need to be processed into a format that we can run – which is Verilog. A Python script “**cpu\toplevel\genfuse.py**” generates Verilog test code for a selected number of Fuse tests.

See that script file for more details on how to configure it before it can be run.

When run, it creates “**cpu\toplevel\test\_fuse.i**” include file.

|  |
| --- |
| // Automatically generated by genfuse.py  force dut.reg\_file\_.reg\_gp\_we=0;  force dut.reg\_control\_.ctl\_reg\_sys\_we=0;  force dut.z80\_top\_ifc\_n.fpga\_reset=1;  #2 //--------------------------------------------------------------------------------  force dut.instruction\_reg\_.ctl\_ir\_we=1;  force dut.instruction\_reg\_.db=0;  #2 release dut.instruction\_reg\_.ctl\_ir\_we;  release dut.instruction\_reg\_.db;  $fdisplay(f,"Testing opcode 00 NOP");  ... |

Once generated, this include file needs to be compiled with a ModelSim project file “**cpu\toplevel\simulation\modelsim\test\_top.mpf**” to run the test. The test output will show in the ModelSim window and the test will also create and write it into a file “**fuse.result.txt**”.

**Hint:** You can speed up Fuse simulation if you disable output to the wave window by typing:

|  |
| --- |
| VSIM 10> nolog –all |

The following command re-enables the output to the wave window:

|  |
| --- |
| VSIM 10> nolog –reset |

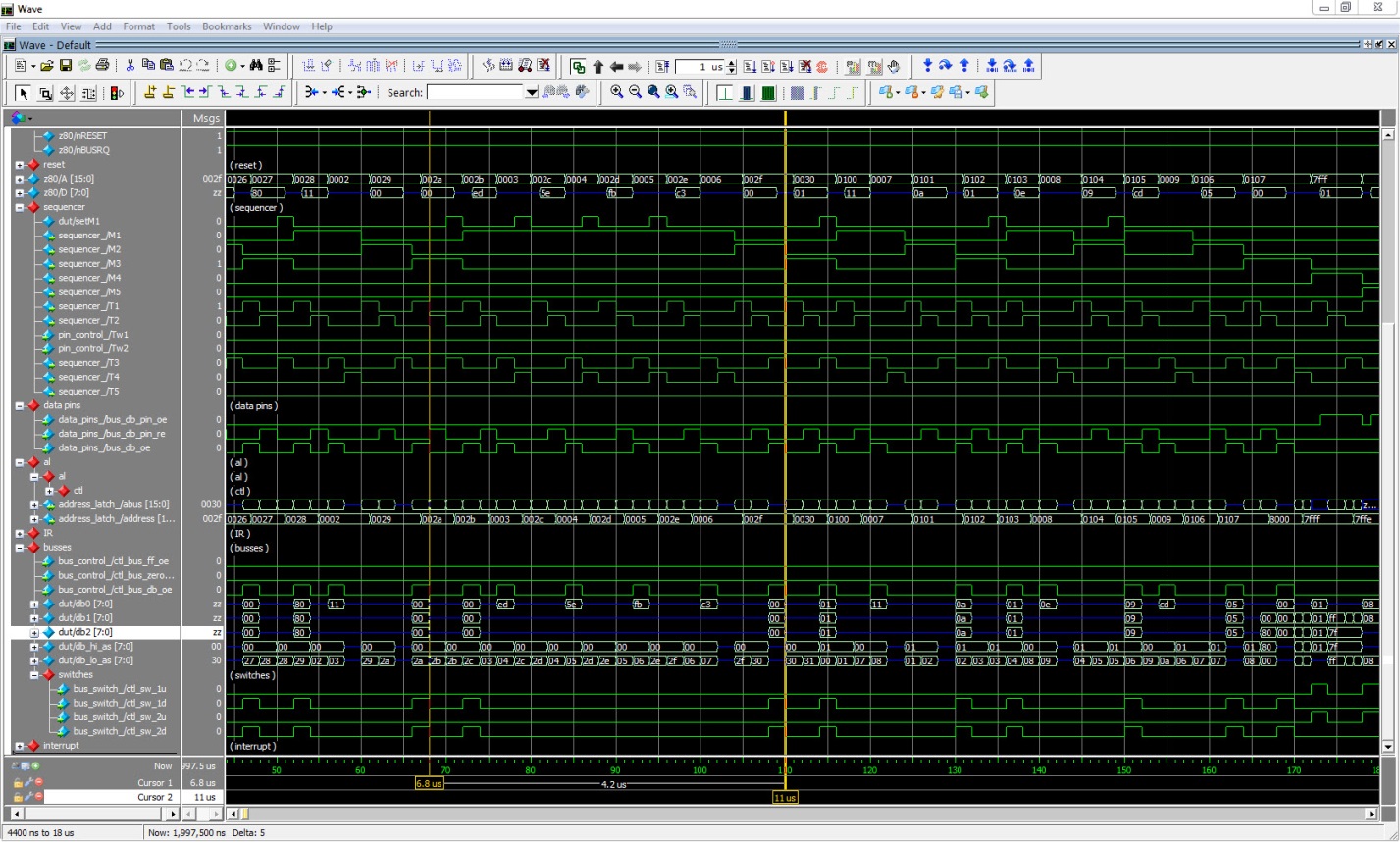


Image 1 : Fuse tests in ModelSim

Results of Fuse tests is written in the file “**fuse.result.txt**”, one instruction per line:

|  |
| --- |
| Testing opcode 00 NOP  Testing opcode ed67 RRD  Testing opcode ed6f RLD  Testing opcode 81 ADD A,C  Testing opcode cb41 BIT 0,C  Testing opcode cb93 RES 2,E  ... |

## Selected functional tests

There are 3 tests that help verify some ALU operations by cross-checking the results run on a real Z80 with the algorithm written in Python:

|  |  |  |
| --- | --- | --- |
| Test directory | Z80 test file | Description |
| tools\dongle\daa | tools\zmac\test.daa.asm | Execute DAA instruction for all values 0-255 |
| tools\dongle\neg | tools\zmac\test.neg.asm | Execute NEG instruction for all values 0-255 |
| tools\dongle\sbc | n/a | Simulate SUB and SBC instructions |

Python scripts run the Arduino Z80 dongle (described in the Tools section) and generate output files. Those files are then compared with the output produced by instruction test Python scripts which implement corresponding algorithms. Lastly, the same text files are compared with ModelSim simulation of those instructions and also by running the same \*.asm executable on the Simple Host FPGA implementation.

Those “golden” files include flags and accumulator going into the instruction and the result:

|  |
| --- |
| F:00 A:00 -> 00 F:44  F:00 A:01 -> 01 F:00  F:00 A:02 -> 02 F:00  F:00 A:03 -> 03 F:04  F:00 A:04 -> 04 F:00  F:00 A:05 -> 05 F:04  F:00 A:06 -> 06 F:04  F:00 A:07 -> 07 F:00  ... |

## Z80 Assembly level tests

Folder “**tools/zmac**” contains several Z80 assembly level tests.

|  |  |
| --- | --- |
| Test source file | Description |
| tools\zmac\hello\_world.asm | Mandatory “Hello, World” |
| tools\zmac\zexdoc.asm | Tests documented Z80 instructions and flags |
| tools\zmac\zexall.asm | Tests ALL Z80 instructions and flags (documented and undocumented) |

They all run under ModelSim, but the last two are very comprehensive tests and should normally be run only on the FPGA in full speed mode.

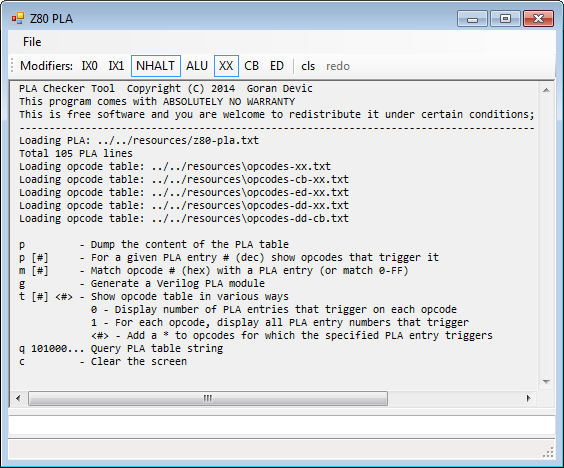
# Tools

## PLA Checker Tool

PLA checker tool in “**tools\z80\_pla\_checker**” directory is a test utility to verify and create PLA code used to statically decode Z80 instruction groups.

In addition to the C# source code, the Windows executable is also checked in so you don’t have to have Microsoft Visual Studio IDE installed to use the tool.

Upon start, the PLA checker tool loads a number of files from the “**resources**” directory including the raw PLA table definition reverse-engineered from the image of a Z80 die as well as opcode mnemonics.

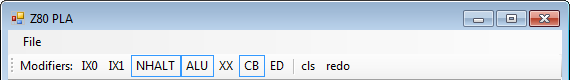


The tool was invaluable in the development phase of A-Z80 cpu and maintain its value as a cross-checker for the PLA code. Available commands are:

|  |  |
| --- | --- |
| Cmd | Description |
| h or ? | Help, list all commands. |
| p | PLA table contains a set of modifiers and a gate-level logic array that ‘filters’ various instruction opcode groups. This command shows you those groups.  C:\Users\gdevic\AppData\Local\Temp\SNAGHTML294146f7.PNG |
| p # | Given a PLA entry number (decimal), show opcodes that are activated by it   |  | | --- | | 10>>> p 3  PLA Entry: 3 Modifier: XX, NHALT  DD => [3] IX/IY prefix  FD => [3] IX/IY prefix | |
| m # | This is a reverse-lookup that shows all PLA table entries that would activate a specific opcode given as a hex number:   |  | | --- | | 12>>> m 76  Opcode: 76  [58] ld r,(hl)  [59] ld (hl),r  [61] ld r,r'  [95] halt | |
| t | Dumps the opcode table in several ways. One or two optional arguments are given which restrict the table or show extra information including the number of PLA entries that trigger for each opcode etc.  C:\Users\gdevic\AppData\Local\Temp\SNAGHTML29487d90.PNG |
| q # | Useful only while simulating the CPU design, this command decodes the actual PLA table string which is a long sequence of binary digits (105 bits in total) |
| g | Generates Verilog code that implements the PLA decode. The output of this command is used to create “**cpu\control\pla\_decode.sv**” source file which is at the core of the design.  C:\Users\gdevic\AppData\Local\Temp\SNAGHTML295b3710.PNGThe image shows the start of the PLA decode module implemented in Verilog. |

Z80 has several opcode tables and addressing modes selected either by the instruction prefix bytes (0xCB, 0xED and IX/IY) or by the internal state (HALT, ALU,…)

PLA checker tool lets you set or unset any of these modifiers when generating opcode dumps.



The modifier buttons directly correspond to modifiers in the PLA table and let you simulate the exact PLA logic behavior.

The tool keeps a history of commands that are typed in. A number displayed at the front of a *prompt* “>>>” is a location in the history buffer. Pressing **PgUp** and **PgDown** selects a command from the history buffer; **ESC** clears the command line.

## Arduino Tools

Directory “**tools\Arduino\Z80\_dongle**” contains firmware for the *Arduino Mega* connected to a Zilog Z80 through a custom dongle. This setup can be used to pace Z80 in a controlled way and to execute test instructions and monitor bus activity. You can read more about that dongle at [www.baltazarstudios.com](http://www.baltazarstudios.com).

It was heavily used to generate tables for the correct bus behavior. These tables and Python scripts that create them are checked with the project in the directory “**tools\dongle**”.

# Integration

This section describes how to integrate the A-Z80 CPU into your own project.

The method is tested with Altera design tools (Quartus), but it should be relatively easy for someone skilled in the art to use other vendor such is Xilinx.

The integration involves adding all relevant source files. This table lists them:

|  |
| --- |
| cpu/alu/alu\_slice.v  cpu/alu/alu\_shifter\_core.v  cpu/alu/alu\_select.v  cpu/alu/alu\_prep\_daa.v  cpu/alu/alu\_mux\_8.v  cpu/alu/alu\_mux\_4.v  cpu/alu/alu\_mux\_3z.v  cpu/alu/alu\_mux\_2z.v  cpu/alu/alu\_mux\_2.v  cpu/alu/alu\_flags.v  cpu/alu/alu\_core.v  cpu/alu/alu\_control.v  cpu/alu/alu\_bit\_select.v  cpu/alu/alu.v  cpu/bus/bus\_switch.sv  cpu/bus/inc\_dec\_2bit.v  cpu/bus/inc\_dec.v  cpu/bus/data\_switch\_mask.v  cpu/bus/data\_switch.v  cpu/bus/data\_pins.v  cpu/bus/control\_pins\_n.v  cpu/bus/bus\_control.v  cpu/bus/address\_pins.v  cpu/bus/address\_latch.v  cpu/bus/address\_mux.v  cpu/control/sequencer.v  cpu/control/resets.v  cpu/control/ir.v  cpu/control/interrupts.v  cpu/control/decode\_state.v  cpu/control/clk\_delay.v  cpu/control/pin\_control.v  cpu/control/pla\_decode.sv  cpu/control/memory\_ifc.v  cpu/control/execute.sv  cpu/registers/reg\_latch.v  cpu/registers/reg\_file.v  cpu/registers/reg\_control.v  cpu/toplevel/z80\_top\_direct\_n.sv |

In addition, any one of the two sample implementations (*basic host* and *zxspectrum*) provide a good starting point and a working example.

# Pinout

The top-level file “**cpu\toplevel\z80\_top\_direct\_n.sv**” exports the following interface:

|  |
| --- |
| module z80\_top\_direct\_n(  output wire nM1,  output wire nMREQ,  output wire nIORQ,  output wire nRD,  output wire nWR,  output wire nRFSH,  output wire nHALT,  output wire nBUSACK,  input wire nWAIT,  input wire nINT,  input wire nNMI,  input wire nRESET,  input wire nBUSRQ,  input wire CLK,  output wire [15:0] A,  inout wire [7:0] D  ); |

The pinout is 100% identical to the Zilog Z80 package; bus timings also implement tri-state signaling. (While this is admittedly not optimal for an FPGA implementation, the goal of the project is to mimic the actual Z80 silicon).

Your system design should simply include all necessary files and instantiate a “**z80\_top\_direct\_n**” module.

# Sample implementations

Two working implementations are included. They are both located in the “**host**” directory and they use the Altera DE1 FPGA development board.

Warning: The synthesis and *fMax* numbers as shown might vary depending on the tool versions, applied timing constraints and the exact configuration.

## Simple host

A “*basic host*” board contains A-Z80 CPU, 16 KB RAM embedded within single port Cyclone RAM cells and a unidirectional implementation of the UART to write the text out. The board’s architecture is so simple that it made sense to create a ModelSim configuration as well.

|  |  |
| --- | --- |
| File | Description |
| host\basic\host\_board.qpf | Quartus project file for FPGA |
| host\...\simulation\modelsim\ test\_host.mpf | ModelSim project file for simulation |
| host\basic\host\_board\_fpga.sv | Top-level board source file for FPGA implementation |
| host\basic\ host\_board\_ModelSim.sv | Top-level board source file for ModelSim board model |
| host\basic\test\_host.sv | ModelSim test bench for the simulation model |

This host board can load and run any Z80 executable (for example, one of those in “**tools\zmac**” directory). Programs can print to UART and on a physical DE1 board the text is seen through the attached terminal; in the simulation environment the text is written in a window of a ModelSim project. Image 2 shows the output of the “**tools\zmac\hello\_world.asm**” being captured through the serial port.

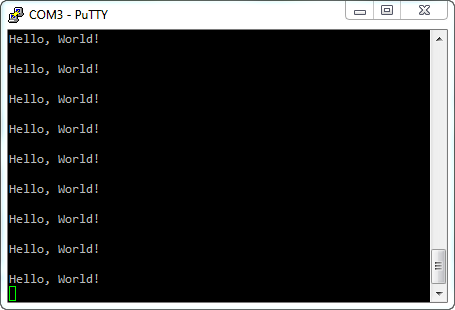
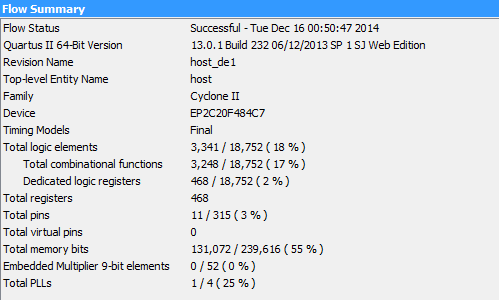
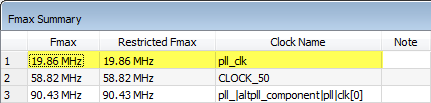


Image 2: "Hello, World"

This is the synthesis result of a simple host design on an Altera DE1 board:



Since the CPU CLK is derived from the *pll\_clk*, the effective A-Z80 fmax for this compilation is 19.86 MHz.



## Sinclair ZX Spectrum

The year was 1982: this project fully implements a *Sinclair ZX Spectrum 48K* computer.

The model contains Verilog code for all parts that make up that computer. Directory “**host\zxspectrum\ula**” contains blocks (drivers) for the keyboard, video signal using the VGA, sound, RAM memory, clocks etc.

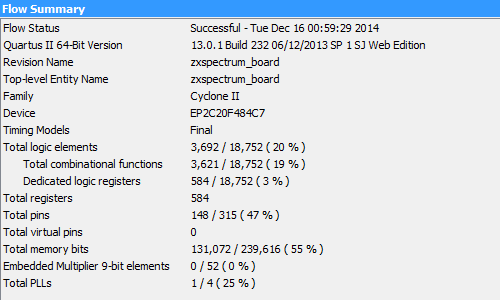
There are 2 system ROM images included in the “**host\zxspectrum\rom**” directory – the original ZX Spectrum ROM and an improved, so-called “Gosh Wonderful” ROM – merged into a single image which is to be flashed into the DE1’s flash memory starting at the address 0.

Image 3 shows a game “*Manic Miner*” loading through the audio line-in connector into the FPGA board (center) and a Kempston compatible joystick in the foreground.

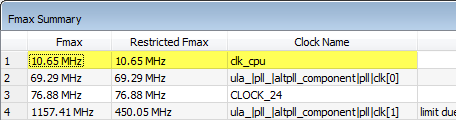


Image 3 : Sinclair ZX Spectrum on Altera DE1

This is the synthesis result of a ZX Spectrum host design on Altera DE1 board:



Although the computer runs at 3.5 MHz, the *clk\_cpu* fmax for this compilation is 10.65 MHz.



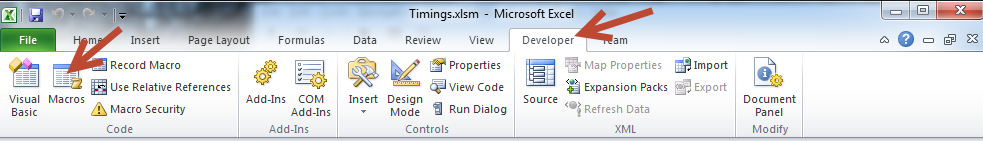
# Advanced Topics

## Modifying the A-Z80 CPU

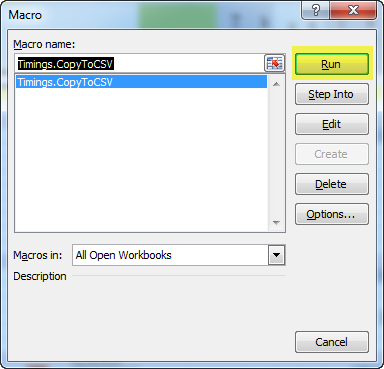
If you want to make a change to any instruction’s timing or a sequence of operations, do it in the file “**cpu\control\Timings.xlsm**”. This is a Microsoft Excel spreadsheet file that contains timing tables for each instruction group. Vertical columns are operations on specific blocks. Instruction groups are listed by the M and T clock providing the exact timing for each set of operations.

Operations itself are represented by short tokens (for example, “PC” or “mr”, etc.) which are defined in the file “**cpu\control\timing\_macros.i**”. Every token is defined and translated into one or more concrete control signals.

After you change the timing spreadsheet export it into a TAB-separated file. The spreadsheet contains a macro to do that for you. Click on the “Developer” menu and run the Macros:



This will replace the existing CSV file which is ok. Both are checked in although one is generated from the other one.



After that is done, create a Verilog file from those timings by running a python script “**cpu\control\genmatrix.py**”. That script reads the CSV text file timing table and generates file “**exec\_matrix.i**” file which implements actual Verilog code that controls the timings.

All Python scripts in this project can be run in-place without the need to specify arguments.

If you change any *schematic file* and your change adds or removes that module’s input or output signals, you need to run two Python scripts to recreate global includes:

“**cpu\control\genref.py**” – generates global include files using all export module signals:

* “exec\_module.i” contains input/output definitions to be included in the module def.
* “exec\_zero.i” contains Verilog code to set all input wires to zero.

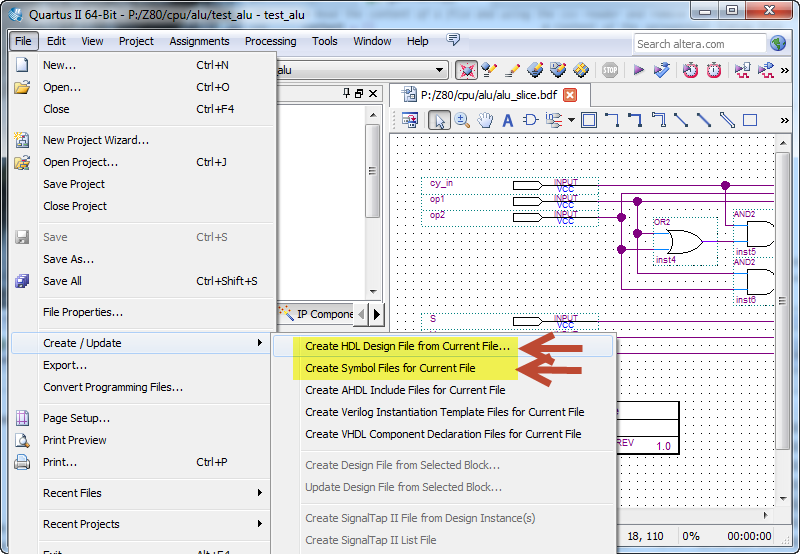
“**cpu\toplevel\genglobals.py**” – generates a list of global wire defines:

* “globals.i” contains Verilog code that defines all global signal wires.

*Quartus* project files (\*.qpf, \*.qsf) in “cpu\alu”, “cpu\bus”, “cpu\control” and “cpu\registers” directories are non-functional and just conveniently hold sets of module files together. Quartus project in the “cpu\toplevel” directory contains a top-level schematic diagram only and is also not functional. They are only containers to hold files.

In order to compile a project, look in a sample project such is “**host\basic\host\_board.qpf**”.

When you are modifying a schematic (which are most of the A-Z80 blocks), open a Quartus container project for that module (for example, when modifying a schematic in the ALU block, open “**cpu\alu\test\_alu.qpf**”), change the schematics, compile it (to make sure it has no errors) and then export it to both the Verilog equivalent and a symbol file as shown:



|  |
| --- |
| Verilog code is used to compile with the rest of the A-Z80 files in your master top-level design project while a symbol file is optional for now but could be used in the future to create a schematic top-level. |