via6522

Overview

The via6522 is a versatile interface adapter 32-bit peripheral core that is register compatible with a 6522. The low order eight bits of a register mirror the 6522 function.

Features

- 32-bit port data width
- 3 64-bit Timers
- 1 32-bit shift register

Registers

Reg	Bits	Moniker		Comment
00	32	PB	Port B I/O	
04	32	PA	Port A I/O	handshaking
08	32	PBDDR	Port B data direction	
0C	32	PADDR	Port A data direction	
10	32	T1CL	Timer 1/3 count low	
14	32	T1CH	Timer 1/3 count high	
18	32	T1LL	Timer 1/3 latch low	
1C	32	T1LH	Timer 1/3 latch high	
20	32	T2CL	Timer 2 count low	
24	32	T2CH	Timer 2 count high	
28	32	SR	Shift register	
2C	16	ACR	Auxiliary control register	
30	16	PCR	Peripheral control register	
34	16	IFR	Interrupt flag register	
38	32	IER	Interrupt enable register	
3C	32	PA	Port A I/O	no handshaking

PB (Reg 0)

Operates in the same manner as the 6522 port B but is 32-bits wide rather than 8-bits. If port B input latching is enabled, then input data on port B is latched by an active transition of the selected handshaking signal. Otherwise input data is reflected directly by reading the port register.

PA (Reg 1)

Operates in the same manner as the 6522 port A but is 32-bits wide rather than 8-bits. If port A input latching is enabled, then input data on port A is latched by an active transition of the selected handshaking signal. Otherwise input data is reflected directly by reading the port register.

PBDDR (Reg 2)

Operates in the same manner as the 6522 port B ddr but is 32-bits wide rather than 8-bits. Each bit that is set in this register set the corresponding port B I/O to an output. Each bit that is clear in this register sets the port B I/O to an input. The default value in this register at reset is zero, making all port B I/O's inputs.

PADDR (Reg 3)

Operates in the same manner as the 6522 port A ddr but is 32-bits wide rather than 8-bits. Each bit that is set in this register set the corresponding port A I/O to an output. Each bit that is clear in this register sets the port A I/O to an input. The default value in this register at reset is zero, making all port A I/O's inputs.

T1CL (Reg 4)

Similar function to the reg 4 of the 6522. Provides read access to the low order 32-bits of timer 1. Acts as a latch for the low 32-bits of the value to be loaded into the timer. Byte lane selects allow loading of only the byte that needs to be modified.

This register also provides access to timer 3 if the timer 3 access bit is set in the peripheral control register.

T1CH (Reg 5)

Similar in function to register 5 of the 6522. When the timer is in 16-bit mode writing this register transfers bit 0 to 7 of the timer 1 latch to bits 0 to 7 of the timer and transfers input data bits 0 to 7 to counter bits 8 to 15 of the timer. Timer counter bits 16 to 63 are set to zero.

When the timer is in 64-bit mode writing this register transfers the low order latch to bits 0 to 31 of the counter, and bits 32 to 63 of the counter are loaded with the input data value.

This register also provides access to timer 3 high order bits if the timer 3 access bit is set in the peripheral control register.

T1LL (Reg 6)

Similar in function to register 6 of the 6522. Provides access to the timer 1/3 low order latches.

T1LH (Reg 7)

Similar in function to register 7 of the 6522. Provides access to the timer 1/3 high order latches.

T2CL (Reg 8)

Similar in function to register 8 of the 6522. Provides access to timer 2 low order latch / count.

T2CH (Reg 9)

Similar in function to register 9 of the 6522. Provides access to timer 2 high order latch / count.

SR (Reg 10)

Similar in function to register 10 of the 6522. The shift register is 32-bits wide. When configured to operate in 32-bit mode data is shifted into bit zero and out of bit thirty-one in a manner analogous to the eight-bit operation. When configured for 8-bit mode (the default mode) only the low order eight bits of the shift register are used.

ACR (Reg 11)

The low order eight bits of the register mirror the 6522 function. Only 12 bits of this register are implemented.

Bits	Function
0	port a input latch enable
1	port b input latch enable
2 to 4	shift register mode
5	timer 2 mode
6 to 7	timer 1 mode
8	timer 1 64-bit enable (1= 64 bit, 0 = 16 bit)
9	timer 2 64-bit enable (1 = 64 bit, 0 = 16 bit)
10	shift register 32-bit enable (1 = 32 bit, 0 = 8 bit)
11	reserved
12	timer 3 mode (1 = continuous, 0 = pulse)
13 to 15	reserved

Timer 2 Mode	Operation
0	count down bus clock
1	count down negative edges of PB6

PCR (Reg 12)

The low order eight bits of the register mirror the 6522 function. Only nine bits of this register are implemented.

Bits	
0	CA1 mode
1 to 3	CA2 mode
4	CB1 mode
5 to 7	CB2 mode
8	T3 access (1 = access T3 registers, 0 = access T1 registers)
9 to 15	reserved

IFR (Reg 13)

The interrupt flag register mirrors the operation of the interrupt flag register in the 6522. There is one extra bit (bit 8) which indicates a timer 3 interrupt.

Bits	Source
0	ca2 active transition
1	ca1 active transition
2	shift register
3	cb2 active transition
4	cb1 active transition
5	timer 1 underflow
6	timer 2 underflow
7	set if any interrupt is present

8	timer 3 underflow

IER (Reg 14)

This register mirrors the function of the IER register in the 6522. There is one extra bit assigned as interrupt enable for timer 3 (bit 8 of the IER). The bits (24 to 29) allow setting an interrupt enable delay count. Interrupts will not be enabled until after the delay count expires. Disabling interrupts always takes effect immediately.

Key Differences from a 6522.

Timers may operate in either 16-bit or 64-bit mode. This is controlled by ACR register bits 8 and 9. The default mode is 16-bit mode compatible with a 6522.

In one-shot mode the timers do not disable interrupts after the first pulse, since the timers are 64-bit and it would be quite some time before they underflow again. In other words, the system will likely have been reset before the timers underflow a second or more times.

If the timers are in 16-bit mode (the default mode) then the timer high registers are associated with timer bits 8 to 15. Otherwise if the timers are in 64-bit mode the timer high registers are associated with timer bits 32 to 63. The timer low registers are always associated with timer bits 0 to 31.

Loading the timer high register when timers are configured for 16-bit mode zeros out the upper 48-bits of the timers, thus limiting the count to a 16-bit count.

The reset input (rst_i) is active high.

The IRQ output (irq_o) is not open collector and is active high.

There is only a single active high circuit select (cs_i).