|  |  |
| --- | --- |
|  |  |
| 0 | Address bits 0 to 31 |
| 1 | address bits 32 to 63 |
| 3 | control wr + byte lane selects 0 to 15 |
| 4 | data bits 0 to 31 |
| 5 | data bits 32 to 63 |
| 6 | data bits 64 to 95 |
| 7 | data bits 96 to 127 |
| 8 to 15 | reserved |