rtfItanium

Bundle Format

Bundle Format:

|  |  |  |  |
| --- | --- | --- | --- |
| 127 120 | 119 80 | 79 40 | 39 0 |
| Template8 | Slot2 | Slot1 | Slot0 |

Instruction Formats:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Immediate7 | | | | | A | R | Immed15 | | | | | Rs16 | Opcode4 | Rd6 | | | | ML |
| Immediate7 | | | | | A | R | Immed9 | | | Rs26 | | Rs16 | Opcode4 | Immed6 | | | | MS |
| ~7 | | | | | A | R | ~9 | | | Rs26 | | 636 | Dh4 | 636 | | | | PUSH |
| Immediate7 | | | | | A | R | Immed15 | | | | | 636 | Bh4 | 636 | | | | PUSHC |
| Funct5 | | | | Immed2 | A | R | Sc3 | | Rs36 | Immed6 | | Rs16 | Opcode4 | Rd6 | | | | MLX |
| Funct5 | | | | Immed2 | A | R | Sc3 | | Rs36 | Rs26 | | Rs16 | Opcode4 | Immed6 | | | | MSX |
| 255 | | | | ~2 | ~ | ~ | ~3 | | ~6 | ~6 | | ~6 | Opcode4 | ~6 | | | | MEMDB |
| 245 | | | | ~2 | ~ | ~ | ~3 | | ~6 | ~6 | | ~6 | Opcode4 | ~6 | | | | MEMSB |
| Immediate7 | | | | | Op2 | | Immed15 | | | | | Rs16 | Opcode4 | Rd6 | | | | RI |
| Funct5 | | | | Funct22 | Op2 | | Sz3 | | Rs36 | Rs26 | | Rs16 | Opcode4 | Rd6 | | | | R3 |
| Funct5 | | | | Rg2 | o | w | ~3 | | Rs36 | Bw6 | | Bo6 | Bh4 | Rd6 | | | | BF |
| Funct5 | | | | Rg2 | o | Bw4 | | | Rs36 | Rs26 | | Bo6 | Bh4 | Rd6 | | | | BFI |
| Td20..13 | | | | | | To12..3 | | | | Rs26 | | Rs16 | Opcode4 | To2..0 | | Cond3 | | Bcc |
| Td20..13 | | | | | | To12..3 | | | | Bitno6..1 | | Rs16 | 5h4 | To2..0 | | B0 | Cn2 | BBS |
| Td20..13 | | | | | | To12..3 | | | | Immed6 | | Rs16 | Opcode4 | To2..0 | | Imm3 | | BEQI |
| ~9 | | | | | | | ~3 | | Rs36 | Rs26 | | Rs16 | 2h4 | ~2 | Cond4 | | | BRg |
| ~9 | | | | | | | ~3 | | ~6 | ~6 | | ~6 | 3h4 | ~6 | | | | NOP |
| Immediate7 | | | | | ~2 | | Immed15 | | | | | Rs16 | 8h6 | 616 | | | | JAL |
| Address30 | | | | | | | | | | | | | Opcode4 | Address6 | | | | CALL |
| Immediate18 | | | | | | | | | | 616 | | 636 | Bh4 | 636 | | | | RET |
| H | 04 | | | ~5 | | | | Cause8 | | ~2 | Imask4 | Rs16 | Fh4 | ~6 | | | | BRK |
| 0 | 14 | | | ~5 | | | | 2558 | | ~2 | 04 | 06 | Fh4 | ~6 | | | | PFI |
| 05 | | | | ~7 | | | | | ~6 | ~6 | | Rs16 | Eh4 | Sema6 | | | | RTI |
| 15 | | | | ~5 | | | | PrivLvl8 | | T2 | Imask4 | Rs16 | Eh4 | ~6 | | | | REX |
| 25 | | | | ~7 | | | | | ~6 | ~6 | | ~6 | Eh4 | ~6 | | | | SYNC |
| 35 | | | | ~7 | | | | | ~6 | ~2 | Imask4 | Rs16 | Eh4 | Rd6 | | | | SEI |
| Immediate7 | | | | | ~ | ~ | Immed9 | | | Rs26 | | Rs16 | Ch4 | Immed6 | | | | CHKI |
| ~12 | | | | | | | | | Rs36 | Rs26 | | Rs16 | Dh4 | ~6 | | | | CHK |
| Funct5 | | | | Prec4 | | | Rm3 | | Rs36 | Rs26 | | Rs16 | Opcode4 | Rd6 | | | | FLT3 |
| ~5 | | | | Prec4 | | | Rm3 | | Op6 | Rs26 | | Rs16 | 14 | Rd6 | | | | FLT2 |
| Immediate7 | | | | | Op2 | | Immediate15 | | | | | Rs16 | Opcode4 | Rd6 | | | | FLTLDI |
| Op2 | | OL2 | ~3 | | 02 | | ~3 | | Regno12 | | | Rs16 | 54 | Rd6 | | | | CSR |
| Funct5 | | | | Cmd4 | | | ~11 | | | | Tn4 | Rs16 | Opcode4 | Rd6 | | | | TLB |

Memory Loads

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | xx00 | xx01 | xx10 | xx11 |
| 00xx | LDB | LDC | LDP | LDD |
| 01xx | LDBU | LDCU | LDPU | LDDR |
| 10xx | LDT | LDO |  |  |
| 11xx | LDTU | LDOU | LEA | {MLX} |

Indexed Memory Loads

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | xx00 | xx01 | xx10 | xx11 |
| 00xx | LDBX | LDCX | LDPX | LDDX |
| 01xx | LDBUX | LDCUX | LDPUX | LDDRX |
| 10xx | LDTX | LDOX |  |  |
| 11xx | LDTUX | LDOUX | LEAX |  |

Memory Stores

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | xx00 | xx01 | xx10 | xx11 |
| 00xx | STB | STC | STP | STD |
| 01xx |  |  |  | STDC |
| 10xx | STT | STO | CAS | PUSHC |
| 11xx | TLB | PUSH | CACHE | {MSX} |

Indexed Memory Stores / Misc

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | xx000 | xx001 | xx010 | xx011 | xx100 | xx101 | xx110 | xx111 |
| 00xx | STBX | STCX | STPX | STDX |  |  |  | STDCX |
| 01xx | STTX | STOX | CASX |  |  |  | CACHE |  |
| 10xx |  |  |  |  |  |  |  |  |
| 11xx | MEMSB | MEMDB |  |  |  |  |  |  |

Flow Control

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | xx00 | xx01 | xx10 | xx11 |
| 00xx | Bcc | BLcc | BRcc | NOP |
| 01xx | FBcc | BBc | BEQ # | BNE # |
| 10xx | JAL | JMP | CALL | RET |
| 11xx | CHK # | CHK | RTI / REX | BRK |

Floating Point

Opcode4 - Bits 6 to 9

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | xx00 | xx01 | xx10 | xx11 |
| 00xx |  | {FLT2} | FAND # | FOR # |
| 01xx | FMA | FMS | FNMA | FNMS |
| 10xx |  |  |  |  |
| 11xx |  |  |  |  |

Op6 – Bits 22 to 27

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x |  |  |  |  | FADD | FSUB | FCMP |  | FMUL | FDIV |  |  | FAND | FOR |  |  |
| 1x | FMOV |  | FTOI | ITOF | FNEG | FABS | FSIGN | FMAN | FNABS | FCVTSD |  | FCVTSQ | FSTAT | FSQRT |  |  |
| 2x | FTX | FCX | FEX | FDX | FRM |  |  |  |  | FCVTDS |  |  |  |  |  |  |
| 3x |  |  |  |  |  |  | FSYNC |  | FSLT | FSGE | FSLE | FSGT | FSEQ | FSNE | FSUN |  |

|  |  |  |
| --- | --- | --- |
| Unit |  |  |
| 1 | Branch |  |
| 2 | Integer |  |
| 3 | Floating Point |  |
| 4 | Memory Load |  |
| 5 | Memory Store |  |
| 6 |  |  |
| 7 |  |  |

ALU

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x |  |  | {R3} | {R3} | ADD | CSR | CMP | CMPU | AND | OR | XOR | {BF} | BLEND |  |  |  |
| 1x | SLT | SGE | SLE | SGT | SLTU | SGEU | SLEU | SGTU | SEQ | SNE |  | {BF} |  |  |  |  |
| 2x | MUL | MULU | DIV | DIVU | MOD | MODU |  |  | MADF |  |  | {BF} |  |  |  |  |
| 3x | FXMUL |  |  |  | ADDS1 | ADDS2 | ADDS3 |  | ANDS1 | ANDS2 | ANDS3 | {BF} | ORS1 | ORS2 | ORS3 |  |

ALU – R3 Format

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | MULH | MULUH | ADDV | SUBV | ADD | SUB | CMP | CMPU | AND | OR | XOR |  | NAND | NOR | XNOR |  |
| 1x | SLT | SGE | SLE | SGT | SLTU | SGEU | SLEU | SGTU | SEQ | SNE | MOV | CMOVNZ | MIN | MAX | PTRDIF |  |
| 2x | MUL | MULU | DIV | DIVU | MOD | MODU |  |  | MADF | MUX |  |  |  |  |  |  |
| 3x | FXMUL | FXDIV | SHL | ASL | SHR | ASR | ROL | ROR | SHL # | ASL # | SHR # | ASR # | ROL # | ROR # | BMM |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Template | Slot0 | Slot1 | Slot2 |
| 00 | Mem Unit | Int Unit | Int Unit |
| 01 | Mem Unit | Int Unit | Int Unit |
| 02 | Mem Unit | Int Unit | Int Unit |
| 03 | Mem Unit | Int Unit | Int Unit |
| 04 | Mem Unit |  |  |
| 05 | Mem Unit |  |  |
| 06 |  |  |  |
| 07 |  |  |  |
| 08 | Mem Unit | Mem Unit | Int Unit |
| 09 | Mem Unit | Mem Unit | Int Unit |
| 0A | Mem Unit | Mem Unit | Int Unit |
| 0B | Mem Unit | Mem Unit | Int Unit |
| 0C | Mem Unit | FP Unit | Int Unit |
| 0D | Mem Unit | FP Unit | Int Unit |
| 0E | Mem Unit | Mem Unit | FP Unit |
| 0F | Mem Unit | Mem Unit | FP Unit |
| 10 | Mem Unit | Int Unit | Branch Unit |
| 11 | Mem Unit | Int Unit | Branch Unit |
| 12 | Mem Unit | Branch Unit | Branch Unit |
| 13 | Mem Unit | Branch Unit | Branch Unit |
| 14 |  |  |  |
| 15 |  |  |  |
| 16 | Branch Unit | Branch Unit | Branch Unit |
| 17 | Branch Unit | Branch Unit | Branch Unit |
| 18 | Mem Unit | Mem Unit | Branch Unit |
| 19 | Mem Unit | Mem Unit | Branch Unit |
| 1A |  |  |  |
| 1B |  |  |  |
| 1C | Mem Unit | FP Unit | Branch Unit |
| 1D | Mem Unit | FP Unit | Branch Unit |
| 1E |  |  |  |
| 1F |  |  |  |

Templates

## ADD - Addition

**Description**:

Add two values. The first operand must be in a register. The second operand may be in a register or may be an immediate value specified in the instruction.

**Instruction Format**:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Immediate7 | 02 | Immed15 | Rs16 | 44 | Rd6 | RI |

**Instruction Format**:

The following instruction format adds three registers together.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 25 | 02 | 02 | Sz3 | Rs36 | Rs26 | Rs16 | 24 | Rd6 | R3 |

**Clock Cycles:** 0.33

**Execution Units:** All ALU’s

**Exceptions**: none

**Notes**:

For parallel operation forms the registers are treated as if they were a group of registers corresponding to the size selected. And the same operation is performed on each part of the register. For parallel forms the entire register is updated.

|  |  |
| --- | --- |
| Sz3 |  |
| 0 | reserved |
| 1 | reserved |
| 2 | reserved |
| 3 | reserved |
| 4 | Byte Parallel |
| 5 | Char Parallel |
| 6 | Half Parallel |
| 7 | Word |

## BFINSI – Bitfield Insert Immediate

**Description**:

A bitfield is inserted into the target register Rd by combining a value read from Rs3 with a constant shifted to the left. The bitfield may not be larger than six bits. To accommodate a larger field multiple instructions can be used, or a value loaded into a register and the BFINS instruction used.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 45 | Rg2 | o | Bw4 | Rs36 | Imm6 | Bo6 | Bh4 | Rd6 |

**Instruction Format**:

|  |  |
| --- | --- |
| Rg2 Bit |  |
| 0 | 1= Bo is a register spec, 0 = Bo is a six bit immediate |
| 1 | 1. = Bw is a register spec, 0 = Bw is a six bit immediate |

Rg[1] bit should always be clear for this instruction

**Clock Cycles**: 1

**Execution Units:** ALU #0 Only

**Exceptions**: none