Libre Silicon

David Lanzendörfer (leviathan)

Lanceville Technologies Group Ltd.

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What we do

- We make **truely free silicon** through an open manufacturing process
- Breaking the monopoly of big semiconductor manufacturers
- Eliminating the vendor lock-in to big semiconductor manufacturers
- Making semiconductor development super quick and inexpensive

What we do

- Introducing the LSPL (LibreSilicon public license)
- Attracting commercial design houses to develop **free silicon**
- Eliminating NDAs[1] from hardware design flow
- Eliminating hardware back doors

[1] Non-disclosure Agreements

Why are we doing this?

- MPWs[2] cost around 20'000 USD
- MPWs take around 2-9 months
- All manufacturers want NDAs (some NDAs even have NDAs!)
- Your design for a vendor process contains process specific design quirks (also under NDA!)
- No manufacturer provides the GDS2 files in order to manufacture the designs in your basement (there is **no** free silicon yet)
- You can't even publish your own designs!

[2] Multi Project Wafer

Imagine you like to manufacture your own chip

- You're going to a foundry
- Signing at least 3 NDAs, one for the PDK[3], one for the standard cell libary and one for purchase details
- Invest a lot of money for the layout development and the mask set
- And have some reasons to change the foundry service…

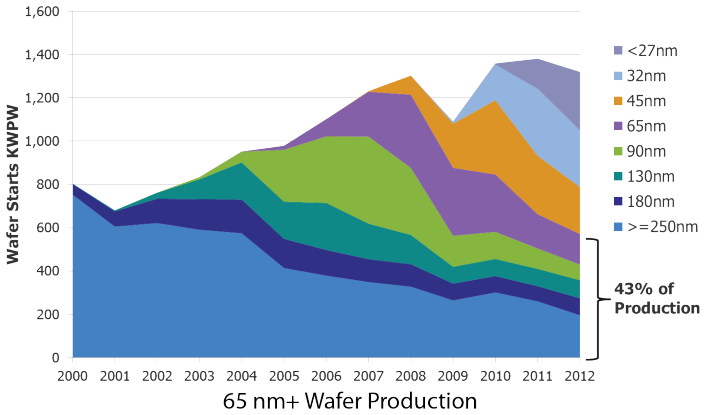
[3] Process design kit

Well, you're fucked. . .
someecards
user card

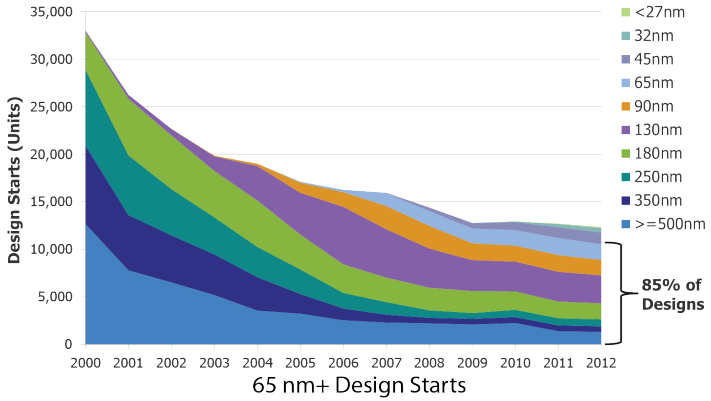
Reasons are

- The technology is completely different
- The standard cells are mostly different
- The mask does not leave the foundry
- And even do not match another technology in another foundry
- Well, you've burned the costs for layout and mask set

Closed silicon market



65 nm+ Wafer Production



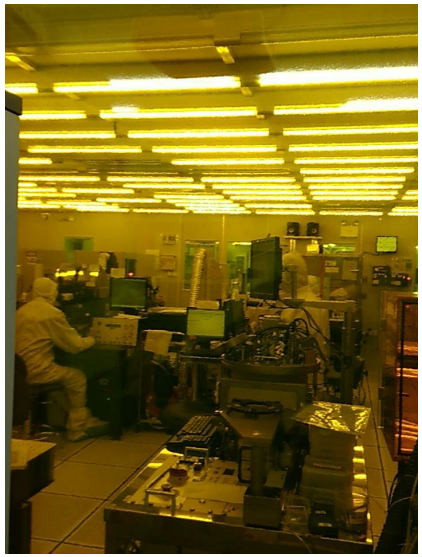
65 nm+ Design Starts

4

[4] http://semimd.com/favre/2016/08/24

How we do it

- Introducing an open source chip manufacturing process standard specification
- Introducing a fully integrated free EDA for ASIC design[5]
- Renting the clean room and manufacturing equipment at HKUST every 2 weeks for around 12 hours



Libre Silicon EDA Tools

- QtFlow EDA[6]
  - EDA suite written in Qt5
  - Wave viewer
  - Planned:
    - Integration of higher level HDLs (CLash)
    - Plugins through PythonQt
- Icarus Verilog simulation[7]
- QRouter maze router[8]
- GrayWolf floor planner[9]
- Libre silicon compiler[10]

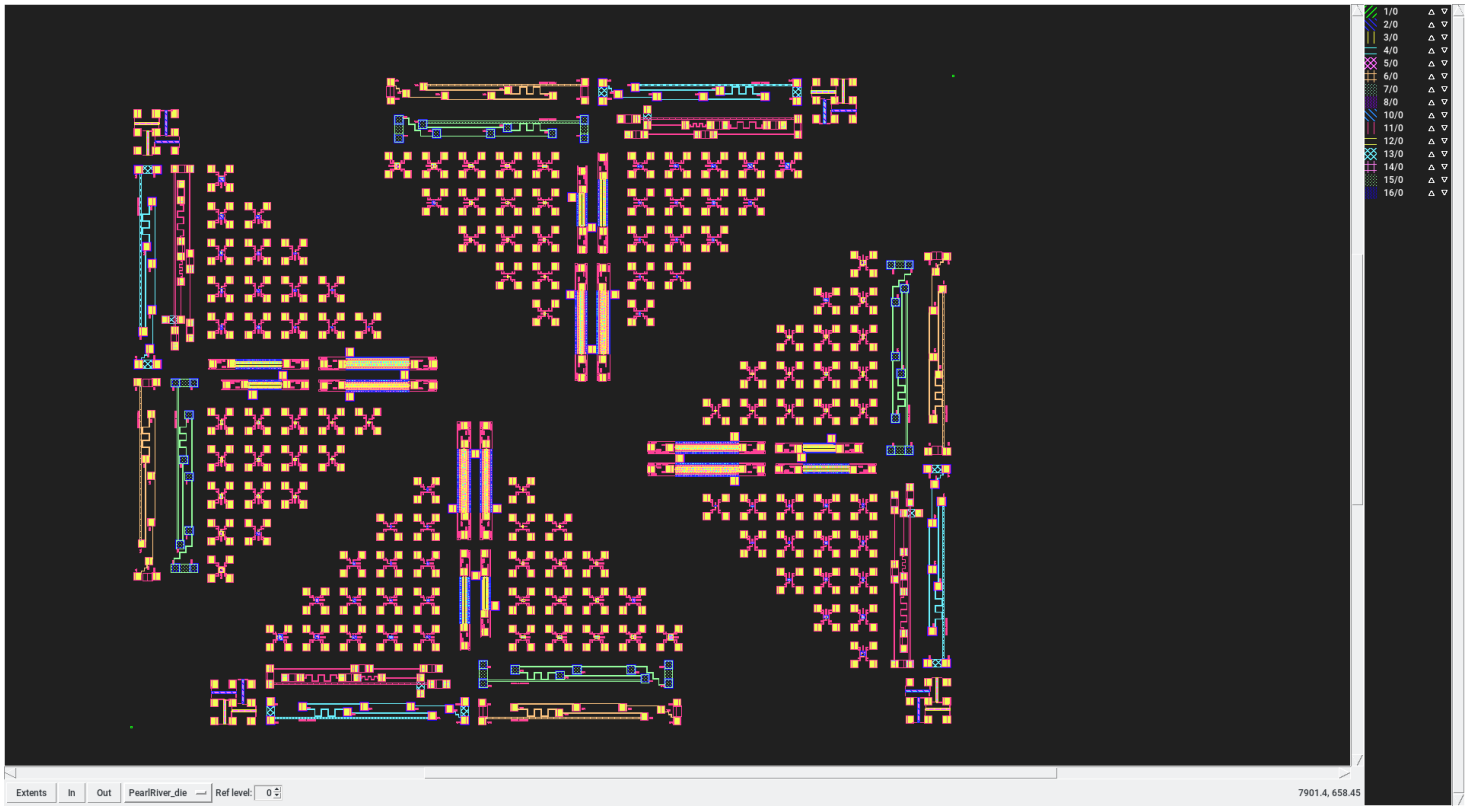
[6] https://github.com/leviathanch/qtflow
[7] http://iverilog.icarus.com
[8] https://github.com/leviathanch/qrouter
[9] https://github.com/leviathanch/graywolf
[10] https://github.com/foshardware/lsc.git

Helpful links

- Mailing list
  `https://list.o2s.ch/mailman/listinfo/libre-silicon-devel`
- Process
  `https://github.com/libresilicon/libresiliconprocess`
- Test wafer (珠江芯片一号)
  `https://github.com/chipforge/PearlRiver`
- Standard cell library
  `https://github.com/chipforge/StdCellLib`
- Layout software/EDA
  `https://github.com/leviathanch/qtflow`

You can help :-)

PearlRiver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PearlRiver_die
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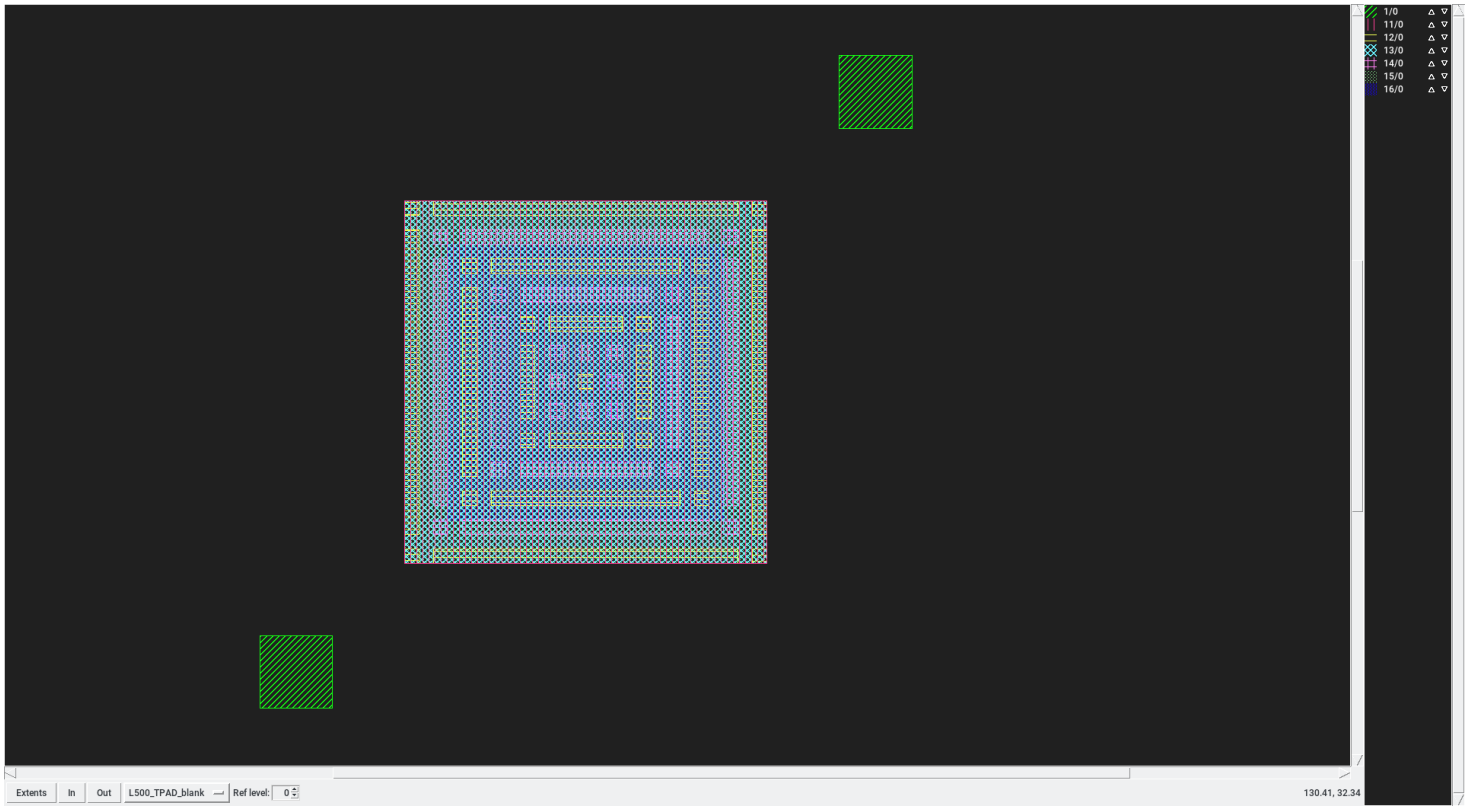
Bonding pad


1/0
11/0
12/0
13/0
14/0
15/0
16/0
Extents
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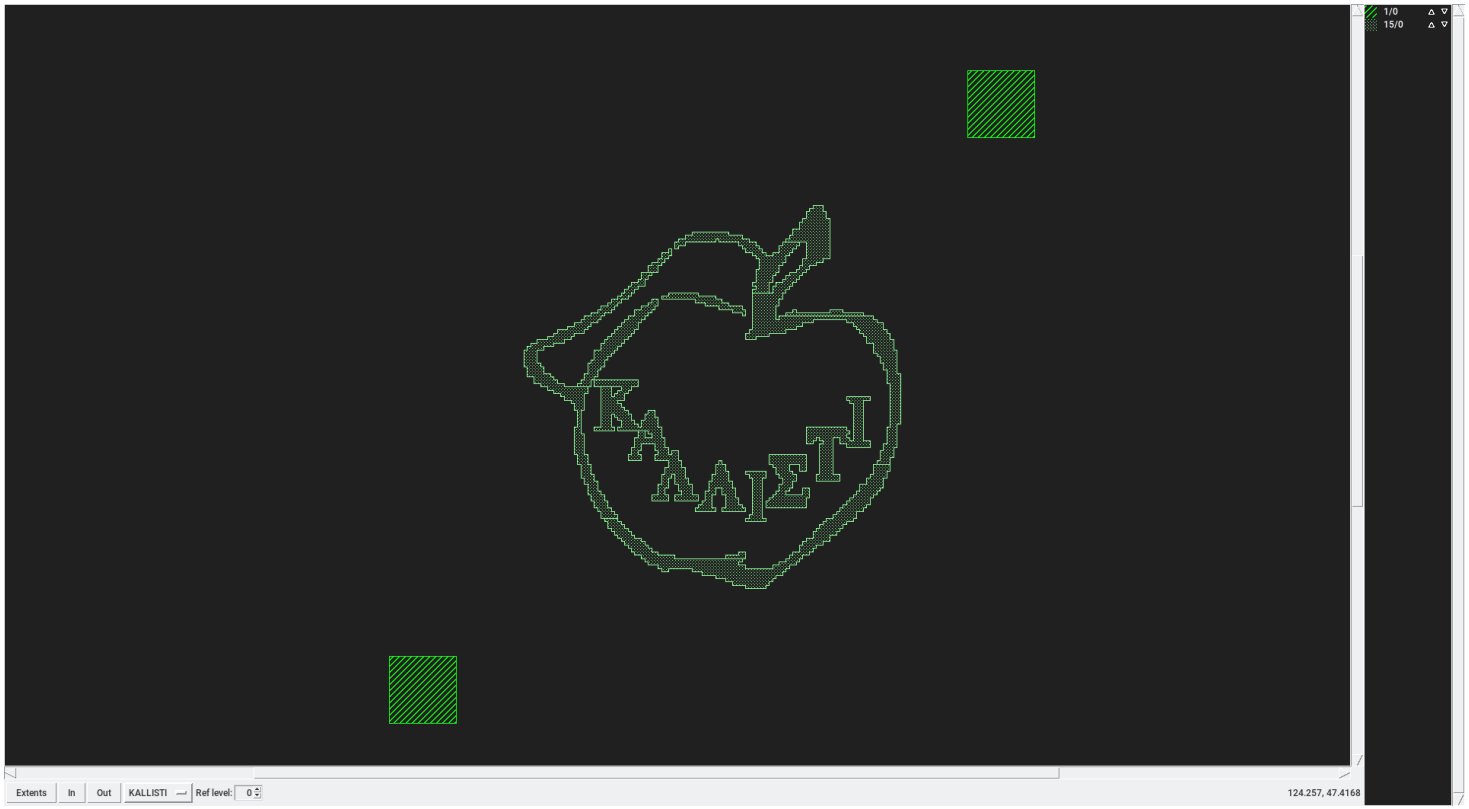
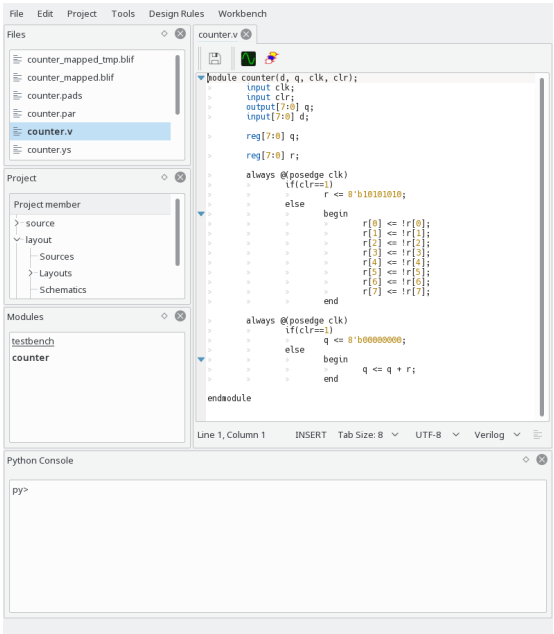
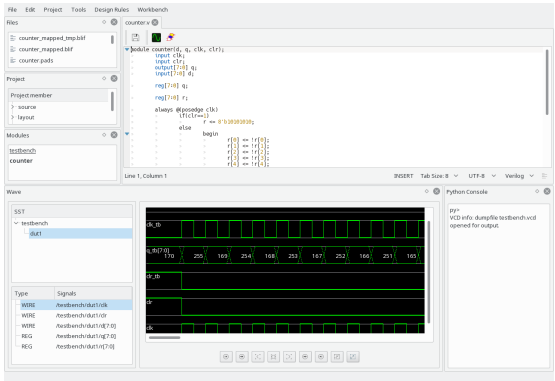
Out
L500_TPAD_blank
Ref level:
0
130.41, 32.34

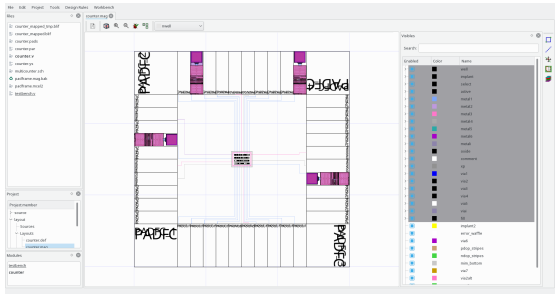
Holy apple of divine discord



QtFlow screen shots







Make your self independend

- You know about semiconductor manufacturing? Help us design an open and free process
- Fit with licensing? Help us with the LSPL
- You can help in other places if you like :-)

TODO

- Shrink PearlRiver(珠江芯片一号) test wafer
- Next review before ordering the masks
- Documentation about what and how we like to measure parameters
- Transfer parameters into Spice BSIM3v3 models
- Manufacture a couple of wafers and doing measurement at HKUST
- Process refinement
- Finish standard cells
- Install process foundry for mass production
- Manufacture first microcontroller chip in 2019 (北角芯片)

License

- Free and open source - while for real hardware GPL or BSD does not work.
- Others like CERN we already evaluated.
- We like that everybody can use the process (even in your basement),
- Including universities and real foundries.

Transfer-able

- Everybody should have the possibility to transfer own designs into other foundries.
- Foundries can compete in production cost and / or corporate.
- Usable for education also, while even analog designs heavy depends on process parameters.

The history so far

- 2017
- 2018

2017

- leviathan opened a possibility to rent a clean room at Hong Kong University of Science and Technology
- leviathan got some funding
- leviathan gave a lightning talk in Leipzig at the 34th Chaos Communication Congress

2018

- We developed the first version of our 1um LibreSilicon process
- We are working on the standard cell library
- We already held a tool chain hackathon
- We are layouting a first test wafer(珠江芯片一号) for technology parameter measurement
- Currently reviewing the test wafer and compress the layout now for more chips per wafer.

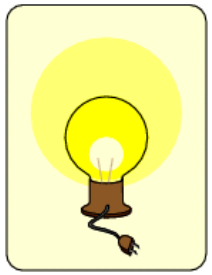
Links

- Process
  `https://github.com/libresilicon/libresiliconprocess`
- Test wafer (珠江芯片一号)
  `hhttps://github.com/chipforge/PearlRiver`
- Standard cell library
  `hhttps://github.com/chipforge/StdCellLib`
- Tool Chain
  `hhttps://github.com/leviathanch/qtflow`

Community projects

Icarus Verilog

Yosys Open SYnthesis Suite

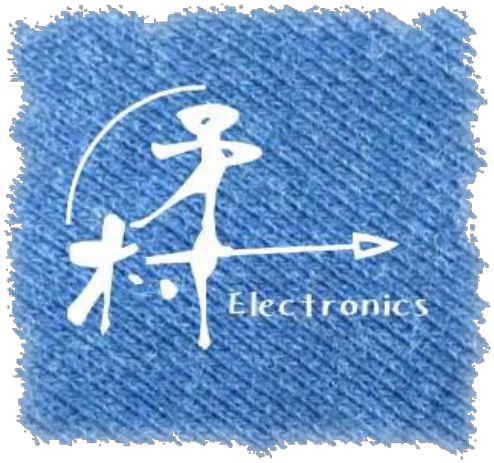


Companies and institutions

香港科技大學
THE HONG KONG
UNIVERSITY OF SCIENCE
AND TECHNOLOGY

NFF
Nanoelectronics Fabrication Facility

efabless.com



Mumble

- Weekly voice only conference call over Mumble[11]
- Every Sunday 21 p.m Hong Kong Time
- Server 109.109.202.102, Port 64738

[11] `https://www.mumble.com/mumble-download.php`

Contact me

- E-Mail (preferred): david.lanzendoerfer@lanceville.cn
- Check whether I'm hanging around in Mumble (WARNING: Sometimes there are strange people there, it's public)
- IRC:
  - Channel ##lsa on irc.freenode.net belongs to LibreSilicon alliance
  - I'm hanging around on irc.freenode.net as leviathanch

Thanks!

非常感谢你们!

Thank you very much!