Design and Analysis of SRAM Using Opensource EDA Tools

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*Abstract—The paper constitutes of the design and analysis of 6-Transister* *Static Random-Access Memory (SRAM). It is static and volatile, implying data retention persists for as long as the device is powered without any form of a refresh, however, once the power is cut, data will be lost. It is random access, meaning the next memory location that can be read or written to does not depend on the last access location. The SRAM has been designed to achieve an access time of less than 2.5ns and a memory array of 1024\*32bits. The SRAM has been designed using 180nm CMOS technology. The Applications have been mentioned below.*

Keywords— Static Random-Access Memory, 6-Transister, static, volatile, access time, CMOS, memory array

# Introduction

In modern day computer systems, the memory has a very important role in storing large amount of data values as well as program instructions. A large portion i.e. more than half of the transistors present on polysilicon chip has been dedicated to cache memory. This ratio is expected to further increase. [2] In this paper we are going to design SRAM based cache memory which is mainly used due to its High performance and Low power design in comparison with the DRAM (Dynamic Random-Access Memory). 6T SRAM is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered.[1]

# SRAM-Basic Architecture and Working

## SRAM Architecture

Fig.1 SRAM architecture

Basic SRAM memory array consists of N-words i.e. N number of rows in memory array and each word is M-bits wide i.e. M number of columns in memory array. A very large memory array is divided into a smaller memory arrays, which minimizes the amount of power dissipation, delay, and reduces the overhead caused by peripheral circuitry. Row and column decoders are used for selecting a particular word and bit. A Sense amplifier is present below the column decoder which gives the I/O ports the amplified output of a particular bit line. There is a pre-charge circuitry which is present for each pair of bit lines, which pre-charges the bit lines equivalently. Refer above Fig.1.[2]

## 6T SRAM Basic Structure

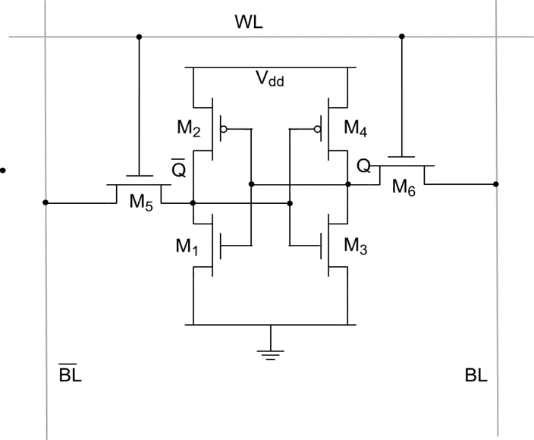
Each bit in a 6T SRAM requires 6 transistors. Two NMOS pass transistors for Read/Write operations which are also known as access transistors. Four transistors for the two-inverter latch.

Fig.2 6T SRAM Structure

From Fig.2 M5 and M6 are the access transistors and M1, M2, M3 and M4 are the two inverter transistors. The Bit lines as well as the word line are connected to the access transistors for Read/Write on the latch [4][5].

## 6T SRAM Working

Read Operation:

Assume Q to be storing the value 1 and assume that the bit lines (BL and ~BL) are pre-charged. The Read pulse is given through the word line (WL) and the access transistors (M5 & M6) are enabled after word line delay. The values of Q and ~Q are transferred to bit lines by leaving BL at its pre-charge value and discharging ~BL through M5-M1[4].And thus the value of Q is read via the bit lines through a sense amplifier and the output is driven to the I/O port via the sense amplifier.

Write Operation:

In order to change the value inside the latch we must change the value of the bit lines. The bit lines are set to the desired value due to the bit line drivers being stronger than weak transistors in the SRAM cell itself [3].Let us assume the bit line BL is set to logical 1 and ~BL to logical 0 .Now when write pulse is given from word line, the Q=1 discharges through bit line and becomes 0 while the ~Q cannot be pulled to a logical high by bit line due to the read stability criteria, but new value of ~Q is set by access transistor M6 which is connected to the input of the ~Q inverter [4][3].

Both Read and Write operations are done by proper sizing of transistors.

## Implementation of 6T SRAM in Open-Ram compiler

Memory Compiler requires 3 fundamental inputs:

1. Design Rules- DRC and LVS(PDK’s)
2. Custom Cells
3. Configuration Files- Compiler Provided

As a memory designer we need to design all the custom cells.

Custom cells to design are as follows:

1. 6T single SRAM cell
2. Synchronous DFF- For Timing/Control logic
3. Sense Amplifier
4. Tri Gate Buffer-For Data Output
5. Write Driver

Steps to Implement custom cells:

1. Circuit design on E-sim
2. Pre-layout Simulations using ng-spice
3. Layout Design using Magic
4. Post-Layout Simulations using ng-spice

# Applications of SRAM

SRAM are usually more expensive, faster and less power hungry than DRAM. Due to the high circuit complexity they are not used in high density and low-cost applications.

* Low power and High-Speed SRAM are usually used in high performance microprocessors (mainly used in small cache memories). They are also widely used System on Chip (SOC’s).
* Widely used in portable devices such as smartphones, portable PSD, etc.
* They are used in Electronic Dictionary/Data Bank. They are also used in MP3 players, GSM/CDMA. They are used in High Speed Network devices such as modems and routers.
* They are also used in DVR and CCTV applications.

# References

[1] Abhishek Agalet “6T SRAM Cell: Design And Analysis” Int. Journal of Engineering Research and Applications ,Vol. 4, Issue 3( Version 1), March 2014.

[2] J. Rabaey, A. Chandrakasan, and B. Nicolic, Digital Integrated Circuits A Design Perspective, 2nd ed.Prentice Hall, 2003.

[3] Ajay Kumar Dadoria, Arjun Singh Yadav, C.M Roy,“Comparative Analysis Of Variable N-T Sram Cells” International Journal of Advanced Research in Computer Science and Software Engineering,Volume 3, Issue 4, April 2013.

[4] Neil H.E. weste & David Money Harris “CMOS VLSI Design: A Circuits and Systems Perspective” ISBN: 0321149017/9780321149015Third edition, Pearson Education, 2005.

[5] G. Shivaprakash1\* and D. S. Suresh2“Design of Low Power 6T-SRAM Cell and Analysis for High Speed Application”, Indian Journal of Science and Technology, Vol 9(46).