

# REALTEK

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**RTD1395DB-VA1-CG**

**RTD1395DC-VA1-CG**

**RTD1395PB-VA1-CG**

## **4K UHD MULTIMEDIA SOC**

### **DATASHEET**

**(CONFIDENTIAL: Development Partners Only)**

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## USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTD1395 controller ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

## REVISION HISTORY

Revision	Release Date	Summary
1.0	2018/09/12	First release.

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## 1. General Description

The RTD1395DB/RTD1395DC/RTD1395PB are cutting-edge High Definition Media Processor SoCs (System-on-Chip) for Consumer Electronics featuring a Trusted Execution Environment with an independent secure operating system, VP9 and H.265 decoding up to Ultra HD, and H.264 FHD media Decoding and Encoding with multiple formats, Wireless/Wired Networking, DTV, and a comprehensive set of High-Speed peripherals.

The RTD1395 is equipped with a high-performance quad-core CPU, ARM Cortex-A53, with 512K L2 Cache embedded. The RTD1395 also integrates an efficient ARM Mali-470 Graphic Processing Unit (GPU) to accelerate 2D and 3D graphics processing. For acceleration of the OSD and 2D user interface, the built-in Streaming Engine of the RTD1395 provides commonly used drawing functions. The CPU is dedicated to applications, while most of the functions of the RTD1395 utilize separate hardware circuits to provide efficiently optimized systems. The Video DSP of the RTD1395 is dedicated to manipulating, decoding video streams in various formats, e.g. decoding 4K2K H.265, Full HD MPEG1/2/4/H.264/H.264 MVC, AVC/VC-1, VP8, VP9, AVS, AVS Plus, HD JPEG, etc. Video DSP can also handle encoding of up to Full HD with H.264 format. Video decoding and encoding can run simultaneously.

Additionally, video post processing of the RTD1395 is handled by a video processing subsystem that supports 3D de-interlacing, video scaling up to 4K2K and so on. Audio decoding is carried out by an Audio DSP that is capable of decoding a set of audio formats, e.g. DTS HD, Dolby® Digital Plus, TrueHD, and other popular formats. The Audio DSP also performs audio post processing.

The RTD1395 provides a secure environment for a rich operating system, bringing UHD and HDR content to big screens. A secure video path and secure storage are fundamentally essential to secure systems. With the deployment of ARM TrustZone and the implementation of a proprietary security mechanism, the RTD1395 protects video and highly confidential information from leaks. An independent secure operating system runs on the RTD1395. In addition, the RTD1395 hardware offers a cryptography engine, true random number generator, and sufficient One-Time Programmable ROM (OTP) space, which are also substantial elements for a Trusted Execution Environment.

The RTD1395 supports a comprehensive set of peripherals. An HDMI Transmitter with PHY are integrated in the RTD1395. The HDMI interface supports HDCP. Other interfaces include USB2.0 Host/Device with PHY integrated, NAND/NOR/eMMC flash controller, Card reader supporting SD/MMC, high-speed UART for Bluetooth, Gigabit Ethernet MAC, 4-bit SDIO, IrDA Receiver, and dual transport stream interfaces.

The RTD1395 is designed as a cost efficient solution for Ultra High Definition Media Player, OTT Streaming Player, Android TV, DTV Set-top box, or Miracast Wireless Display Adapter.

## 2. Features

- System and Peripherals
  - ◆ ARM Cortex-A53 Quad-Core processor with floating-point unit and NEON SIMD engine embedded, supporting the 64/32-bit ARMv8 architecture
  - ◆ 512KB L2 Cache
  - ◆ ARM TrustZone for Trusted Execution Environment (TEE) with independent secure operating system and integrated secure hardware
  - ◆ Supports OpenGL ES1.1/2.0
  - ◆ Video DSP with HW acceleration
  - ◆ Audio DSP with HW acceleration
  - ◆ Supports up to 4GB DDR4/DDR3 SDRAM with dual channels of 16-bit data interface
  - ◆ Supports Serial Flash with dual I/O data interface
  - ◆ Supports NAND Flash with maximum 12-bit ECC
  - ◆ Supports eMMC 5.0
  - ◆ Boot-ROM and OTP (One-Time Programmable ROM) for Secure-Boot and Key storage
  - ◆ Integrates 10/100 Ethernet MAC and PHY and gigabit Ethernet MAC
  - ◆ Integrates triple USB2.0 High Speed OTG controller and PHY with support for USB Type-C receptacle
  - ◆ Supports SDIO 3.0 interface
  - ◆ Supports SD3.0 interface
  - ◆ Supports SGMII
  - ◆ Supports PCI Express 2.0
  - ◆ Supports UART/I2C/GPIO/IrDA Rx/EJTAG
- Video and Picture Decoding Functions
  - ◆ H.265 MP@L5.1 Main Tier
  - ◆ VP9 Profile 2
  - ◆ MPEG1, VCD 1.0/2.0, SVCD
  - ◆ Supports HD MPEG2 (up to MP@HL 1080i), ISO/IFO/VOB/TS
  - ◆ Supports HD MPEG4 SP/ASP (720p/1080i/1080p), Xvid
  - ◆ H.264 MP@L5.1
  - ◆ H.264 MVC SHP@L4.1
  - ◆ VC-1 SP, MP, AP@L3
  - ◆ AVS JZ@L6.2, AVS+ 1080@60P
  - ◆ H.263 Profile0/3@L70 1080@60P
  - ◆ Sorenson Spark L70
  - ◆ VP8 1080@60P
  - ◆ HD JPEG with 32K x 32K maximum resolution
  - ◆ Full-pixel JPEG decode with high resolution zoom-in
  - ◆ Video up-scaling from SD to Ultra HD (720p/1080i/1080p/2160p)
  - ◆ Supports 24/30/36 bits deep color
- Video and Picture Encoding Functions
  - ◆ MPEG 4 SP@L5
  - ◆ H.264 BP, MP, HP@L4.2
  - ◆ H.264 MVC SHP 1080@30P
  - ◆ H.263 Profile3@L70 1080@60P
  - ◆ HD JPEG in high resolution
- Audio Interfaces and Functions
  - ◆ Built-in Audio Codec with 24-bit resolution

- ◆ One I2S interface (2 channels) for Audio output
- ◆ One I2S interface (2 channels) for Audio input
- ◆ IEC 60958 (SPDIF) digital audio output
- ◆ 7.1 CH down-mix
- ◆ MPEG I Layer 1, 2, 3 (2-CH) and MPEG II Layer 1, 2 (Multi-Channel)
- ◆ LPCM, ADPCM, ALAC, FLAC, AAC, WAV, AIFF, VSELP, and OGG Vorbis
- ◆ DTS HD, Dolby Digital Plus, TrueHD (Licensee Only)
- ◆ WMA/WMA Pro, Dolby Digital AC3, and DTS (Licensee Only)
- ◆ LPCM/ADPCM/MP3/AAC audio recording
- ◆ DTS Broadcast capable (Licensee Only)
- ◆ Dolby Digital Consumer Encoder capable (Licensee Only)

- Video Interfaces and Functions
  - ◆ TV encoder with 12-bit video D/A converters
  - ◆ NTSC and PAL TV systems
  - ◆ Composite analog video output
  - ◆ Simultaneous SD and HD outputs
  - ◆ HDMI v2.0b transmitter with CEC, support for 3D over HDMI
  - ◆ 3D De-interlacer
  - ◆ Bitmap OSD
  - ◆ Support for CGMS-A, WSS
- Power Design
  - ◆ Support for Dynamic Voltage Frequency Scaling
- Miscellaneous
  - ◆ Thermal sensor
  - ◆ Voltage sensor
- Package: 15mm x 15mm, TFBGA 406 with 0.65mm ball pitch

### 3. Block Diagram

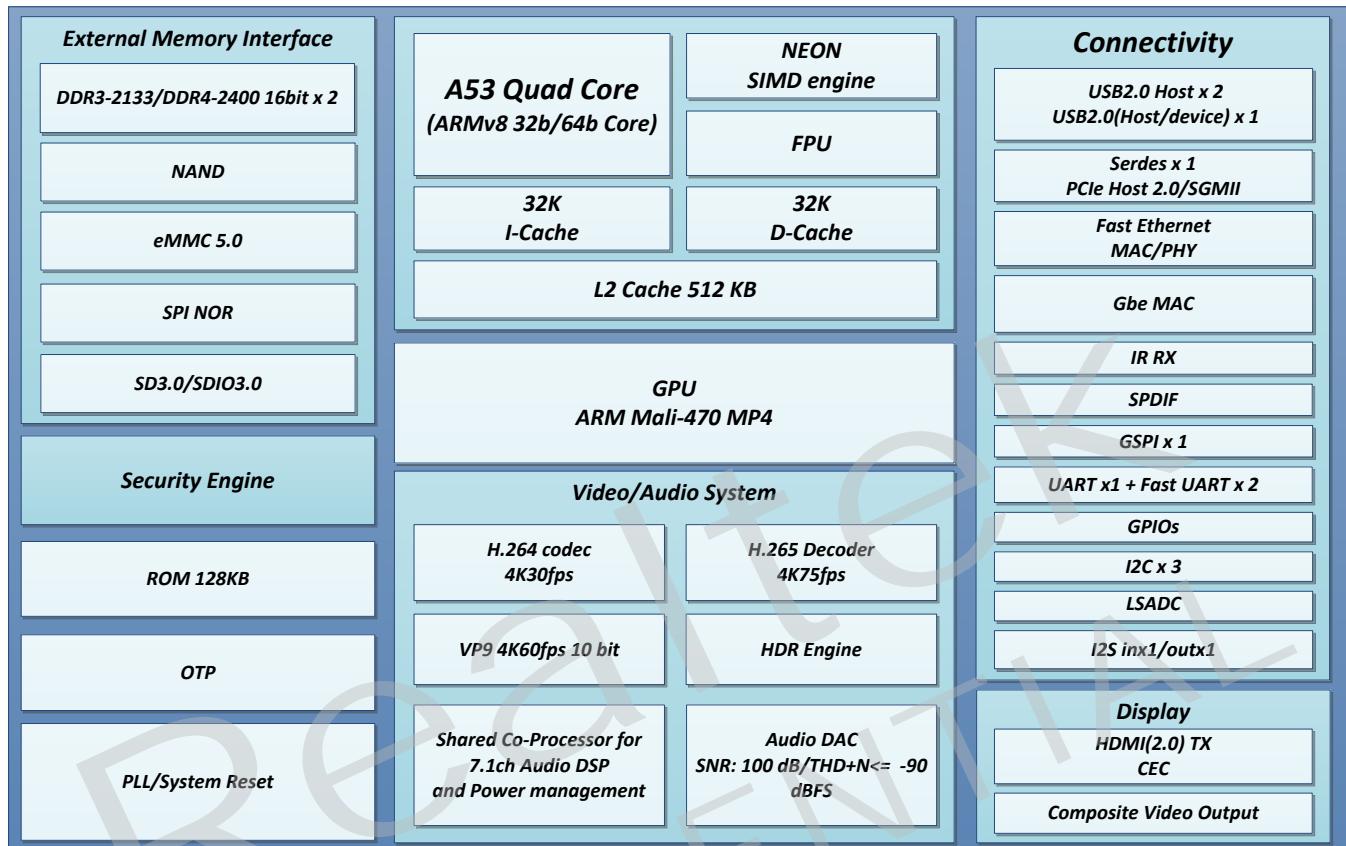


Figure 1. Block Diagram

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For details, contact Dolby Labs at: Dolby Labs, 100 Potrero Avenue, San Francisco, CA 94103, USA.

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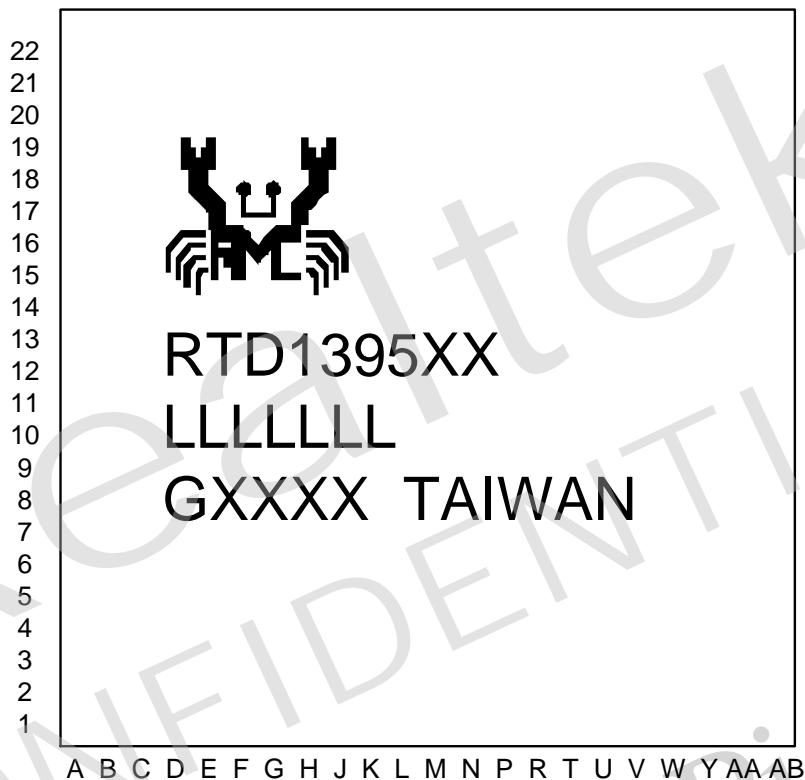
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## 5. Pin Assignments

### 5.1. Package Identification

XX in the model number indicates DB, DC, or PB model. Green package is indicated by the 'G' in GXXXX (Figure 2)



**Figure 2. Package Identification**

## 5.2. Pin Assignments (Bottom View)

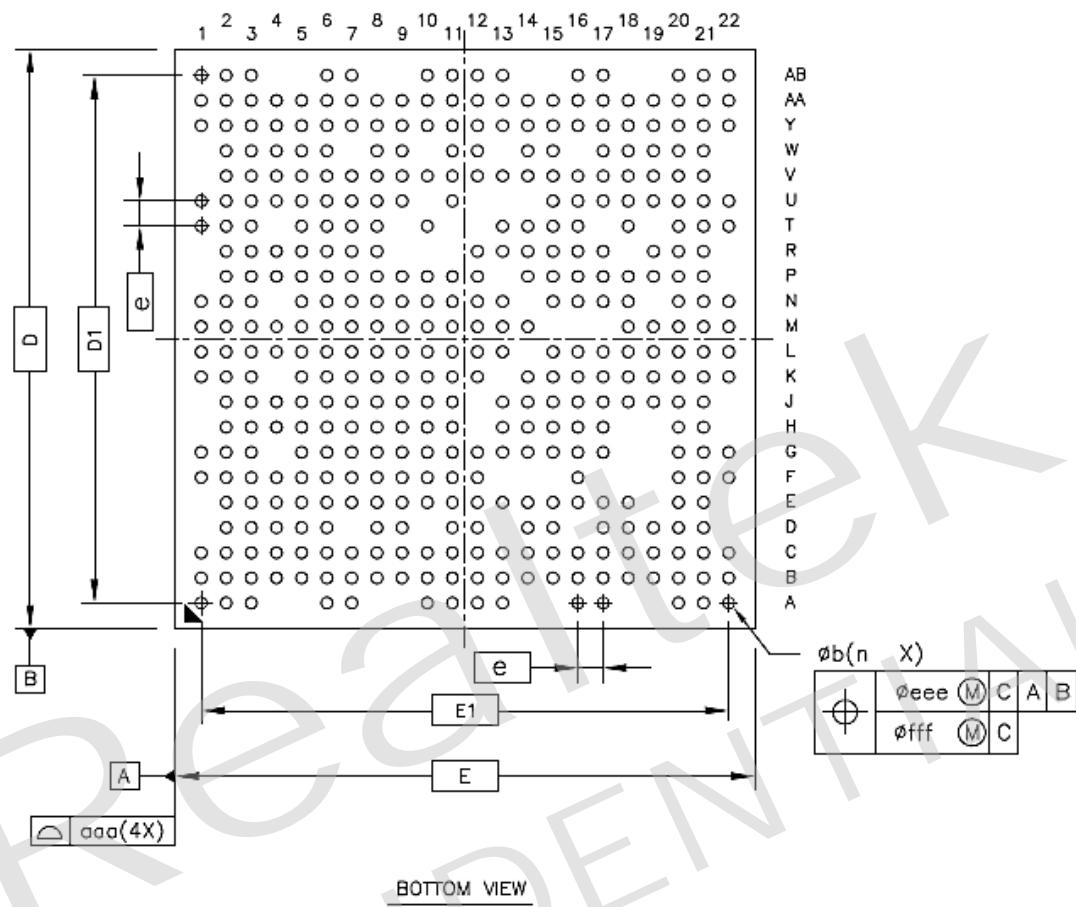


Figure 3. Pin Assignments (Bottom View)

## 6. Pin Descriptions

DI: Digital Input

AI: Analog Input

DO: Digital Output

AO: Analog Output

DB: Digital Bi-Directional

AB: Analog Bi-Directional

GND: Ground

PWR: Power Supply

**Table 1. Pin Descriptions**

Pin No.	Pin Name	I/O	Default Value	Description
A1	DDR4_DQ29	DB	-	DDR4 Data 29
	DDR3_DQ30	DB		DDR3 Data 30
A2	DDR4_DQ25	DB	-	DDR4 Data 25
	DDR3_DQ28	DB		DDR3 Data 28
A3	GND	GND	-	Digital Ground
A6	DDR4_DQ28	DB	-	DDR4 Data 28
	DDR3_DQ27	DB		DDR3 Data 27
A7	DDR4_DQ16	DB	-	DDR3/DDR4 Data 16
A10	GND	GND	-	Digital Ground
A11	EMMC_DATA_4	DB	1	eMMC Data 4
	NF_D2	DB		NAND Flash Data 2
A12	EMMC_DATA_3	DB	1	eMMC Data 3
	NF_D1	DB		NAND Flash Data 1
A13	GND	GND	-	Digital Ground
A16	RESET_N	DI	1	Chip Reset, Schmitt Trigger Input
A17	GPIO_1	DB	1/5V tolerance	General Purpose I/O 1
A20	UR0_RX	DI	1	UART0 Receive Data Input
A21	TP1_DATA	DI	1	Secondary Transport Stream Input Data
A22	TP1_VALID	DI	1	Secondary Transport Stream Input Data Valid
B1	DDR4_DQ31	DB	-	DDR4 Data 31
	DDR3_DQ26	DB		DDR3 Data 26
B2	GND	GND	-	Digital Ground
B3	DDR4_DQS3_c	DB	-	DDR3/DDR4 DQ[31:24] Data Strobe
B4	GND	GND	-	Digital Ground
B5	DDR4_DQ24	DB	-	DDR4 Data 24
	DDR3_DQ31	DB		DDR3 Data 31
B6	DDR4_DQ26	DB	-	DDR4 Data 26
	DDR3_DQ29	DB		DDR3 Data 29
B7	DDR4_DQ20	DB	-	DDR4 Data 20
	DDR3_DQ18	DB		DDR3 Data 18
B8	DDR4_DQ18	DB	-	DDR4 Data 18
	DDR3_DQ22	DB		DDR3 Data 22
B9	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
B10	EMMC_DATA_2	DB	1	eMMC Data 2
	NF_D5	DB		NAND Flash Data 5
B11	EMMC_DATA_0	DB	1	eMMC Data 0
	NF_D3	DB		NAND Flash Data 3
B12	EMMC_DATA_5	DB	1	eMMC Data 5
	NF_D0	DB		NAND Flash Data 0
B13	EMMC_CMD	DB	1	eMMC Command Line
	NF_RD#	DO		NAND Flash Read Enable
B14	SPI_SO	DB	-	Serial Flash Data Output (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)
	NF_CE1#	DO	1	NAND Flash Chip Enable 1
B15	PLLBUS_XOUT	AO	-	27MHz Crystal Oscillator Output
B16	BOOT_SEL	DI	0	Boot Selection High: Boot from NOR Flash Low: Boot from Internal ROM
B17	GPIO_12	DB	1	General Purpose I/O 12
	I2C0_SCL	DB		I2C Serial Clock Output
	PWM_0	DO		PWM_0 Output. (location 0)
B18	GPIO_6	DB	1	General Purpose I/O 6
	EJ_TCLK	DI		EJTAG Test Mode Clock (location 0)
	AI_SD	DI		I2S Serial Data Input for Audio L/R Input
B19	GPIO_2	DB	1	General Purpose I/O 2
	EJ_RST#	DI		EJTAG Reset (location 0)
	AIO_LRCK	DB		Audio-In Interface: I2S Word Select Clock Output/Input to/from ADC Audio-Out Interface: I2S Word Select Clock Output/Input to/from ADC
B20	UR0_TX	DO	-	UART0 Transmit Data Output
B21	TP1_CLK	DI	1	Secondary Transport Stream Input Clock
B22	TP1_SYNC	DI	1	Secondary Transport Stream Input SYNC
C1	GND	GND	-	Digital Ground
C2	DDR4_DQ19	DB	-	DDR4 Data 19
	DDR3_DQ17	DB		DDR3 Data 17
C3	DDR4_DQ17	DB	-	DDR4 Data 17
	DDR3_DQ19	DB		DDR3 Data 19
C4	DDR4_DQS3_t	DB	-	DDR3/DDR4 DQ[31:24] Data Strobe
C5	DDR4_DM2	DO	-	DDR3/DDR4 DQ[23:16] Data Mask
C6	GND	GND	-	Digital Ground
C7	GND	GND	-	Digital Ground
C8	GND	GND	-	Digital Ground
C9	EMMC_DATA_6	DB	1	eMMC Data 6
	NF_D7	DB		NAND Flash Data 7
C10	EMMC_DATA_7	DB	1	eMMC Data 7
	NF_D6	DB		NAND Flash Data 6
C11	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
C12	GND	GND	-	Digital Ground
C13	EMMC_CLK	DO	-	eMMC Clock Output
	NF_CLE	DO		NAND Flash Command Latch Enable
C14	SPI_CE_N	DO	1	Serial Flash Chip Select Output
	NF_CE0#	DO		NAND Flash Chip Enable 0
	I2C5_SDA	DB		I2C Serial Data Signal
C15	PLLBUS_XIN	AI	-	27MHz Crystal Oscillator Input
C16	WD_RSET	DI	1	Default Input. When a watchdog reset is triggered, output low to reset on-board PMICs. 0: Reset, 1: Active
C17	GND	GND	-	Digital Ground
C18	GPIO_5	DB	1	General Purpose I/O 5
	EJ_TMS	DI		EJTAG Test Mode Select (location 0)
	AO_SD	DB		I2S Serial Data Output for Downmixing Channels
C19	GPIO_47	DB	1/5V tolerance	General Purpose I/O 47
	FAN_IN	DI		Fan Speed Detect (Tachometer Input)
C20	TP0_DATA	DI	1	Primary Transport Stream Input Data
C21	TP0_CLK	DI	1	Primary Transport Stream Input Clock
C22	GND	GND	-	Digital Ground
D2	GND	GND	-	Digital Ground
D3	DDR4_DQ21	DB	-	DDR3/DDR4 Data 21
D4	DDR4_DQ27	DB	-	DDR4 Data 27
	DDR3_DQ24	DB		DDR3 Data 24
D5	DDR4_DQS2_t	DB	-	DDR3/DDR4 DQ[23:16] Data Strobe
D6	DDR4_DQS2_c	DB	-	DDR3/DDR4 DQ[23:16] Data Strobe
D8	DDR4_DQ22	DB	-	DDR4 Data 22
	DDR3_DQ20	DB		DDR3 Data 20
D9	DDR_VIO	PWR	-	DDR Power
D11	VDD_EMMC	PWR	-	NAND & eMMC Pin Power
D12	EMMC_DD_SB	DI	0	eMMC Data Strobe
D14	SPI_SCK	DO	-	Serial Flash Clock
	NF_WR#	DO	1	NAND Flash Write Enable
D15	IR_RX	DI	1	Infrared Input from IR Receiver; 3.3V Tolerant
D17	GPIO_13	DB	1	General Purpose I/O 13
	I2C0_SDA	DB		I2C Serial Data Signal
	PWM_1	DO		PWM_1 Output. (location 0)
D18	GPIO_4	DB	1	General Purpose I/O 4
	EJ_TDO	DO		EJTAG Test Data Output (location 0)
	AIO_CK	DO		Audio-In Interface: Main Clock Output to ADC as Master Mode Audio-Out Interface: Main Clock Output to DAC
D19	GPIO_50	DB	1	General Purpose I/O 50
	SPDIF	DO		IEC 60958 (SPDIF) Output
D20	TP0_VALID	DI	1	Primary Transport Stream Input Data Valid
D21	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
E2	DDR4_DQ4	DB	-	DDR4 Data 4
	DDR3_DQ2	DB		DDR3 Data 2
E3	DDR4_DQ2	DB	-	DDR4 Data 2
	DDR3_DQ6	DB		DDR3 Data 6
E4	DDR4_DQ23	DB	-	DDR3/DDR4 Data 23
E5	GND	GND	-	Digital Ground
E6	DDR4_DM3	DO	-	DDR3/DDR4 DQ[31:24] Data Mask
E7	GND	GND	-	Digital Ground
E8	DDR4_DQ30	DB	-	DDR4 Data 30
	DDR3_DQ25	DB		DDR3 Data 25
E9	DDR_VIO	PWR	-	DDR Power
E10	DDR_VIO	PWR	-	DDR Power
E11	EMMC_DATA_1	DB	1	eMMC Data 1
	NF_D4	DB		NAND Flash Data 4
E12	EMMC_RST_N	DO	1	eMMC Reset Signal
	NF_RDY	DI		NAND Flash Ready
E13	GND	GND	-	Digital Ground
E14	SPI_SI	DB	-	Serial Flash Data Input (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)
	NF_ALE	DO		NAND Flash Address Latch Enable
	I2C5_SCL	DB		I2C Serial Clock Output
E15	TESTMODE	DI	0	Select Test Mode
E16	GPIO_0	DB	1/5V tolerance	General Purpose I/O 0
E17	GPIO_3	DB		General Purpose I/O 3
	EJ_TDI	DI		EJTAG Test Data Input (location 0)
E17	AIO_BCK	DB		Audio-In Interface: I2S Bit Clock Output/Input to/from ADC Audio-Out Interface: I2S Bit Clock Output/Input to/from DAC
E18	GND	GND	-	Digital Ground
E20	TP0_SYNC	DI	1	Primary Transport Stream Input SYNC
E21	ADAC_DACREF_33	PWR	-	AD/DA Reference Power
F1	DDR4_DQ12	DB	-	DDR4 Data 12
	DDR3_DQ11	DB		DDR3 Data 11
F2	DDR4_DQ0	DB	-	DDR3/DDR4 Data 0
F3	GND	GND	-	Digital Ground
F4	DDR4_DQ6	DB	-	DDR4 Data 6
	DDR3_DQ4	DB		DDR3 Data 4
F5	DDR4_DQ14	DB	-	DDR4 Data 14
	DDR3_DQ9	DB		DDR3 Data 9
F6	DDR_VIO	PWR	-	DDR Power
F7	DDR_VIO	PWR	-	DDR Power
F8	DDR_VIO	PWR	-	DDR Power
F9	DDR_VIO	PWR	-	DDR Power
F10	DDR_VIO	PWR	-	DDR Power

Pin No.	Pin Name	I/O	Default Value	Description
F11	3.3V_SPI	PWR	-	SPI Power 3.3V
F12	3.3V_PLL	PWR	-	PLL Power 3.3V
F16	3.3V_TGPIO	PWR	-	Digital IO Power 3.3V
F20	GND_ADAC	GND	-	Audio DAC Ground
F21	ADAC_AOR	AO	-	Audio DAC Output Right Channel
F22	ADAC_AOL	AO	-	Audio DAC Output Left Channel
G1	DDR4_DQ10	DB	-	DDR4 Data 10
	DDR3_DQ13	DB		DDR3 Data 13
G2	DDR4_DQ8	DB	-	DDR4 Data 8
	DDR3_DQ15	DB		DDR3 Data 15
G3	GND	GND	-	Digital Ground
G5	GND	GND	-	Digital Ground
G6	DDR_VIO	PWR	-	DDR Power
G7	DDR_VIO	PWR	-	DDR Power
G8	DDR_VIO	PWR	-	DDR Power
G9	DDR_VIO	PWR	-	DDR Power
G10	DDR_VIO	PWR	-	DDR Power
G11	GND	GND	-	Digital Ground
G12	1.8V_PLL	PWR	-	PLL Power 1.8V
G13	GND_PLL	GND	-	PLL Ground
G14	1.0V_PLL	PWR	-	PLL Power 1.0V
G15	1.0V_CORE	PWR	-	Core Power
G16	1.0V_CORE	PWR	-	Core Power
G17	1.0V_CORE	PWR	-	Core Power
G20	GND	GND	-	Digital Ground
G21	CVBS	AO	-	Composite Output
G22	ADAC_VREF	AO	-	Audio Reference VCM
H2	DDR4_DM1	DO	-	DDR3/DDR4 DQ[15:8] Data Mask
H3	GND	GND	-	Digital Ground
H4	DDR4_DQS0_t	DB	-	DDR3/DDR4 DQ[7:0] Data Strobe
H5	DDR4_DQS0_c	DB	-	DDR3/DDR4 DQ[7:0] Data Strobe
H6	DDR_VIO	PWR	-	DDR Power
H7	DDR_VIO	PWR	-	DDR Power
H8	GND	GND	-	Digital Ground
H9	GND	GND	-	Digital Ground
H10	GND	GND	-	Digital Ground
H11	GND	GND	-	Digital Ground
H13	GND	GND	-	Digital Ground
H14	1.0V_CORE	PWR	-	Core Power
H15	1.0V_CORE	PWR	-	Core Power
H16	1.0V_CORE	PWR	-	Core Power
H17	1.0V_CORE	PWR	-	Core Power
H20	GND	GND	-	Digital Ground
H21	TMDS_OP_C	AO	-	HDMI Output Data Pair 2+

Pin No.	Pin Name	I/O	Default Value	Description
J2	GND	GND	-	Digital Ground
J3	DDR4_DM0	DO	-	DDR3/DDR4 DQ[7:0] Data Mask
J4	DDR4_DQS1_t	DB	-	DDR3/DDR4 DQ[15:8] Data Strobe
J5	DDR4_DQS1_c	DB	-	DDR3/DDR4 DQ[15:8] Data Strobe
J6	DDR_VIO	PWR	-	DDR Power
J7	DDR_VIO	PWR	-	DDR Power
J8	GND	GND	-	Digital Ground
J9	GND	GND	-	Digital Ground
J10	GND	GND	-	Digital Ground
J11	GND	GND	-	Digital Ground
J13	GND	GND	-	Digital Ground
J14	1.0V_CORE	PWR	-	Core Power
J15	1.0V_CORE	PWR	-	Core Power
J16	1.0V_CORE	PWR	-	Core Power
J17	1.0V_CORE	PWR	-	Core Power
J18	1.0V_CORE	PWR	-	Core Power
J19	3.3V_ADAC	PWR	-	Audio DAC Power 3.3V
J20	TMDS_ONC	AO	-	HDMI Output Data Pair 2-
J21	GND	GND	-	Digital Ground
K1	GND	GND	-	Digital Ground
K2	DDR4_DQ13	DB	-	DDR4 Data 13
	DDR3_DQ14	DB		DDR3 Data 14
K3	DDR4_DQ9	DB	-	DDR4 Data 9
	DDR3_DQ12	DB		DDR3 Data 12
K5	GND	GND	-	Digital Ground
K6	DDR4_ZQ	PWR	-	Reference Pin for ZQ Calibration
K7	DDR_VIO	PWR	-	DDR Power
K8	GND	GND	-	Digital Ground
K9	GND	GND	-	Digital Ground
K10	GND	GND	-	Digital Ground
K11	GND	GND	-	Digital Ground
K12	GND	GND	-	Digital Ground
K14	1.0V_CORE	PWR	-	Core Power
K15	1.0V_CORE	PWR	-	Core Power
K16	1.0V_CORE	PWR	-	Core Power
K17	1.0V_CORE	PWR	-	Core Power
K18	1.0V_CORE	PWR	-	Core Power
K19	3.3V_VDAC	PWR	-	Video DAC Power 3.3V
K20	TMDS_OPB	AO	-	HDMI Output Data Pair 1+
K21	TMDS_ONB	AO	-	HDMI Output Data Pair 1+
K22	GND	GND	-	Digital Ground
L1	DDR4_DQ1	DB	-	DDR4 Data 1
	DDR3_DQ3	DB		DDR3 Data 3

Pin No.	Pin Name	I/O	Default Value	Description
L2	DDR4_DQ15	DB	-	DDR4 Data 15
	DDR3_DQ10	DB		DDR3 Data 10
L3	GND	GND	-	Digital Ground
L4	DDR4_DQ7	DB	-	DDR3/DDR4 Data 7
L5	DDR4_DQ11	DB	-	DDR4 Data 11
	DDR3_DQ8	DB		DDR3 Data 8
L6	DDR4_ZQ_VREF	PWR	-	Reference Voltage for ZQ
L7	DDR_VIO	PWR	-	DDR Power
L8	GND	GND	-	Digital Ground
L9	GND	GND	-	Digital Ground
L10	GND	GND	-	Digital Ground
L11	GND	GND	-	Digital Ground
L12	GND	GND	-	Digital Ground
L13	GND	GND	-	Digital Ground
L15	1.0V_CORE	PWR	-	Core Power
L16	1.0V_CORE	PWR	-	Core Power
L17	1.0V_CORE	PWR	-	Core Power
L18	1.0V_TX	PWR	-	HDMI TX Power 1.0V
L19	3.3V_TX	PWR	-	HDMI TX Power 3.3V
L20	GND	GND	-	Digital Ground
L21	TMDS_OPA	AO	-	HDMI Output Data Pair 0+
L22	TMDS_ONA	AO	-	HDMI Output Data Pair 0-
M1	DDR4_DQ3	DB	-	DDR4 Data 3
	DDR3_DQ1	DB		DDR3 Data 1
M2	DDR4_DQ5	DB	-	DDR3/DDR4 Data 5
M3	GND	GND	-	Digital Ground
M4	DDR4_CK1_t	DO	-	DDR3/DDR4 Clock Positive Output 1
M5	DDR4_CK1_c	DO	-	DDR3/DDR4 Clock Negative Output 1
M6	DDR_VIO	PWR	-	DDR Power
M7	DDR_VIO	PWR	-	DDR Power
M8	GND	GND	-	Digital Ground
M9	GND	GND	-	Digital Ground
M10	GND	GND	-	Digital Ground
M11	GND	GND	-	Digital Ground
M12	GND	GND	-	Digital Ground
M13	GND	GND	-	Digital Ground
M14	GND	GND	-	Digital Ground
M18	1.8V_TX	PWR	-	HDMI TX 1.8V
M19	3.3V_MBIAS	PWR	-	Bandgap Power 3.3V
M20	GND_MBIAS	GND	-	Bandgap Ground
M21	TMDS_CKN	AO	-	HDMI Output Clock Pair-
M22	TMDS_CKP	AO	-	HDMI Output Clock Pair+
N1	GND	GND	-	Digital Ground
N2	DDR4_CK0_t	DO	-	DDR3/DDR4 Clock Positive Output 0

Pin No.	Pin Name	I/O	Default Value	Description
N3	DDR4_CK0_c	DO	-	DDR3/DDR4 Clock Negative Output 0
N5	GND	GND	-	Digital Ground
N6	DDR_VIO	PWR	-	DDR Power
N7	DDR_VIO	PWR	-	DDR Power
N8	GND	GND	-	Digital Ground
N9	GND	GND	-	Digital Ground
N10	GND	GND	-	Digital Ground
N11	GND	GND	-	Digital Ground
N12	GND	GND	-	Digital Ground
N13	GND	GND	-	Digital Ground
N15	CPU_DVS	PWR	-	CPU DVFS Power
N16	CPU_DVS	PWR	-	CPU DVFS Power
N17	CPU_DVS	PWR	-	CPU DVFS Power
N18	CPU_DVS	PWR	-	CPU DVFS Power
N20	MBIAS_REXT_6K	PWR	-	Bandgap Voltage of Whole Chip. Connect to GND via a 6.19KΩ, ±1% Resistor
N21	VOCEC_TX	AB	-	HDMI TX Consumer Electronics Control
N22	GND	GND	-	Digital Ground
P2	GND	GND	-	Digital Ground
P3	DDR3_CKE1	DO	-	DDR3 Clock Enable Output 1
P4	DDR4_BG1	DO	-	DDR4 Bank Group 1
	DDR3_BA1	DO		DDR3 Bank Address 1
P5	DDR4_RAS#/A16	DO	-	DDR4 Row Address Select Output / Address 16
	DDR3_A10	DO		DDR3 Address 10
P6	DDR_VIO	PWR	-	DDR Power
P7	DDR_VIO	PWR	-	DDR Power
P8	GND	GND	-	Digital Ground
P9	GND	GND	-	Digital Ground
P10	GND	GND	-	Digital Ground
P11	GND	GND	-	Digital Ground
P12	GND	GND	-	Digital Ground
P14	CPU_DVS	PWR	-	CPU DVFS Power
P15	CPU_DVS	PWR	-	CPU DVFS Power
P16	CPU_DVS	PWR	-	CPU DVFS Power
P17	CPU_DVS	PWR	-	CPU DVFS Power
P18	CPU_DVS	PWR	-	CPU DVFS Power
P19	3.3V_HGPIO	PWR	-	Digital IO Power 3.3V
P20	GPIO_17	DB	1/5V tolerance	General Purpose I/O 17
	I2C1_SDA	DB		I2C Serial Data Signal
P21	GPIO_16	DB	1/5V tolerance	General Purpose I/O 16
	I2C1_SCL	DB		I2C Serial Clock Output
R2	DDR3_CKE0	DO	-	DDR3 Clock Enable Output 0
R3	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
R4	DDR4_CAS#/A15	DO	-	DDR4 Column Address Select Output / Address 15
	DDR3_A4	DO		DDR3 Address 4
R5	DDR4_BA1	DO	-	DDR4 Bank Address 1
	DDR3_A1	DO		DDR3 Address 1
R6	GND	GND	-	Digital Ground
R7	GND	GND	-	Digital Ground
R8	1.8V_DDR	PWR	-	DDR Power 1.8V
R12	1.8V_SD	PWR	-	SD Power 1.8V
R13	CPU_DVS	PWR	-	CPU DVFS Power
R14	CPU_DVS	PWR	-	CPU DVFS Power
R15	CPU_DVS	PWR	-	CPU DVFS Power
R16	CPU_DVS	PWR	-	CPU DVFS Power
R17	SCPU_MEM	PWR	-	L2 Cache DVFS Power
R19	GPIO_19	DB	1/5V tolerance	General Purpose I/O 19
	UR2_TX	DO		UART2 Transmit Data Output (location 0)
	GSPI_SCK	DO		Serial Interface Controller Clock (location 0)
	SC_CLK	DO		Smart Card Clock Signal
R20	GPIO_18	DB	1/5V tolerance	General Purpose I/O 18
	UR2_RX	DI		UART2 Receive Data Input (location 0)
	GSPI_MISO	DI		Serial Interface Controller Data Input (location 0)
	SC_RST#	DO		Smart Card Reset Signal
R21	HDMI_HPD	DI	1/5V tolerance	HDMI Hot Plug-In
	GPIO_7	DB		General Purpose I/O 7
T1	DDR4_CS1#	DO	-	DDR4 Chip Select Output 1
T2	DDR4_CS0#	DO	-	DDR4 Chip Select Output 0
T3	GND	GND	-	Digital Ground
T5	GND	GND	-	Digital Ground
T6	3.3V_DDR	PWR	-	DDR Power 3.3V
T7	GND_LSADC	GND	-	Digital Ground
T8	1.0V_DDRPLL	PWR	-	DDR Power 1.0V
T10	1.0V_USB	PWR	-	USB Power 1.0V
T13	1.0V_PCIE	PWR	-	PCIe Power 1.0V
T14	1.0V_ETN	PWR	-	ETN Power 1.0V
T15	CPU_DVS	PWR	-	CPU DVFS Power
T16	CPU_DVS	PWR	-	CPU DVFS Power
T18	GPIO_22	DB	1/5V tolerance	General Purpose I/O 22
	PWM_2	DO		PWM_2 Output (location 1)
T20	GPIO_21	DB	1/5V tolerance	General Purpose I/O 21
	PWM_1	DO		PWM_1 Output (location 1)

Pin No.	Pin Name	I/O	Default Value	Description
T21	GPIO_20	DB	1/5V tolerance	General Purpose I/O 20
	PWM_0	DO		PWM_0 Output (location 1)
	UR2_CTS#	DI		UART2 Clear to Send Input (location 0)
	GSPI_CS	DO		Serial Interface Controller Chip Select Output (location 0)
	SC_DATA	DB		Smart Card Input or Output for Serial Data
T22	GPIO_31	DB	1/5V tolerance	General Purpose I/O 31
	UR2_RTS#	DO	-	UART2 Request to Send Output (location 0)
	GSPI_MOSI	DO	-	Serial Interface Controller Data Output (location 0)
	SC_CD	DI	-	Smart Card Card Detect Signal
U1	DDR4_TEN	DO	-	DDR4 Connectivity Enable
U2	DDR4_ALERT	DO	-	DDR4 Alert
U3	GND	GND	-	Digital Ground
U4	DDR4_A3	DO	-	DDR4 Address 3
	DDR3_A15	DO		DDR3 Address 15
U5	DDR4_A1	DO	-	DDR4 Address 1
	DDR3_A12	DO		DDR3 Address 12
U6	GND	GND	-	Digital Ground
U7	3.3V_LSADC	PWR	-	LSADC Power 3.3V
U8	3.3V OTP PROBE	PWR	-	OTP Probe Power 3.3V
U9	3.3V_USB	PWR	-	USB Power 3.3V
U11	3.3V_SD_GPIO	PWR	-	SD/GPIO Power 3.3V
U15	3.3V_ETN	PWR	-	Ethernet Power 3.3V
U16	3.3V_SCPU	PWR	-	SCPU Power 3.3V
U17	SD_CAP	PWR	-	SD/MMC Pin Power, connect to an external capacitor
U18	GPIO_34	DB	1	General Purpose I/O 34
	SD_WP	DI		SD/MMC Write Protect
U19	GPIO_30	DB	1	General Purpose I/O 30
U20	GPIO_14	DB	1	General Purpose I/O 14
	ETN_LED0	DO		Ethernet LED0, 10M ACT/Link, programmable
	PWM_2	DO		PWM_2 Output. (location 0)
U21	GPIO_15	DB	1	General Purpose I/O 15
	ETN_LED1	DO		Ethernet LED1, 100M ACT/Link, programmable
	PWM_3	DO		PWM_3 Output. (location 0)
U22	GPIO_23	DB	1/5V tolerance	General Purpose I/O 23
	PWM_3	DO		PWM_3 Output. (location 1)
V2	DDR4_A5	DO	-	DDR4 Address 5
	DDR3_A6	DO		DDR3 Address 6
V3	DDR4_A7	DO	-	DDR4 Address 7
	DDR3_A8	DO		DDR Address 8
V4	DDR4_A12	DO	-	DDR4 Address 12
	DDR3_BA2	DO		DDR3 Bank Address 2
V5	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
V6	DDR4_BA0	DO	-	DDR4 Bank Address 0
	DDR3_WE#	DO		DDR3 Write Enable Output
V7	GND	GND	-	Digital Ground
V8	DDR4_BG0	DO	-	DDR4 Bank Group 0
	DDR3_CAS#	DO		DDR3 Column Address Select Output
V9	LSADC	AI	-	Low Speed ADC
V10	GPIO_49	DB	1	General Purpose I/O 49
V11	USB_HSDM_1	AB	-	USB2.0 D- Signal (USB2.0 HOST only)
V12	VDD_UR1	PWR	-	UR1_TX, UR1_RX, UR1_CTS#, UR1_RTS# Pin Power
V13	VDD_SDIO	PWR	-	SDIO Pin Power
V14	GPIO_27	DB	1	General Purpose I/O 27
	UR2_TX	DO		UART2 Transmit Data Output (location 1)
	GSPI_SCK	DO		Serial Interface Controller Clock (location 1)
V15	GPIO_41	DB	1	General Purpose I/O 41
	SDIO_CLK	DO	-	SDIO Clock Output (location 1)
V16	GND	GND	-	Digital Ground
V17	GPIO_45	DB	1	General Purpose I/O 45
	SDIO_D3	DB		SDIO Data3 (location 1)
V18	GND	GND	-	Digital Ground
V19	GPIO_35	DB	1	General Purpose I/O 35
	SD_CD	DI		SD/MMC Card Detect
V20	GPIO_36	DB	1	General Purpose I/O 36
	SD_D0	DB		SD/MMC Data0
	SDIO_D0	DB		SDIO Data0 (location 0)
	EJ_RST#	DI		EJTAG Reset (location 1)
V21	GPIO_37	DB	1	General Purpose I/O 37
	SD_D1	DB		SD/MMC Data1
	SDIO_D1	DB		SDIO Data1 (location 0)
	EJ_TDI	DI		EJTAG Test Data Input (location 1)
W2	GND	GND	-	Digital Ground
W3	DDR4_A13	DO	-	DDR4 Address 13
	DDR3_A11	DO		DDR3 Address 11
W4	DDR4_PAR	DO	-	DDR4 Command and Address Parity
W5	DDR4_ACT#	DO	-	DDR4 Activation Command
	DDR3_A0	DO		DDR3 Address 0
W6	DDR4_A6	DO	-	DDR4 Address 6
	DDR3_BA0	DO		DDR3 Bank Address 0
W8	DDR4_WE#/A14	DO	-	DDR4 Write Enable Output / Address14
	DDR3_RAS#	DO		DDR3 Row Address Select Output
W9	GPIO_52	DB	1	General Purpose I/O 52
W11	USB_HSDP_1	AB	-	USB2.0 D+ Signal (USB2.0 HOST only)

Pin No.	Pin Name	I/O	Default Value	Description
W12	GPIO_25	DB	1/5V tolerance	General Purpose I/O 25
	UR2 RTS#	DO		UART2 Request to Send Output (location 1)
	GSPI_MOSI	DO		Serial Interface Controller Data Output (location 1)
	CLKOUT_32K	DO		Output 32K clock to board for BT wake on module using, when BT at suspend mode. 32K clock for power saving
W14	GPIO_28	DB	1	General Purpose I/O 28
	UR2 CTS#	DI		UART2 Clear to Send Input (location 1)
	GSPI_CS	DO		Serial Interface Controller Chip Select Output (location 1)
W15	GPIO_46	DB	1	General Purpose I/O 46
	PCIE_CLKREQ	AO		PCIe Clock Request
	MDIO	DB		Input/Output of Management Data
W17	PCIE_REFCLK_P	AO	-	PCIe Differential Reference Clock
W18	PCIE_REFCLK_M	AO	-	PCIe Differential Reference Clock
W19	GPIO_39	DB	1	General Purpose I/O 39
	SD_D3	DB		SD/MMC Data3
	SDIO_D3	DB		SDIO Data3 (location 0)
	EJ_TCLK	DI		EJTAG Test Mode Clock (location 1)
W20	GPIO_33	DB	1	General Purpose I/O 33
	SD_CLK	DO	-	SD/MMC Clock Output
	SDIO_CLK	DO		SDIO Clock Output (location 0)
	EJ_TDO	DO	1	EJTAG Test Data Output (location 1)
W21	GND	GND	-	Digital Ground
Y1	GND	GND	-	Digital Ground
Y2	DDR4_A9	DO	-	DDR4 Address 9
	DDR3_A14	DO		DDR3 Address 14
Y3	DDR4_A10	DO	-	DDR4 Address 10
	DDR3_A2	DO		DDR3 Address 2
Y4	DDR4_A11	DO	-	DDR4 Address 11
	DDR3_A5	DO		DDR3 Address 5
Y5	DDR4_A8	DO	-	DDR4 Address 8
	DDR3_A3	DO		DDR3 Address 3
Y6	GND	GND	-	Digital Ground
Y7	GND	GND	-	Digital Ground
Y8	GND	GND	-	Digital Ground
Y9	GPIO_53	DB	1	General Purpose I/O 53
Y10	USB_HSDM_0	AB	-	USB2.0 D- Signal (USB2.0 HOST or DEVICE)
Y11	GND	GND	-	Digital Ground
Y12	GND	GND	-	Digital Ground
Y13	GPIO_9	DB	1	General Purpose I/O 9
	UR1_TX	DO		UART1 Transmit Data Output
Y14	GPIO_29	DB	1	General Purpose I/O 29
	MDC	DO		Management Data Clock
Y15	GND	GND	-	Digital Ground
Y16	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
Y17	GND	GND	-	Digital Ground
Y18	PCIE_HSON	AO	-	PCIe Differential Transmit Output
	SGMII_HSON	AO		SERDES differential output. 1.25GHz serial interface to transmit data to an external device that supports SGMII
Y19	PCIE_HSIP	AI	-	PCIe Differential Receive Input
	SGMII_HSIP	AI		SERDES differential input. 1.25GHz serial interface to receive data from an external device that supports SGMII
Y20	ETN_TXOP	AB	-	MDI mode: Transmit Output. MDIX mode: Receiver Input
Y21	GPIO_32	DB	1	General Purpose I/O 32
	SD_CMD	DB		SD/MMC Command Line
	SDIO_CMD	DB		SDIO Command Line (location 0)
	EJ_TMS	DI		EJTAG Test Mode Select (location 1)
Y22	GND	GND	-	Digital Ground
AA1	DDR4_A4	DO	-	DDR4 Address 4
	DDR3_A13	DO		DDR3 Address 13
AA2	GND	GND	-	Digital Ground
AA3	DDR4_A2	DO	-	DDR4 Address 2
	DDR3_A7	DO		DDR3 Address 7
AA4	GND	GND	-	Digital Ground
AA5	DDR3_CS0#	DO	-	DDR3 Chip Select Output 0
AA6	DDR3_CS1#	DO	-	DDR3 Chip Select Output 1
AA7	DDR4_CKE0	DO	-	DDR4 Clock Enable Output 0
AA8	DDR4_CKE1	DO	-	DDR4 Clock Enable Output 1
AA9	GPIO_48	DB	1	General Purpose I/O 48
AA10	USB_HSDP_0	AB	-	USB2.0 D+ Signal (USB2.0 HOST or DEVICE)
AA11	USB_HSDM_2	AB	-	USB2.0 D- Signal (USB2.0 HOST only)
AA12	GPIO_24	DB	1/5V tolerance	General Purpose I/O 24
	USB_CC2	AB		USB Type C Port Configuration Channel
AA13	GPIO_8	DB	1	General Purpose I/O 8
	UR1_RX	DI		UART1 Receive Data Input
AA14	GPIO_11	DB	1	General Purpose I/O 11
	UR1_RTS#	DO		UART1 Request to Send Output
AA15	GPIO_26	DB	1	General Purpose I/O 26
	UR2_RX	DI		UART2 Receive Data Input (location 1)
	GSPI_MISO	DI		Serial Interface Controller Data Input (location 1)
AA16	GPIO_40	DB	1	General Purpose I/O 40
	SDIO_CMD	DB		SDIO Command Line (location 1)
AA17	GPIO_44	DB	1	General Purpose I/O 44
	SDIO_D2	DB		SDIO Data2 (location 1)
AA18	PCIE_HSOP	AO	-	PCIe Differential Transmit Output
	SGMII_HSOP	AO		SERDES differential output. 1.25GHz serial interface to transmit data to an external device that supports SGMII
AA19	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
AA20	PCIE_HSIN	AI	-	PCIe Differential Receive Input
	SGMII_HSIN	AI		SERDES differential input. 1.25GHz serial interface to receive data from an external device that supports SGMII
AA21	ETN_RXIP	AB	-	MDI mode: Receiver Input. MDIX mode: Transmit Output
AA22	GPIO_38	DB	1	General Purpose I/O 38
	SD_D2	DB		SD/MMC Data2
	SDIO_D2	DB		SDIO Data2 (location 0)
AB1	DDR4_A0	DO	-	DDR4 Address 0
	DDR3_A9	DO		DDR3 Address 9
AB2	DDR4_RST#	DO	-	DDR3/DDR4 Reset
AB3	GND	GND	-	Digital Ground
AB6	DDR4_ODT0	DO	-	DDR3/DDR4 On-Die Termination 0
AB7	DDR4_ODT1	DO	-	DDR3/DDR4 On-Die Termination 1
AB10	GND	GND	-	Digital Ground
AB11	USB_HSDP_2	AB	-	USB2.0 D+ Signal (USB2.0 HOST only)
AB12	GPIO_51	DB	1/5V tolerance	General Purpose I/O 51
	USB_CC1	AB		USB Type C Port Configuration Channel
AB13	GPIO_10	DB	1	General Purpose I/O 51
	UR1_CTS#	DI		UART1 Clear to Send Input
AB16	GPIO_42	DB	1	General Purpose I/O 42
	SDIO_D0	DB		SDIO Data0 (location 1)
AB17	GPIO_43	DB	1	General Purpose I/O 43
	SDIO_D1	DB		SDIO Data1 (location 1)
AB20	GND	GND	-	Digital Ground
AB21	ETN_TXON	AB	-	MDI mode: Transmit Output. MDIX mode: Receiver Input
AB22	ETN_RXIN	AB	-	MDI mode: Receiver Input. MDIX mode: Transmit Output

## 7. System Global Resources

### 7.1. Absolute Maximum Ratings

**WARNING:** Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 2. Power Supply Specification**

Symbol	Min.	Max.	Unit	Description
CPU_DVS	-0.4	1.25	V	Voltage on power pin for CPU
1V	-0.4	1.25	V	Supply voltage on power pin for Analog or Digital Logic, Isolated Block Logic, GPU
DDR_VIO	-0.4	1.975	V	Voltage on power pin for DDR controller
1.8V	-0.4	1.98	V	Supply voltage on power pin for Analog or Digital Logic
3.3V	-0.4	3.63	V	Voltage on power pin for I/O Pad, Analog or Digital Logic
DC input	-0.4	Corresponding Supply Voltage +0.4	V	Input voltage on any I/O pin
DC output	-0.4	Corresponding Supply Voltage +0.4	V	Output voltage on any I/O pin
Tstg	-55	150	°C	Storage temperature

### 7.2. Recommended Operating Conditions

It is important to provide adequate power and ground for high-speed digital and sensitive analog design. To achieve the best quality, the power and ground pins are separated into several groups. The DC voltage listed in Table 3 does not include ripple.

**Table 3. Recommended Operating Conditions**

Symbol	Min.	Typ.	Max.	Unit	Description
CPU_DVS	0.78	1.0	1.12	V	Voltage on power pin for CPU
1V	0.95	1.0	1.05	V	Supply voltage on power pin for Analog or Digital Logic, Isolated Block Logic, GPU
DDR_VIO	For DDR3	1.425	1.5	V	Voltage on power pin for DDR controller
	For DDR4	1.14	1.2		
1.8V	1.71	1.8	1.89	V	Supply voltage on power pin for Analog or Digital Logic
3.3V	3.135	3.3	3.465	V	Voltage on power pin for I/O Pad, Analog or Digital Logic
Tj	0	-	125	°C	Junction Temperature

**Table 4. DC Characteristics**

Symbol	Min.	Typ.	Max.	Unit	Description
V <sub>OH</sub>	For DDR_VIO	-	0.9*DDR_VIO	V	Minimum high level output voltage
	For 1.8V I/O	1.45**	-		
	For 3.3V I/O	2.6**	-		
V <sub>OL</sub>	For DDR_VIO	-	0.1*DDR_VIO	V	Maximum low level output voltage
	For 1.8V I/O	-	-		
	For 3.3V I/O	-	-		
V <sub>IH</sub>	For DDR_VIO	0.5*DDR_VIO +0.100	-	V	Maximum high level input voltage
	For 1.8V I/O	1.27	-		
	For 3.3V I/O	2.2	-		
V <sub>IL</sub>	For DDR_VIO	0	-	V	Maximum low level input voltage
	For 1.8V I/O	-	-		
	For 3.3V I/O	-	-		

\*Test Condition:  $I_{OL}=2mA$

\*\*Test Condition:  $I_{OH}=-2mA$

### 7.3. Power Management

The RTD1395 provides a Sleep Mode that shuts down all PLLs and logic to save power during idle state. Sleep Mode is entered via a software instruction sequence, and exited by a hardware reset. External wake-up events may be selected to automatically generate a wake-up reset.

For lower power consumption in Sleep Mode, all parts of the RTD1395 can be powered off except for the isolation block. The wake-up function still works in this Sleep Mode.

Some RTD1395 modules can be individually powered down by gating off their clock tree. Those modules can be powered on without resetting the whole chip.

### 7.4. Power Ripple

**Table 5. Power Ripple**

Symbol	Max.	Unit	Description
CPU_DVS	70	mV <sub>p-p</sub>	Voltage on power pin for CPU
1V	60	mV <sub>p-p</sub>	Supply voltage on power pin for Analog or Digital Logic, Isolated Block Logic, GPU
DDR_VIO	60	mV <sub>p-p</sub>	Voltage on power pin for DDR controller
1.8V	40	mV <sub>p-p</sub>	Supply voltage on power pin for Analog or Digital Logic
3.3V	50	mV <sub>p-p</sub>	Voltage on power pin for I/O Pad, Analog or Digital Logic

## 7.5. Crystal Requirements

**Table 6. Crystal Requirements for the RTD1395**

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F <sub>ref</sub>	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	27	-	MHz
F <sub>ref</sub> Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T <sub>a</sub> =0°C~70°C	-30	-	30	ppm
F <sub>ref</sub> Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T <sub>a</sub> =25°C	-50	-	50	ppm
F <sub>ref</sub> Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	40	Ω
CL	Load Capacitance	10	-	20	pF
Jitter	Broadband Peak-to-Peak Jitter	-	-	200	ps
DL	Drive Level	-	-	-	mW

Note1: The CLK source can come from other places in the system, but it must accord with the parameters above.

Note2: The ESR maximum value of 40ohm is based on shunt capacitance (Co) less than 4pF.

Note3: The accuracy of the crystal resonance frequency can be achieved by matching the load capacitance correctly to the designed-in circuit. The latest schematic circuit recommends two external capacitors of 33pF connected between the crystal and ground. To match this use the load capacitance specified by the crystal manufacturer of 10~20pF.

## 7.6. Reset, Clock, and PLL

**Table 7. System Global Resources External Pin Description**

Pin Name	Type	Description
RESET_N	DI	Chip Reset, Schmitt Trigger Input
PLLBUS_XIN	AI	27MHz Crystal Oscillator Input
PLLBUS_XOUT	AO	27MHz Crystal Oscillator Output
MBIAS_REXT_6K	PWR	Bandgap Voltage of Whole Chip. Connect to GND via a 6.19KΩ, ±1% Resistor

The external RESET\_N signal is a low-active, Schmitt trigger input. To take effect, it must be held low for at least 500ns. An external crystal (27MHz) is required for normal function, and the embedded PLL circuit will generate all necessary clock signals for various modules. The crystal accuracy should be under 30ppm to ensure the best quality.

## 7.7. Thermal Considerations

To maintain a stable operating condition, the system designer should stay within maximum temperature limits.

**Table 8. Thermal Parameters for the RTD1395**

Thermal Resistance	Value	Comment
Theta JA	23.35 (°C/W)	References: EIA/JESD51-2, EIA/JESD51-9
Theta JC	6.13 (°C/W)	
Theta JB	12.80 (°C/W)	

## 7.8. Power-On Sequence

Generally, the power-on sequence should be as follows:

- Apply CPU\_DVS, 1V simultaneously
- Apply DDR\_VIO, 3.3V, 1.8V in sequence
- Wait for power supplies to stabilize
- Reset operation completes
- System boots up

The RTD1395 integrates a Power-On-Reset (POR) circuit to ensure the chip powers up in a default state. It monitors the status of 3.3V and CPU\_DVS. The POR circuit reset will release after 220 crystal clock cycles when both powers (3.3V & 1.8V) are stable. Figure 4 graphically shows the Power-On sequence timing. The detailed duration is listed in Table 9.

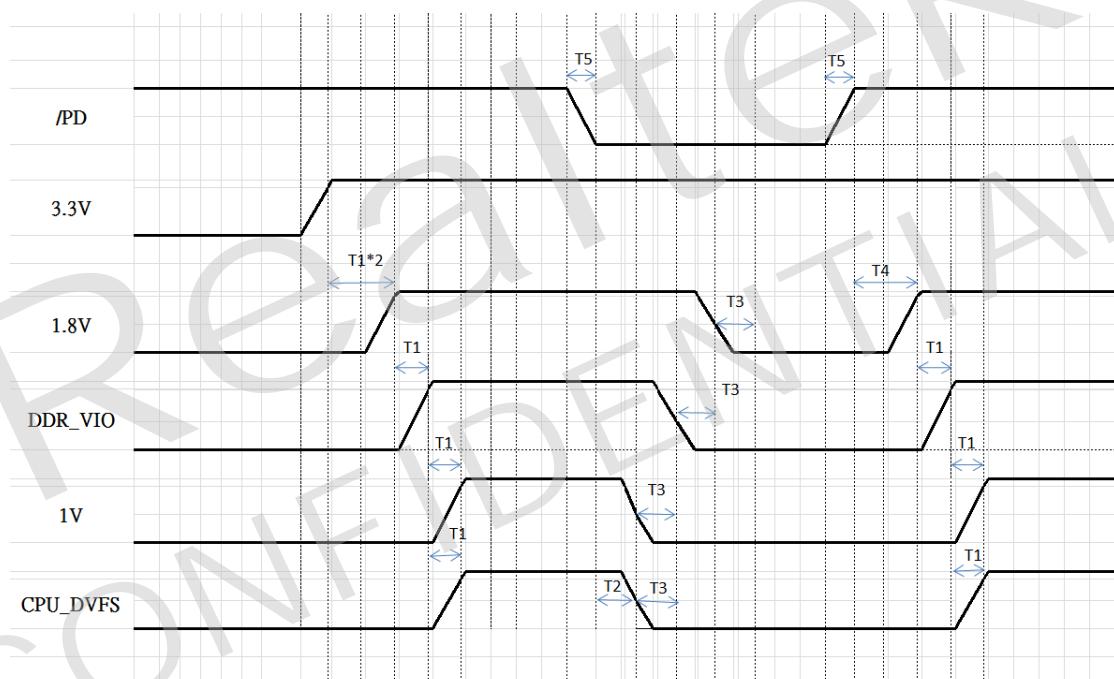


Figure 4. Power-On Sequence Timing Diagram

Table 9. Power-On Sequence Duration

Symbol	Description	Min	Max	Unit
T1	90% voltage delay between rails	1	10	ms
T2	50% voltage delay after PD# low	1	10	ms
T3	50% voltage delay between rails	1	10	ms
T4	90% voltage delay after PD# high	8	20	ms
T5	PD# rise and fall time	0	1	ms

**Table 10. Power-On Reset Trigger Level**

Power Rail	Power-On Reset Trigger Level (V)
CPU_DVS	0.57
1V	0.57
DDR_VIO	0.57
1.8V	1.17
3.3V	2.2

*Note: The IC will enter power on state if the power rails indicate above values.*

## 8. DDR Controller Unit

The RTD1395 DDR3/DDR4 Controller Unit (DCU) provides memory control signals required for external DDR3/DDR4 SDRAM access. With a 32-bit-wide SDRAM, the DCU can access up to 4GB.

### 8.1. Features

- Supports up to 4GB
- Supports Spread Spectrum Clocking (SSC)
- Supports Scrambling
- 1.35V/1.5V compatible DDR3L/DDR3 I/O
- 1.2V compatible DDR4 I/O

### 8.2. DCU Block External Pin Description

Table 11. DCU External Pin Description

Pin Name	Type	Description
DDR3_CK0 / DDR4_CK0_t	DO	DDR3/DDR4 Clock Positive Output 0
DDR3_CK0#/ DDR4_CK0_c	DO	DDR3/DDR4 Clock Negative Output 0
DDR3_CK1 / DDR4_CK1_t	DO	DDR3/DDR4 Clock Positive Output 1
DDR3_CK1#/ DDR4_CK1_c	DO	DDR3/DDR4 Clock Negative Output 1
DDR3_CKE0 / DDR4_CKE0	DO	DDR3/DDR4 Clock Enable Output 0
DDR3_CKE1 / DDR4_CKE1	DO	DDR3/DDR4 Clock Enable Output 1
DDR3_ODT0 / DDR4_ODT0	DO	DDR3/DDR4 On-Die Termination 0
DDR3_ODT1 / DDR4_ODT1	DO	DDR3/DDR4 On-Die Termination 1
DDR3_CS0#/ DDR4_CS0#	DO	DDR3/DDR4 Chip Select Output 0
DDR3_CS1#/ DDR4_CS1#	DO	DDR3/DDR4 Chip Select Output 1
DDR3_RAS#/ DDR4_RAS#	DO	DDR3/DDR4 Row Address Select Output
DDR3_CAS#/ DDR4_CAS#	DO	DDR3/DDR4 Column Address Select Output
DDR3_WE#/ DDR4_WE#	DO	DDR3/DDR4 Write Enable Output
DDR3_RST#/ DDR4_RST#	DO	DDR3/DDR4 Reset
DDR3_DQS0 / DDR4_DQS0_t	DO	DDR3/DDR4 DQ[7:0] Data Strobe
DDR3_DQS0#/ DDR4_DQS0_c	DB	DDR3/DDR4 DQ[7:0] Data Strobe
DDR3_DQS1 / DDR4_DQS1_t	DB	DDR3/DDR4 DQ[15:8] Data Strobe
DDR3_DQS1#/ DDR4_DQS1_c	DB	DDR3/DDR4 DQ[15:8] Data Strobe
DDR3_DQS2 / DDR4_DQS2_t	DB	DDR3/DDR4 DQ[23:16] Data Strobe
DDR3_DQS2#/ DDR4_DQS2_c	DB	DDR3/DDR4 DQ[23:16] Data Strobe
DDR3_DQS3 / DDR4_DQS3_t	DB	DDR3/DDR4 DQ[31:24] Data Strobe
DDR3_DQS3#/ DDR4_DQS3_c	DB	DDR3/DDR4 DQ[31:24] Data Strobe
DDR3_DM0 / DDR4_DM0	DO	DDR3/4 DQ[7:0] Data Mask
DDR3_DM1 / DDR4_DM1	DO	DDR3/4 DQ[15:8] Data Mask
DDR3_DM2 / DDR4_DM2	DO	DDR3/4 DQ[23:16] Data Mask

Pin Name	Type	Description
DDR3_DM3 / DDR4_DM3	DO	DDR3/4 DQ[31:24] Data Mask
DDR3_A[15:0]	DO	DDR3 Address[15:0]
DDR4_A[13:0]	DO	DDR4 Address[13:0]
DDR3_BA[2:0]	DO	DDR3 Bank Address[2:0]
DDR4_BA[1:0]	DO	DDR4 Bank Address[1:0]
DDR4_BG[1:0]	DO	DDR4 Bank Group[1:0]
DDR3_DQ[31:0] / DDR4_DQ[31:0]	DB	DDR3/4 Data[31:0]
DDR4_ACT#	DO	DDR4 Activation Command
DDR4_PAR	DO	DDR4 Command and Address Parity
DDR4_ALERT	DB	DDR4 Alert
DDR4_TEN	DO	DDR4 Connectivity Enable
DDR3_ZQ / DDR4_ZQ	PWR	Reference Pin for ZQ Calibration
DDR3_ZQ_VREF / DDR4_ZQ_VREF	PWR	Reference Voltage for ZQ

### 8.3. DCU Block Pin Mux Table

Table 12. DCU Block External Pin Mux Table

Ball Number	DDR3	DDR4
N2	CK0	CK0_t
N3	CK0#	CK0_c
M4	CK1	CK1_t
M5	CK1#	CK1_c
AA7	-	CKE0
AA8	-	CKE1
AB6	ODT0	ODT0
AB7	ODT1	ODT1
T2	-	CS0#
T1	-	CS1#
P5	A10	RAS#/A16
R4	A4	CAS#/A15
W8	RAS#	WE#/A14
AB2	RST#	RST#
H4	DQS0	DQS0_t
H5	DQS0#	DQS0_c
J4	DQS1	DQS1_t
J5	DQS1#	DQS1_c
D5	DQS2	DQS2_t
D6	DQS2#	DQS2_c
C4	DQS3	DQS3_t
B3	DQS3#	DQS3_c
J3	DM0	DM0
H2	DM1	DM1
C5	DM2	DM2

Ball Number	DDR3	DDR4
E6	DM3	DM3
AB1	A9	A0
U5	A12	A1
AA3	A7	A2
U4	A15	A3
AA1	A13	A4
V2	A6	A5
W6	BA0	A6
V3	A8	A7
Y5	A3	A8
Y2	A14	A9
Y3	A2	A10
Y4	A5	A11
V4	BA2	A12
W3	A11	A13
V6	WE#	BA0
R5	A1	BA1
V8	CAS#	BG0
P4	BA1	BG1
F2	DQ0	DQ0
L1	DQ3	DQ1
E3	DQ6	DQ2
M1	DQ1	DQ3
E2	DQ2	DQ4
M2	DQ5	DQ5
F4	DQ4	DQ6
L4	DQ7	DQ7
G2	DQ15	DQ8
K3	DQ12	DQ9
G1	DQ13	DQ10
L5	DQ8	DQ11
F1	DQ11	DQ12
K2	DQ14	DQ13
F5	DQ9	DQ14
L2	DQ10	DQ15
A7	DQ16	DQ16
C3	DQ19	DQ17
B8	DQ22	DQ18
C2	DQ17	DQ19
B7	DQ18	DQ20
D3	DQ21	DQ21
D8	DQ20	DQ22
E4	DQ23	DQ23
B5	DQ31	DQ24

Ball Number	DDR3	DDR4
A2	DQ28	DQ25
B6	DQ29	DQ26
D4	DQ24	DQ27
A6	DQ27	DQ28
A1	DQ30	DQ29
E8	DQ25	DQ30
B1	DQ26	DQ31
W5	A0	ACT#
W4	-	PAR
U2	-	ALERT
U1	-	TEN
K6	ZQ	ZQ
L6	ZQ_VREF	ZQ_VREF
AA5	CS0#	-
AA6	CS1#	-
R2	CKE0	-
P3	CKE1	-

## 9. Flash Controller

The flash controller supports Serial Peripheral Interface NOR flash memory and 8-bit NAND type flash memory. Each type could be configured as boot device.

### 9.1. Features

- Serial NOR Flash
  - Supports up to 32MB
  - Supports dual I/O read
  - Complies with MXIC protocol
- NAND Flash
  - Built-in SRAM buffer to improve performance
  - Built-in 6/12-bit ECC mechanism to enhance data reliability
  - Supports up to 2 flash chips with interleave accessing

### 9.2. Serial Flash Block External Pin Description

Table 13. Serial Flash Block External Pin Description

Pin Name	Type	Description
SPI_CE_N	DO	Serial Flash Chip Select Output
SPI_SCK	DO	Serial Flash Clock
SPI_SI/SIO0	DB	Serial Flash Data Input (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)
SPI_SO/SIO1	DB	Serial Flash Data Output (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)

### 9.3. NAND Flash Block External Pin Description

Table 14. NAND Flash Block External Pin Description

Pin Name	Type	Description
NF_CLE	DO	NAND Flash Command Latch Enable
NF_ALE	DO	NAND Flash Address Latch Enable
NF_RD#	DO	NAND Flash Read Enable
NF_WR#	DO	NAND Flash Write Enable
NF_RDY	DI	NAND Flash Ready
NF_CE[1:0]#	DO	NAND Flash Chip Enable[1:0]
NF_D[7:0]	DB	NAND Flash Data[7:0]

## 9.4. Boot Device Selection

**Table 15. Boot Device Selection**

ROM Selection	Boot Code	BOOT_SEL	GPIO_48	GPIO_49
ROM on SPI	eMMC	1	1	1
	USB Device	1	1	0
	NOR	1	0	1
	NAND	1	0	0
Internal ROM	eMMC	0	1	1
	USB Device	0	1	0
	NOR	0	0	1
	NAND	0	0	0

## 10. eMMC Controller

The eMMC controller supports eMMC. The data bit width is up to 8 bits. As pins are shared with NAND flash, the system can boot from eMMC, NAND, or serial NOR.

### 10.1. Features

- Supports eMMC 5.0
- Bus width: 1-bit, 4-bit, 8-bit
- Bus speed: Backwards compatibility with legacy MMC card, High speed SDR, High speed DDR, HS200, HS400
- Voltage: 1.8V

### 10.2. eMMC Block External Pin Description

Table 16. eMMC Block External Pin Description

Pin Name	Type	Description
EMMC_RST_N	DO	eMMC Reset Signal
EMMC_CLK	DO	eMMC Clock Output
EMMC_CMD	DB	eMMC Command Line
EMMC_DATA_[7:0]	DB	eMMC Data[7:0]
EMMC_DD_SB	DI	eMMC Data Strobe

### 10.3. NAND/eMMC Pin Mux Description

Table 17. NAND/eMMC Pin Mux Description

NAND Pin	eMMC Pin	NOR Pin
NF_RDY	EMMC_RST_N	-
-	EMMC_DD_SB	-
NF_CLE	EMMC_CLK	-
NF_RD#	EMMC_CMD	-
NF_D3	EMMC_DATA_0	-
NF_D4	EMMC_DATA_1	-
NF_D5	EMMC_DATA_2	-
NF_D1	EMMC_DATA_3	-
NF_D2	EMMC_DATA_4	-
NF_D0	EMMC_DATA_5	-
NF_D7	EMMC_DATA_6	-
NF_D6	EMMC_DATA_7	
NF_CE0#	-	SPI_CE_N
NF_WR#	-	SPI_SCK
NF_CE1#	-	SPI_SO
NF_ALE	-	SPI_SI

## 11. General SPI Interface

The low pin-count is the most important benefit of the Serial Peripheral Interface (SPI). The General SPI controller (G-SPI) is a full-duplex master serial interface and is used to control devices with an SPI interface, such as SPI flash or A/D converters. The GSPI also supports DMA mode to increase the transmitted and received data rate.

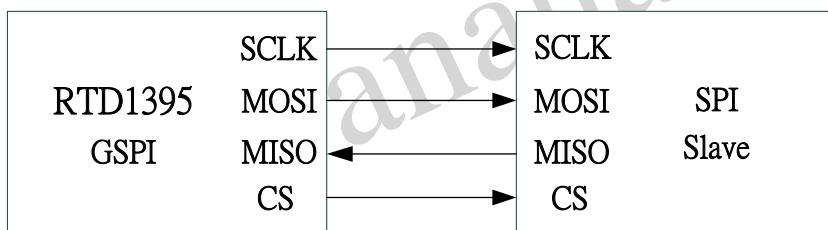
### 11.1. Features

- Serial-master Operation
- DMA Controller Interface
- Phase and polarity are changeable
- Maximum Clock Frequency: 32MHz
- Data Item Size: 4 to 32 bits
- TX and RX FIFO Depth: 10
- Serial Interface: Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire
- Flexible Timing: The sample time of the received serial data bit and the timing control of chip select pin are configurable

### 11.2. General SPI External Signal Description

**Table 18. General SPI External Signal Description**

Pin Name	Type	Description
GSPI_CS	DO	Serial Interface Controller Chip Select Output
GSPI_SCK	DO	Serial Interface Controller Clock
GSPI_MOSI	DO	Serial Interface Controller Data Output
GSPI_MISO	DI	Serial Interface Controller Data Input



**Figure 5. Basic SPI Bus Example**

## 12. High-Speed UART

The RTD1395 provides a high-speed UART for external Bluetooth transceiver connection (data rate is up to 3MHz). With hardware auto flow and DMA control, data transmission is unhindered.

### 12.1. Features

- 32 bytes for each TX & RX FIFO
- UART1 supports H5
- Programmable data rate up to 3MHz
- Hardware auto flow control CTS/RTS signal with polarity selectable
- Interrupt output signal occurs whenever one of the several prioritized interrupt types is enabled and active
- Receive error
- Receive data available
- Character timeout
- Transmitter holding register empty or below threshold interrupt

### 12.2. High-Speed UART Module External Pin Description

Table 19. High-Speed UART Module External Pin Description

Pin Name	Type	Description
UR1_RX	DI	UART1 Receive Data Input
UR1_TX	DO	UART1 Transmit Data Output
UR1_CTS#	DI	UART1 Clear to Send Input
UR1_RTS#	DO	UART1 Request to Send Output
UR2_RX	DI	UART2 Receive Data Input
UR2_TX	DO	UART2 Transmit Data Output
UR2_CTS#	DI	UART2 Clear to Send Input
UR2_RTS#	DO	UART2 Request to Send Output

## 13. Peripherals

### 13.1. General Purpose I/O

The RTD1395 provides multiple GPIO pins. Each general-purpose pin can be individually configured as an input or output pin via the direction configuration register. The Data output and input register (refer to the RTD1395 AN02 GPIO Pin Mux Description.pdf document) can be used to control signals (high or low) when the GPIO pin is configured as output, and show the status when the GPIO pin is configured as input.

When a GPIO pin is configured as input, it can also be configured as an interrupt generator (set in the interrupt enable and detection polarity register) (refer to the RTD1395 AN02 GPIO Pin Mux Description.pdf document).

### 13.2. Universal Asynchronous Receiver and Transmitter

The RTD1395 provides two 16C550 compatible UARTs (Universal Asynchronous Receiver and Transmitter).

#### 13.2.1. Features

- UART CH0 with 32-byte FIFO
- Programmable character properties, such as number of data bits per character (5~8), optional parity bit (with odd or even select) and number of stop bits (1, 1.5, or 2)
- Interrupt output signal occurs whenever one of the several prioritized interrupt types are enabled and active
- Receive Error
- Receive Data Available
- Character Timeout
- Transmitter Holding Register Empty at or below threshold

#### 13.2.2. UART Block External Pin Description

**Table 20. UART Block External Pin Description**

Pin Name	Type	Description
UR0_RX	DI	UART0 Receive Data Input
UR0_TX	DO	UART0 Transmit Data Output

### **13.3. I2C Serial Interface**

The RTD1395 can support three master/slave I2C-bus serial interfaces. A direct Serial Data Line (SDA) and Serial Clock Line (SCL) carry information between bus master and peripheral devices that are connected to the I2C-bus. The SDA and SCL lines are bi-directional.

#### **13.3.1. Features**

- Two-wire/Three-wire I2C serial interface
- Supports two speeds: Standard mode (100Kbps) and Fast mode (400Kbps)
- Clock synchronization
- Master or slave I2C operation
- Supports multi-Master operation (bus arbitration)
- 7-bit or 10-bit addressing
- 8-byte transmit and receive buffers
- 5V tolerance except I2C0\_SCL, I2C0\_SDA and I2C5\_SCL, I2C5\_SDA

#### **13.3.2. I2C Block External Pin Description**

**Table 21. I2C Block External Pin Description**

Pin Name	Type	Description
I2C0_SCL	DB	I2C Serial Clock Output
I2C0_SDA	DB	I2C Serial Data Signal
I2C1_SCL	DB	I2C Serial Clock Output
I2C1_SDA	DB	I2C Serial Data Signal
I2C5_SCL	DB	I2C Serial Clock Output
I2C5_SDA	DB	I2C Serial Data Signal

### **13.4. Infrared Receiver Controller**

The RTD1395 Infrared Receiver controller is designed for receiving commands from consumer remote controllers. It receives signals from an external IR receiver, translates signal zeros into data zeros, and accumulates data bits that conform to the register setting requirements and buffers.

#### **13.4.1. Features**

- IR channel with 2 layers of 32-bit FIFO
- Supports Bi-phase Modulation (e.g., PHILIPS RC-5, RC-6A)
- Supports Pulse Width Modulation (e.g., SONY SIRC)
- Supports Pulse Position Modulation (e.g., NEC, SHARP, PHILIPS RC-MM)
- Address and command length up to 32 bits
- Supports RAW mode for software decode remote signal

### 13.4.2. IR RX Block External Pin Description

**Table 22. IR RX Block External Pin Description**

Pin Name	Type	Description
IR_RX	DI	Infrared Input from IR Receiver; 3.3V Tolerant

## 13.5. Timer Control

The RTD1395 provides three 32-bit timers, a 90kHz timer, and a watchdog timer. The 32-bit timer and watchdog timer count at a fixed 27MHz rate. The 90kHz timer counts at 90kHz. The 32-bit timer can be configured to timer mode or counter mode. Counter mode means the timer only times-out once. Hardware will automatically disable timer interrupts after a time-out in counter mode. Software must enable the timer interrupt and set the target value for the next usage.

### 13.5.1. Features

- Three sets of 32-bit timer hardware
- One 90kHz timer
- One watchdog timer
- 32-bit timer hardware can be configured to timer or counter mode
- Supports timer/counter pulse

## 13.6. LSADC (Low Speed ADC)

The RTD1395 provides a one-channel Low-speed ADC for keypad detection.

- 6-bit ADC
- Frequency: < 1MHz

**Table 23. LSADC Interface**

Pin Name	Type	Description
LSADC	AI	Low Speed ADC

## 13.7. PWM

The RTD1395 provides four sets of PWM at two locations.

- Max/Min Frequency: 6.75MHz/1.6Hz

## 13.8. Smart Card Interface

The RTD1395 provides one ISO 7816 compliant Smart Card Interfaces (has a 40-bytes FIFO) that support embedded Conditional Access (CA) applications.

### 13.8.1. Features

- Supports T=0, T=1, and T=14 protocol.

### 13.8.2. Smart Card Controller External Pin Description

**Table 24. Smart Card Controller External Pin Description**

Pin Name	Type	Description
SC_DATA	DB	Smart Card Input or Output for Serial Data
SC_RST#	DO	Smart Card Reset Signal
SC_CLK	DO	Smart Card Clock Signal
SC_CD	DI	Smart Card Card Detect Signal

## 13.9. DC Fan Control

The DC FAN rotation detect controller is made up of three parts; a de-bounce circuit, a timer, and a counter. The timer counts at 90KHz. Software can setup the timer target value to store the counter value.

When the timer value equals the set target value, the counter value will be stored in registers and the counter cleared. The counter counts via a FAN tachometer pulse signal. The FAN tachometer pulse signal has de-bounce to filter noise. Figure 6 shows the interface of a 4-wire DC Fan.

### 13.9.1. Features

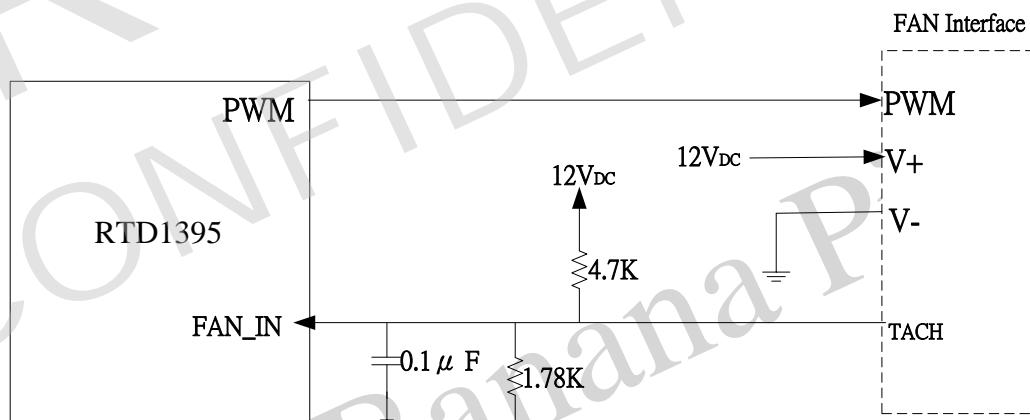
- Supports 3/4-wire fan with tachometer input
- 32-bit timer for precision control
- Configurable de-bounce time for noise filtering
- 5V tolerance for tachometer input

### 13.9.2. DC Fan Control External Pin Description

**Table 25. DC Fan Control External Pin Description**

Pin Name	Type	Description
FAN_IN	DI	Fan Speed Detect (Tachometer Input)

### 13.9.3. Typical 4-Wire Fan Interface



**Figure 6. Typical 4-Wire Fan Interface**

## 14. TV Encoder

The TV encoder encodes digital Y-Cb-Cr video data (4:2:2) to standard TV signal formats (NTSC or PAL) for CVBS. The supported TV formats are NTSC (M,J,4.43) or PAL (B, D, G, H, I, M, N, NC, 60).

The TV encoder supports multiple VBI encodings: Wide-Screen Signaling (WSS) or Teletext B for PAL, Copy Generation Management System (CGMS) for NTSC and Closed Caption (CC) for both NTSC and PAL.

The TV encoder includes a 10-bit voltage output DAC.

### 14.1. Features

- On-chip 10-bit Digital-to-Analog Converter
- Supports VBI encoding: Wide-Screen Signaling (WSS), Teletext B, Copy Generation Management System (CGMS) and Close Caption (CC)
- Video encoding supports multi-composite format that includes NTSC[M, J, 4.43] and PAL [B, D, G, H, I, M, N, NC, 60]

### 14.2. TV Encoder Analog Output Interface

Table 26. TV Encoder Analog Output Interface

Pin Name	Type	Description
CVBS	AO	Composite Output

## 15. HDMI Transmitter

The RTD1395 incorporates a High-Definition Multimedia Interface (HDMI) transmitter; a fully functional single-link transmitter with High-bandwidth Digital Content Protection (HDCP). It transmits studio-quality video/audio to any HDMI/DVI/HDCP-enabled digital receiver. This module is compliant with the HDMI2.0, DVI 1.0, and HDCP specifications. The RTD1395 HDMI transmitter can also carry control and status information.

### 15.1. Features

- HDMI2.0b, HDCP, and DVI 1.0 compliant transmitter

- ◆ Video Support

- Standard-Definition Video Format Timing:

- 720 (1440) x 480i @ 59.94/60Hz
  - 720 (1440) x 576i @ 50Hz
  - 720 x 480p @ 59.94/60Hz
  - 720 x 576p @ 50Hz

- High-Definition Video Format Timing:

- 1280 x 720p @ 59.94/60Hz
  - 1280 x 720p @ 50Hz
  - 1920 x 1080i @ 59.94/60Hz
  - 1920 x 1080i @ 50Hz
  - 1920 x 1080p @ 23.98/24Hz
  - 1920 x 1080p @ 59.94/60Hz
  - 1920 x 1080p @ 50Hz
  - 4K x 2K@23.98/24Hz
  - 4K x 2K@25Hz
  - 4K x 2K@29.97/30Hz
  - 4K x 2K@59.94/60Hz
  - 4K x 2K@50Hz

- Pixel Encoding:

- YCbCr 4:2:2
  - YCbCr 4:4:4
  - RGB 4:4:4

- Color Depth:

- Deep Color 24-bit
  - Deep Color 30-bit
  - Deep Color 36-bit

- 3D Video Format Structure

- Frame Packing
  - Top-and-Bottom
  - Side-by-Side (Half)

- ◆ Audio Support
  - Audio sample rate: 32~192k
  - Sample size: 16~24 bits
  - Up to 8-channel
  - Supports PCM, Dolby Digital, DTS digital audio transmission
  - IEC 60958 and IEC61937 compatible
  - Supports High-Bit-Rate Audio
- Master I2C interface for DDC Connection
- Supports Consumer Electronics Control (CEC)

## **15.2. HDMI Block External Pin Description**

**Table 27. HDMI Block External Pin Description**

Pin Name	I/O	Description
TMDS_CKN	AO	HDMI Output Clock Pair-
TMDS_CKP	AO	HDMI Output Clock Pair+
TMDS_ONA	AO	HDMI Output Data Pair 0-
TMDS_OPA	AO	HDMI Output Data Pair 0+
TMDS_ONB	AO	HDMI Output Data Pair 1-
TMDS_OPB	AO	HDMI Output Data Pair 1+
TMDS_ONC	AO	HDMI Output Data Pair 2-
TMDS_OPC	AO	HDMI Output Data Pair 2+
VOCEC_TX	AB	HDMI TX Consumer Electronics Control
HDMI_HPD	DI	HDMI Hot Plug-In

## 16. Audio-In Interface

The audio-in interface transfers audio PCM data. A 2-channel default I2S interface is supported. For Karaoke application, HW has an I2S input loopback function. The input data of I2S input could be mixed into PCM output data. The data will be modulated and mixed into the PCM output L or R channel. Only the 2ch I2S input would be looped back. The loopback L channel can be added to both output L and R channels, as can the loopback R channel.

### 16.1. Features

- Digital Interface
  - ◆ I2S
    - Sample Rate: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 128k, 176.4k, and 192kHz
    - Supports Master and Slave modes
    - PCM bit number: 16, 18, 20, 24, and 32-bit
    - Mute function for left or right channel
    - Supports Karaoke application with an I2S input loopback function.

## 16.2. Audio External Signal Descriptions

AIO\_CK and AIO\_BCK are the reference clock signals related to the input sampling rate.

AIO\_CK is output as slave mode, so an external crystal is not needed for ADC.

AIO\_LRCK is used as the Word Select line to identify the signal source.

Figure 7 and Figure 8 show the I2S audio-in configuration.

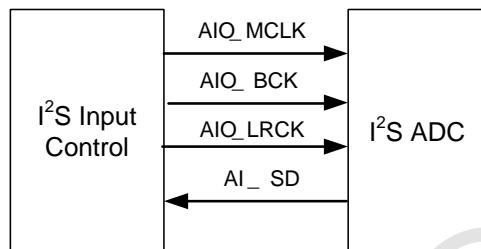


Figure 7. I2S Audio-In Master Mode Interface Configuration

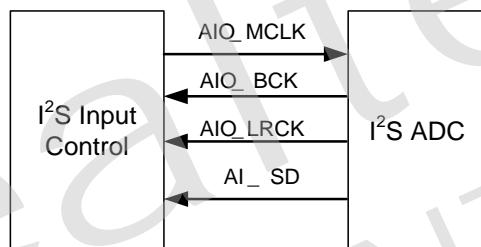


Figure 8. I2S Audio-In Slave Mode Interface Configuration

Table 28. Audio-In Block External Pin Description

Pin Name	Type	Description
AIO_CK	DO	Main Clock Output to ADC as Master Mode
AIO_BCK	DB	I2S Bit Clock Output/Input to/from ADC
AIO_LRCK	DB	I2S Word Select Clock Output/Input to/from ADC
AI_SD	DI	I2S Serial Data Input for Audio L/R Input

## 17. Audio-Out Interface

The audio-out interface transfers audio PCM data or non-PCM bit-stream data. Two digital audio IO interfaces, I2S and SPDIF, are supported. Three I2S output protocols are supported: Default I2S, left justified, and right justified. A 2-channel audio DAC (includes a 1Vrms line-level driver) is embedded in this chip. For HDMI output, the RTD1395's HDMI interface can send the PCM data from audio-out to the HDMI TX module.

### 17.1. Features

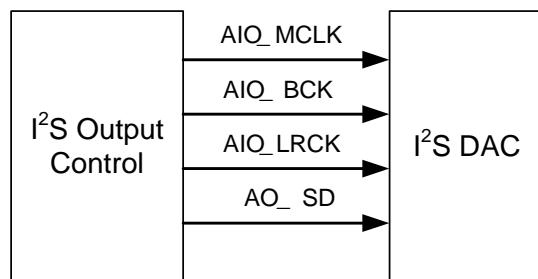
- Digital Interface
  - ◆ I2S
    - Three protocol types: Default I2S, left justified, and right justified
    - Sample rate: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 128k, 176.4k, and 192kHz
    - Supports Master and Slave modes
    - PCM bit number: 16, 18, 20, 24 and 32-bit
    - Variable WS period
    - Mute function for left or right channel
  - ◆ SPDIF
    - Designed in accordance with IEC 60958 (both PCM and non-PCM are supported)
    - Sample rate: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 128k, 176.4k, and 192kHz
    - PCM bit number: 16, 18, 20, and 24 bit
    - Independent mute control for left and right channels
- Analog Interface
  - ◆ Internal Audio DAC
    - 1Vrms line-level driver
    - PCM bit number: 16, 18, 20, and 24 bit
    - Pop-noise-free design on power on/off
    - Independent DAC filter gain for left and right channels
    - Independent mute control for left and right channels

## 17.2. Audio External Signal Descriptions

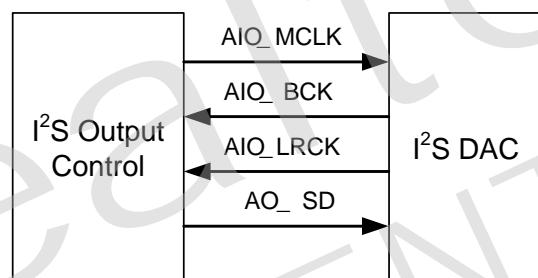
AIO\_MCLK and AIO\_BCK are the reference clock signals related to the output sampling rate.

AIO\_LRCK is used as the Word Select line to identify the signal source.

Figure 9 and Figure 10 show the I<sup>2</sup>S audio-out configuration.



**Figure 9. I2S Audio-Out Master Mode Interface Configuration**



**Figure 10. I2S Audio-Out Slave Mode Interface Configuration**

**Table 29. Audio-Out Block External Pin Description**

Pin Name	Type	Description
AIO_CK	DO	Main Clock Output to DAC
AIO_BCK	DB	I2S Bit Clock Output/Input to/from DAC
AIO_LRCK	DB	I2S Word Select Clock Output/Input to/from DAC
AO_SD	DB	I2S Serial Data Output for Downmixing Channels
ADAC_AOL	AO	Audio DAC Output Left Channel
ADAC_AOR	AO	Audio DAC Output Right Channel
ADAC_VREF	AO	Audio Reference VCM
ADAC_DACREF_33	PWR	AD/DA Reference Power
SPDIF	DO	IEC 60958 (SPDIF) Output

## 18. PCI Express 2.0

The RTD1395 complies with the PCI Express Base Specification Revision 2.0, and runs at 5GHz signal rate with 1x lane. PCI Express lane polarity reversal is also supported to ease PCB layout constraints.

PCI Express is used for extension cards such as 802.11n, 802.11ac Wi-Fi device and NIC device.

### 18.1. Features

- Refer to PCI Express Base Specification Revision 2.0
- Integrated PHY
- PCI Express Gen2.0(5Gbps) in Root Complex (RC) mode
- Built-in 100MHz reference clock (PCIE\_REFCLK\_P, PCIE\_REFCLK\_M)
- Supports 1x lane and polarity reversal
- Supports for 256 bytes payload size
- Support full address translation from PCIE address space to on-chip memory space

### 18.2. PCI Express 2.0 Block External Pin Description

Table 30. PCI Express 2.0 Block External Pin Description

Pin Name	IO Standard	Type	Description
PCIE_HSOP	Analog	AO	PCIe Differential Transmit Output
PCIE_HSON	Analog	AO	PCIe Differential Transmit Output
PCIE_HSIP	Analog	AI	PCIe Differential Receive Input
PCIE_HSIN	Analog	AI	PCIe Differential Receive Input
PCIE_REFCLK_P	Analog	AO	PCIe Differential Reference Clock
PCIE_REFCLK_M	Analog	AO	PCIe Differential Reference Clock
PCIE_CLKREQ	Analog	AO	PCIe Clock Request

### 18.3. Typical PCI Express 2.0 Application

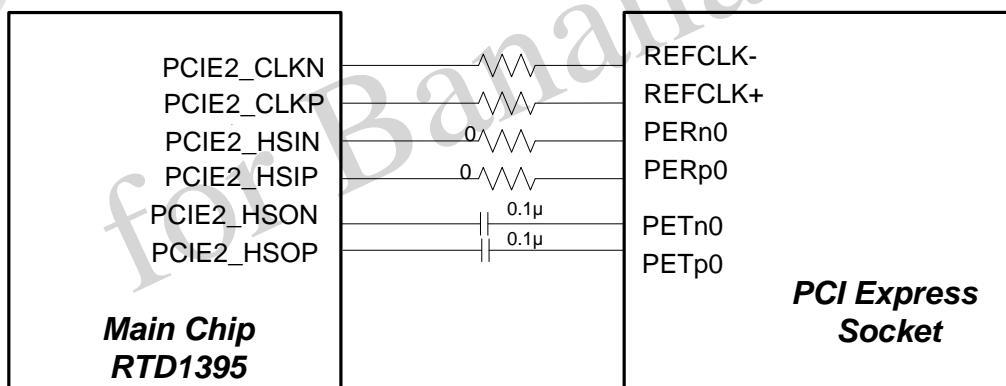


Figure 11. Typical PCI Express 2.0 Application

## 19. Ethernet Controller

The RTD1395 integrates a 10/100/1000M Ethernet MAC, 10/100M PHY, and optional SGMII. It provides full compliance with IEEE 802.3 compliant Media Access Controller and IEEE 802.3x Full Duplex Flow Control.

### 19.1. Features

- 10M and 100Mbps operation, compliant with IEEE 802.3, IEEE802.3u
- Supports Auto-Negotiation with Next Page capability
- Automatic Polarity Correction
- Supports auto MDIX
- Supports Link Down Power Saving
- 1000Mbps (SGMII only) operation
- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports Wake-on-LAN (WOL)
- Supports Full Duplex flow control (IEEE 802.3x)
- Supports IEEE 802.1Q VLAN tagging

### 19.2. Ethernet Block External Pin Description

**Table 31. Ethernet 10/100/1000M Block External Pin Description**

Pin Name	Type	Description
ETN_TXOP	AB	MDI mode: Transmit Output. MDIX mode: Receiver Input
ETN_RXIP	AB	MDI mode: Receiver Input.
ETN_RXIN	AB	MDIX mode: Transmit Output
ETN_LED0	DO	Ethernet LED0, 10M ACT/Link, programmable
ETN_LED1	DO	Ethernet LED1, 100M ACT/Link, programmable
SGMII_HSIP	AI	SERDES differential input. 1.25GHz serial interface to receive data from an external device that supports SGMII
SGMII_HSIN	AI	SERDES differential output. 1.25GHz serial interface to transmit data to an external device that supports SGMII
SGMII_HSOP	AO	SERDES differential output. 1.25GHz serial interface to transmit data to an external device that supports SGMII
SGMII_HSON	AO	SERDES differential output. 1.25GHz serial interface to receive data from an external device that supports SGMII
MDC	DO	Management Data Clock
MDIO	DB	Input/Output of Management Data

### 19.3. Typical Application

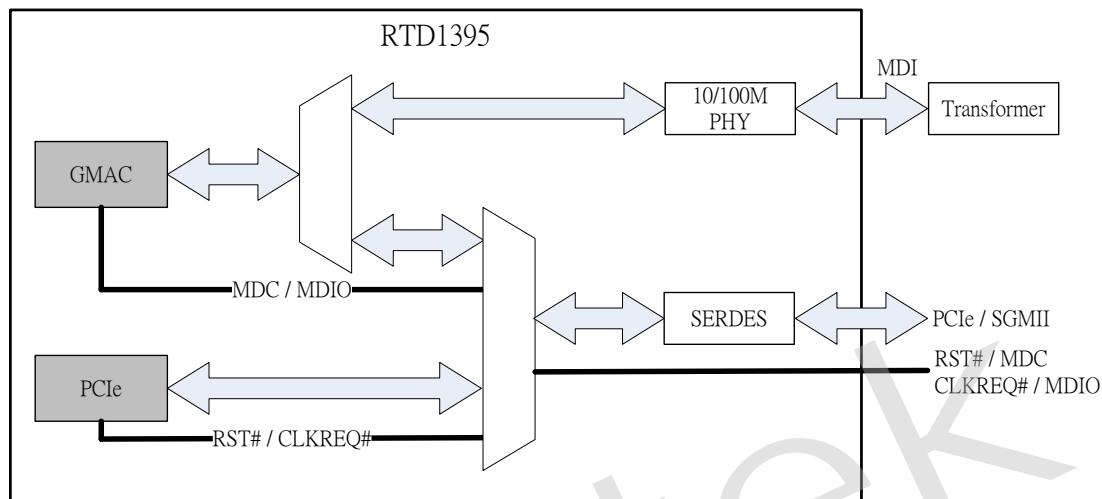


Figure 12. Relationship of PCIe and Ethernet Block

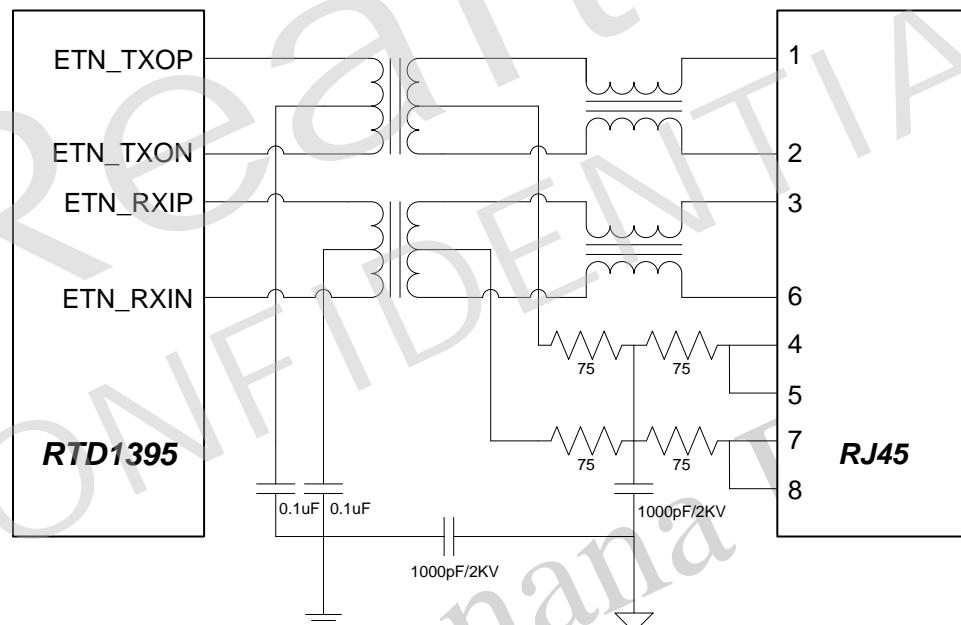


Figure 13. Typical Gigabit Ethernet Application

## 20. USB 2.0 Host/Device Controller

The RTD1395 contains three USB ports all complied with the USB 2.0 standards. First USB2.0 port can be configured as host or device by internal controller according to the role detection of extra CC1/CC2 pins. This port support Type C connector with USB2.0 traffic only and it can not be configured as host & device simultaneously. Only one role can be enabled at one time. For the rest two ports support host mode only.

### 20.1. Features

- CC1/CC2 two pins provide host or device role detection for first USB2.0 port.
- Complies with the XHCI specification and with the USB 2.0 specification
- Built-in termination resistor to reduce system cost
- Supports power management for downstream port devices

### 20.2. USB Block External Pin Description

Table 32. USB Block External Pin Description

Pin Name	Type	Description
USB_CC1	AB	USB Type C Port Configuration Channel
USB_CC2	AB	USB Type C Port Configuration Channel
USB_HSDP_0	AB	USB2.0 D+ Signal (USB2.0 HOST or DEVICE)
USB_HSDM_0	AB	USB2.0 D- Signal (USB2.0 HOST or DEVICE)
USB_HSDP_1	AB	USB2.0 D+ Signal (USB2.0 HOST only)
USB_HSDM_1	AB	USB2.0 D- Signal (USB2.0 HOST only)
USB_HSDP_2	AB	USB2.0 D+ Signal (USB2.0 HOST only)
USB_HSDM_2	AB	USB2.0 D- Signal (USB2.0 HOST only)

## 21. Transport Module

The transport module provides basic support for MPEG Transport Streams (TS) from transport interfaces. It supports several modern digital TV services. Two transport interfaces are supported in the RTD1395; both of which can operate simultaneously.

### 21.1. Features

- Supports terrestrial, cable, and satellite DTV
- Supports two serial inputs

### 21.2. Transport Module External Pin Description

**Table 33. Transport Module External Pin Description**

Pin Name	Type	Description
TP0_SYNC	DI	Primary Transport Stream Input SYNC
TP0_VALID	DI	Primary Transport Stream Input Data Valid
TP0_CLK	DI	Primary Transport Stream Input Clock
TP0_DATA	DI	Primary Transport Stream Input Data
TP1_SYNC	DI	Secondary Transport Stream Input SYNC
TP1_VALID	DI	Secondary Transport Stream Input Data Valid
TP1_CLK	DI	Secondary Transport Stream Input Clock
TP1_DATA	DI	Secondary Transport Stream Input Data

## 22. Card Reader Controller

The card reader controller supports SD card. The data bit width is up to 4 bits.

### 22.1. Features

- SD 3.0 (4-bit bus width, clock frequency up to 208 MHz)

### 22.2. Card Reader Block External Pin Description

Table 34. Card Reader Block External Pin Description

Pin Name	Type	Description
SD_WP	DI	SD/MMC Write Protect
SD_CD	DI	SD/MMC Card Detect
SD_CLK	DO	SD/MMC Clock Output
SD_CMD	DB	SD/MMC Command Line
SD_D[3:0]	DB	SD/MMC Data[3:0]

## 23. SDIO

The SDIO controller supports SDIO. The data bit width is up to 4 bits.

### 23.1. Features

- SDIO 3.0 (4-bit bus width, clock frequency up to 208 MHz)

### 23.2. Card Reader Block External Pin Description

Table 35. Card Reader Block External Pin Description

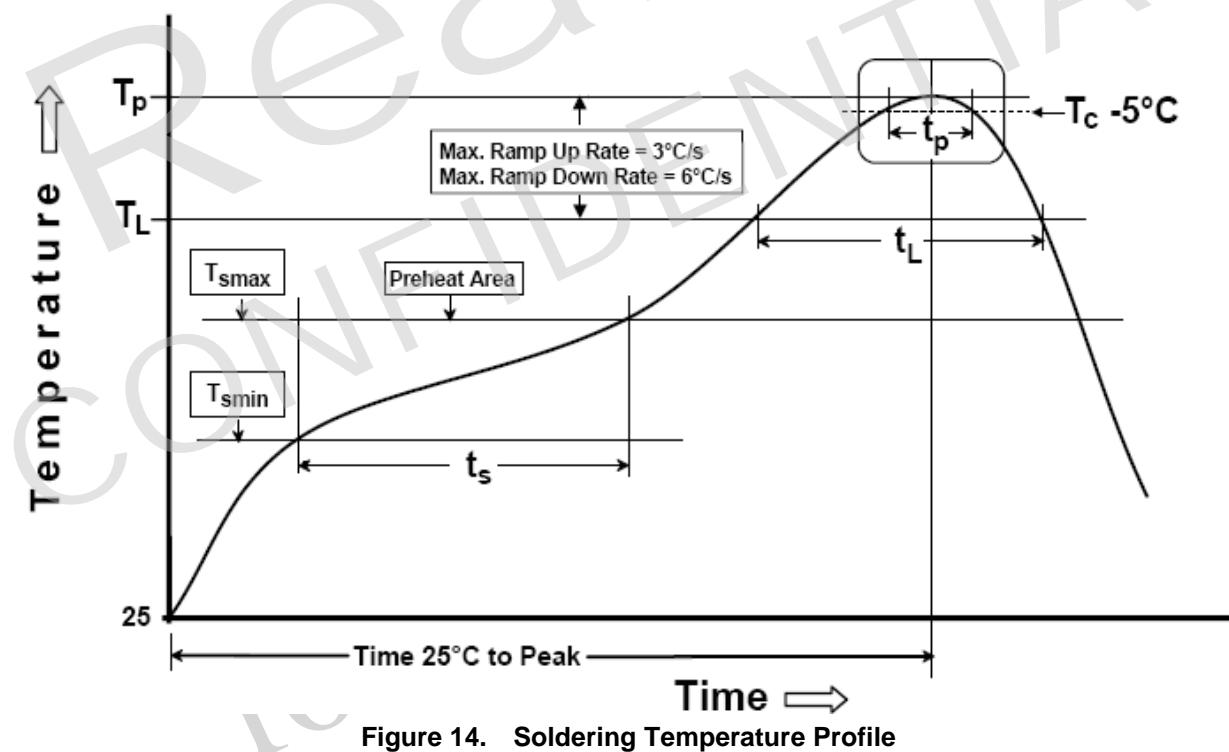
Pin Name	Type	Description
SDIO_CLK	DO	SDIO Clock Output
SDIO_CMD	DB	SDIO Command Line
SDIO_D[3:0]	DB	SDIO Data[3:0]

## 24. Soldering Reflow Profile

The reflow profile is for MSL classification only, not a recommendation for SMT process. Actual board assembly profiles should be developed based on specific process needs and board designs, and should not exceed the parameters in Table 36.

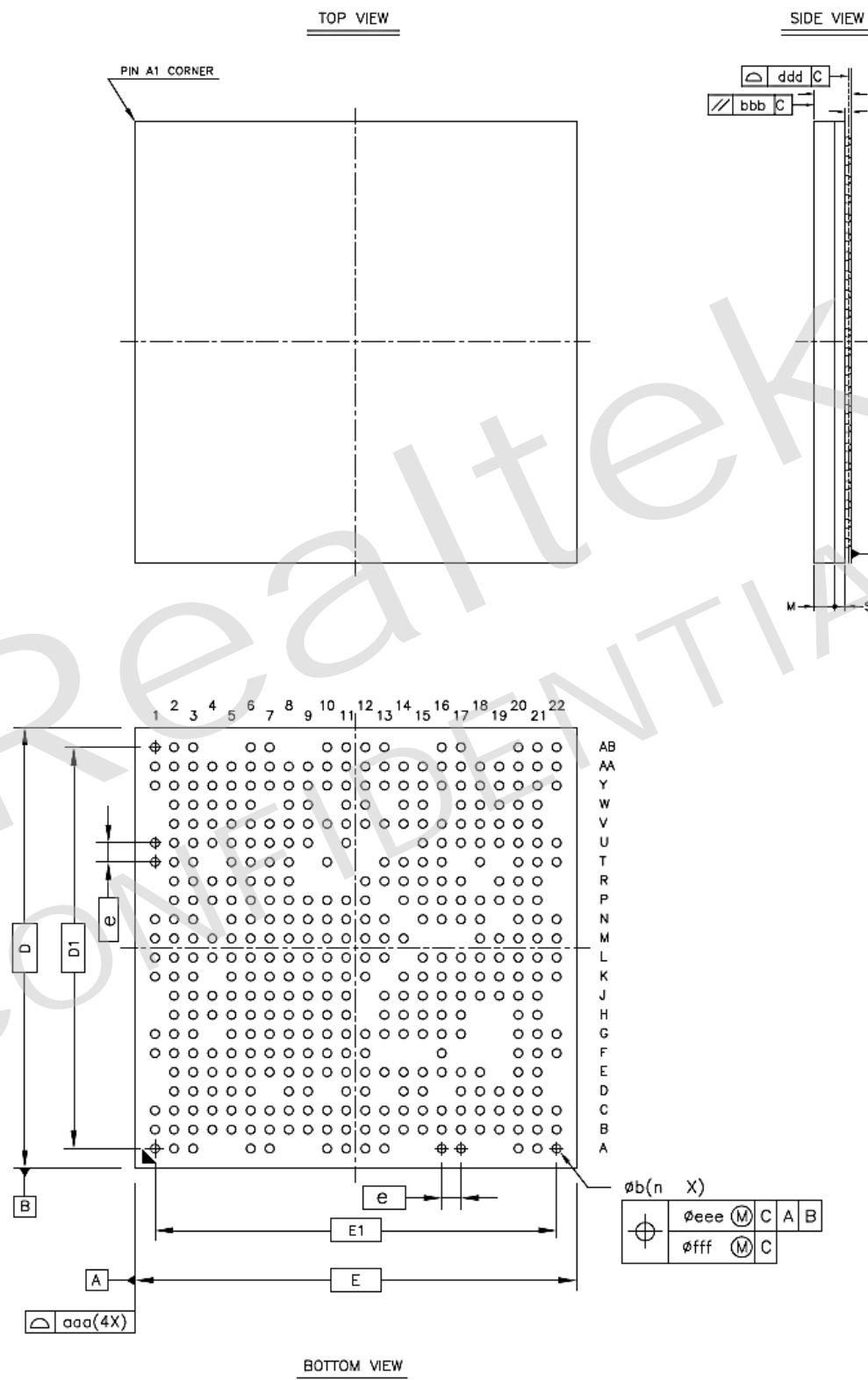
**Table 36. Classification Reflow Profile**

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate ( $T_L$ to $T_p$ )	3°C/second max
Preheat	
$T_{s\min}$	150°C min
$T_{s\max}$	200°C max
$t_s$	60~120 seconds
Time Maintained Above $T_L$	217°C
$t_L$	60~150 seconds
Peak Package Body Temperature ( $T_p$ )	260°C max
Time ( $t_p$ ) within 5°C of Actual Peak Temperature	30 seconds
Ramp-Down Rate ( $T_p$ to $T_L$ )	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



**Figure 14. Soldering Temperature Profile**

## 25. Mechanical Dimensions



## 25.1. Mechanical Dimensions Notes

	Symbol	Common Dimensions		
		MIN.	NOM.	MAX.
Package :		LFBGA		
Body Size:	X	E	15.000	
	Y	D	15.000	
Ball Pitch :		e	0.650	
Total Thickness :		A		1.700
Mold Thickness :		M	0.700	Ref.
Substrate Thickness :		S	0.360	Ref.
Ball Diameter :			0.300	
Stand Off :	A1	0.160	—	0.260
Ball Width :	b	0.270	—	0.370
Package Edge Tolerance :	aaa	0.150		
Mold Flatness :	bbb	0.200		
Coplanarity:	ddd	0.080		
Ball Offset (Package) :	eee	0.150		
Ball Offset (Ball) :	fff	0.080		
Ball Count :	n	406		
Edge Ball Center to Center :	X	E1	13.650	
	Y	D1	13.650	

Note: Dimensions Unit: mm.

## 26. Ordering Information

Table 37. Ordering Information

Part Number	Description	Status
RTD1395DB-VA1-CG	406-Pin TFBGA. Dolby and DTS certified	-
RTD1395DC-VA1-CG	406-Pin TFBGA. Dolby certified	-
RTD1395PB-VA1-CG	406-Pin TFBGA	-

*Note: Only licensees certified by the original licensor(s) are eligible to purchase these products.*

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