Register 1

```
always @(pos edge clk) begin
    if (wrenable) begin
        q = d;
    end
end
```


Data

Wrenable

clock

Q
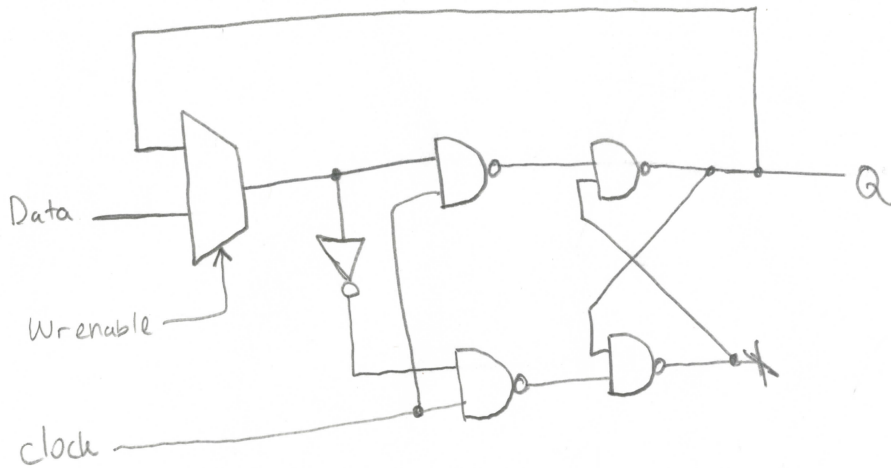
Register 2

```
always @(pos edge (clk & wrenable)) begin
    q = d;
end
```


data

enable

clock

Q

X
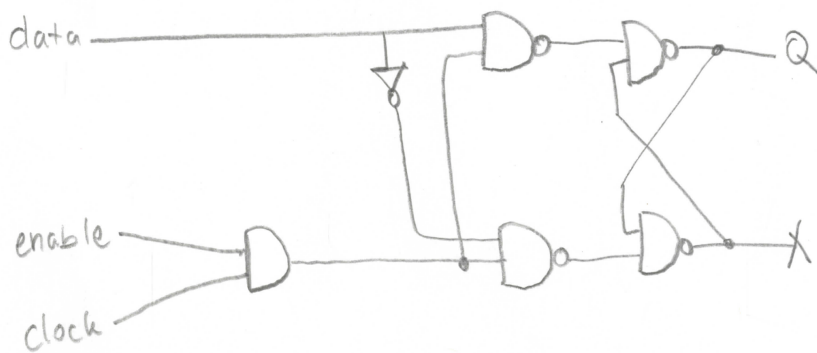
Used resources from: tams.informatik.uni-hamburg.de/applets/hades/webdemos/-
16-flipflops/20-dlatch/dff-enable.html