

# A Thorough Examination of the Differential Difference Amplifier

Logan Sweet & Maggie Jakus

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## 1 Introduction

For our final project, we studied the differential difference amplifier (DDA). A DDA has four inputs, as seen in figure 1. The DDA amplifies the differential mode voltage, the voltage difference between the two input ports. Ideally, the DDA amplifies the differential mode voltage infinitely:

$$V_{out} = \mu V_{dm} = \mu[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})] \text{ as } \mu \rightarrow \infty [2] \quad (1)$$

The DDA has two differential pairs of transistors, and relies on the two pairs of transistors being below saturation. In the ohmic region, small changes in the voltage across a transistor ( $V_{DS}$ ) result in large changes in current, while when a transistor is in saturation, changes in  $V_{DS}$  result in only very minor changes in current due to the Early effect. In the DDA, the gate voltage on one (or more) of the differential pair transistors is changed, which results in the common-node voltage changing and the current in the differential pair transistors changing. This propagates throughout the circuit, causing the output voltage to increase or decrease, depending on which gate voltage was changed and in what direction.

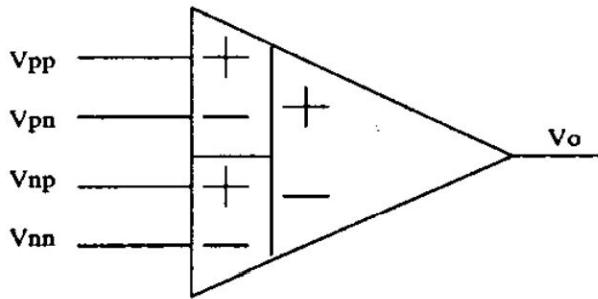


Figure 1: The DDA has a noninverting port (inputs  $V_{pp}$  and  $V_{pn}$ ) and an inverting port ( $V_{np}$  and  $V_{nn}$ ) [1].

## 2 Experiments

For this lab, we built three DDAs on breadboards and in LTSpice. For each circuit, we conducted the following experiments:

## Experiment 1

In experiment 1, we set three of the inputs to 3V and swept the fourth output from rail to rail, measuring  $V_{out}$ . We repeated this with the three inputs at 3.5V and 4V, and then repeated this measurement for each input.

## Experiment 2

In experiment 2, we identified which of the four inputs were inverting (raising the gate voltage on those would decrease the output voltage) and which of the four inputs were noninverting (raising the gate voltage on those raises the output voltage). For one of the inverting inputs, we set the other three inputs to 3V and swept the inverting input in fine increments around the other three, measuring  $V_{out}$ . We repeated this with the noninverting input. From this, we calculated the differential mode voltage gain of the circuit  $A_{dm}$ .

## Experiment 3

In experiment 3, we set  $V_{dm} = 0$  (all inputs were set to 3V) and swept  $V_{out}$  from rail to rail, measuring  $I_{out}$ . We used this to find the incremental output resistance  $R_{out}$ .

## Experiment 4

For experiment 4, we set  $V_{out}$  to a value for which the circuit's gain was large (around 2V) and swept first a noninverting input around the other three inputs (which were all set to the same value, 3V) and measured  $I_{out}$ , and then did the same thing with an inverting input. From this we calculated the incremental transconductance gain  $G_m$ .

## Experiment 5

In experiment 5, we constructed a unity gain follower circuit, connecting the noninverting inputs to  $V_{in}$  and the inverting inputs to  $V_{out}$ . We measured  $V_{out}$  as we swept  $V_{in}$  from rail to rail.

## Circuit 1

The first circuit we built and tested was an adaptation of the DDA shown in *A CMOS Fully Balanced Differential Difference Amplifier and Its Applications* [1]. The benefit of this circuit is that it has a very high gain. The drawbacks will be seen in the data. We both built this on a breadboard and simulated it in LTSpice. The circuit we built had a rail to rail voltage range of 5V; the circuit we simulated had a rail to rail voltage range of 6V. The configuration can be seen in figure 2, and as built on a breadboard in 3.

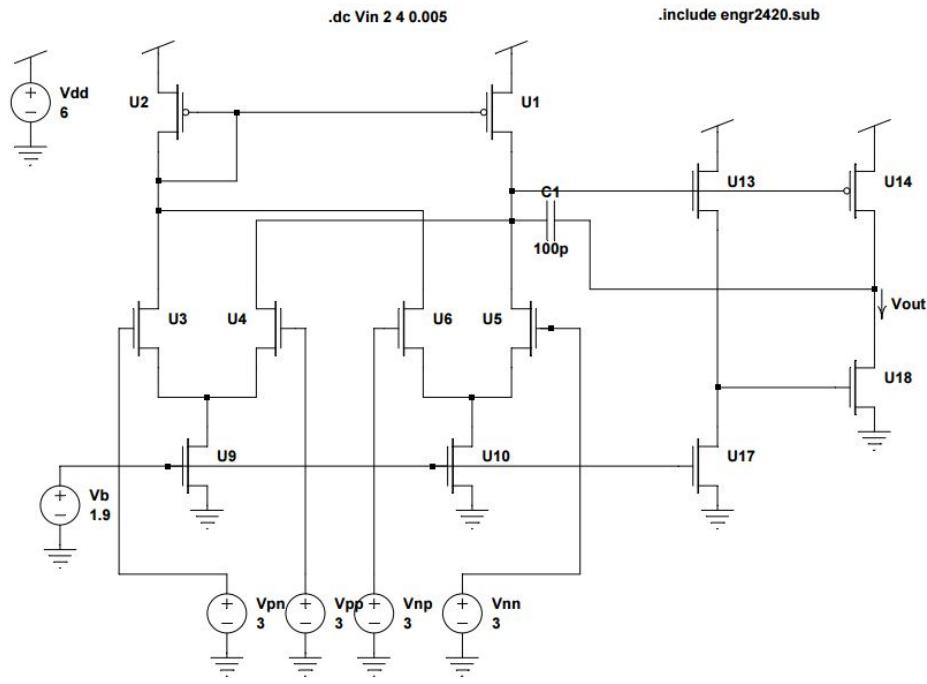


Figure 2: The setup used. For both the build and the simulation, we set  $V_b = 1.9V$ .  $V_{pn}$  and  $V_{np}$  are the inverting inputs, and  $V_{pp}$  and  $V_{nn}$  are the noninverting inputs.

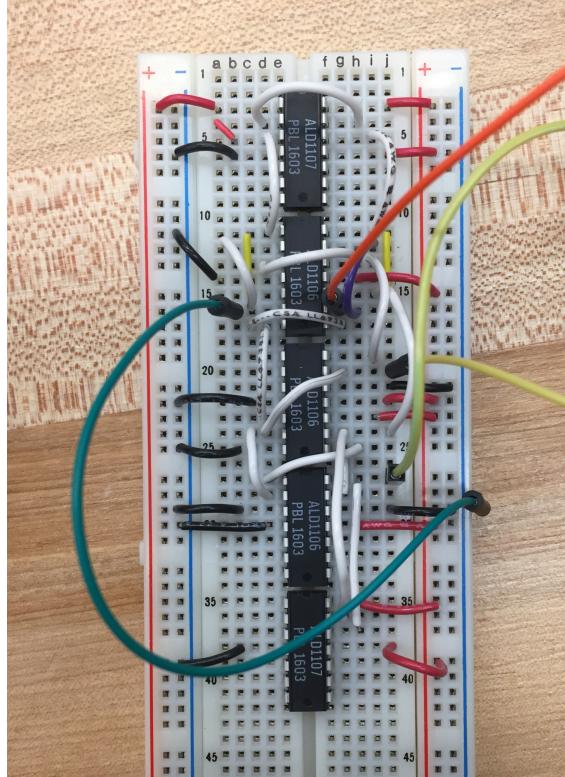


Figure 3: The circuit on a breadboard that we used for data collection.

Part of the reason we both built and simulated this circuit was because of the nonideal behavior we noticed when we first built and tested the circuit. We hoped that simulating the circuit with a slightly larger power supply would yield results that would better align with our expectations of a circuit given our experience in this class. However, as can be seen in the data, the simulation performed similarly to (and often worse than) the actual circuit. For all experiments on this circuit, both built and simulated, we set the bias voltage to around 1.9V. We did this so we could supply sufficient current to the circuit.

### Circuit 1: Experiment 1

We know that  $A_{dm} = R_{out}G_m$ . Using our values we extracted in experiments 3 and 4, we found that  $A_{dm} = 509.46$  for the built circuit and  $A_{dm} = 257.54$  for the simulated circuit. The built circuit has a fairly high gain (and this value is similar to the value extracted from experiment 2), but the value is not quite as high as we expected. This could be due to the limited number of points we were able to get in the high gain region. The simulation consistently underperformed the built circuit.

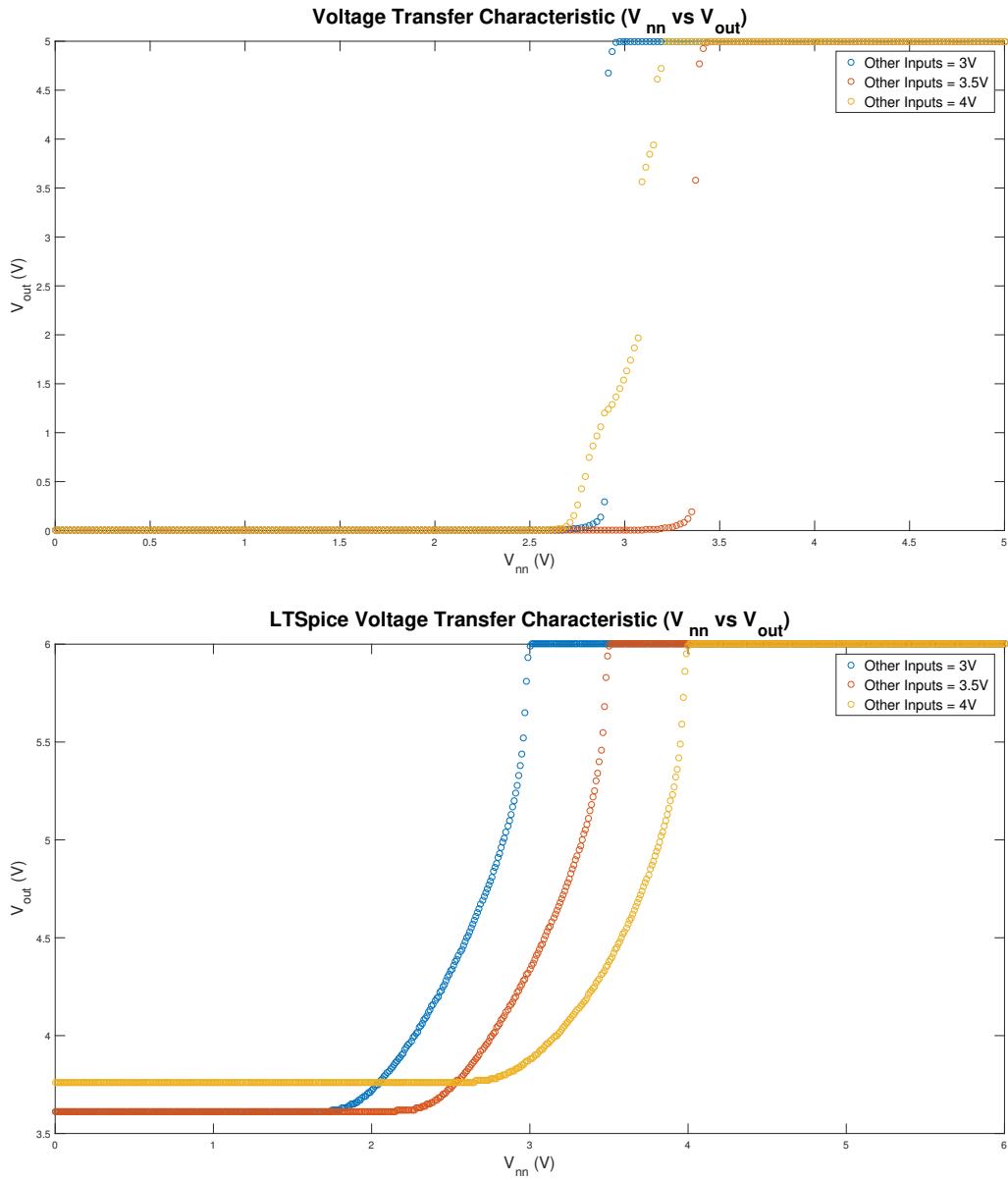


Figure 4: The voltage transfer characteristic of the circuit while sweeping a noninverting input from the built circuit (top) and the LTSpice simulation (bottom). The built circuit shows a higher gain for other inputs = 3V and 3.5V, but the SMU did not capture sufficient points in that region. We are unsure about what happened when other inputs = 4V.

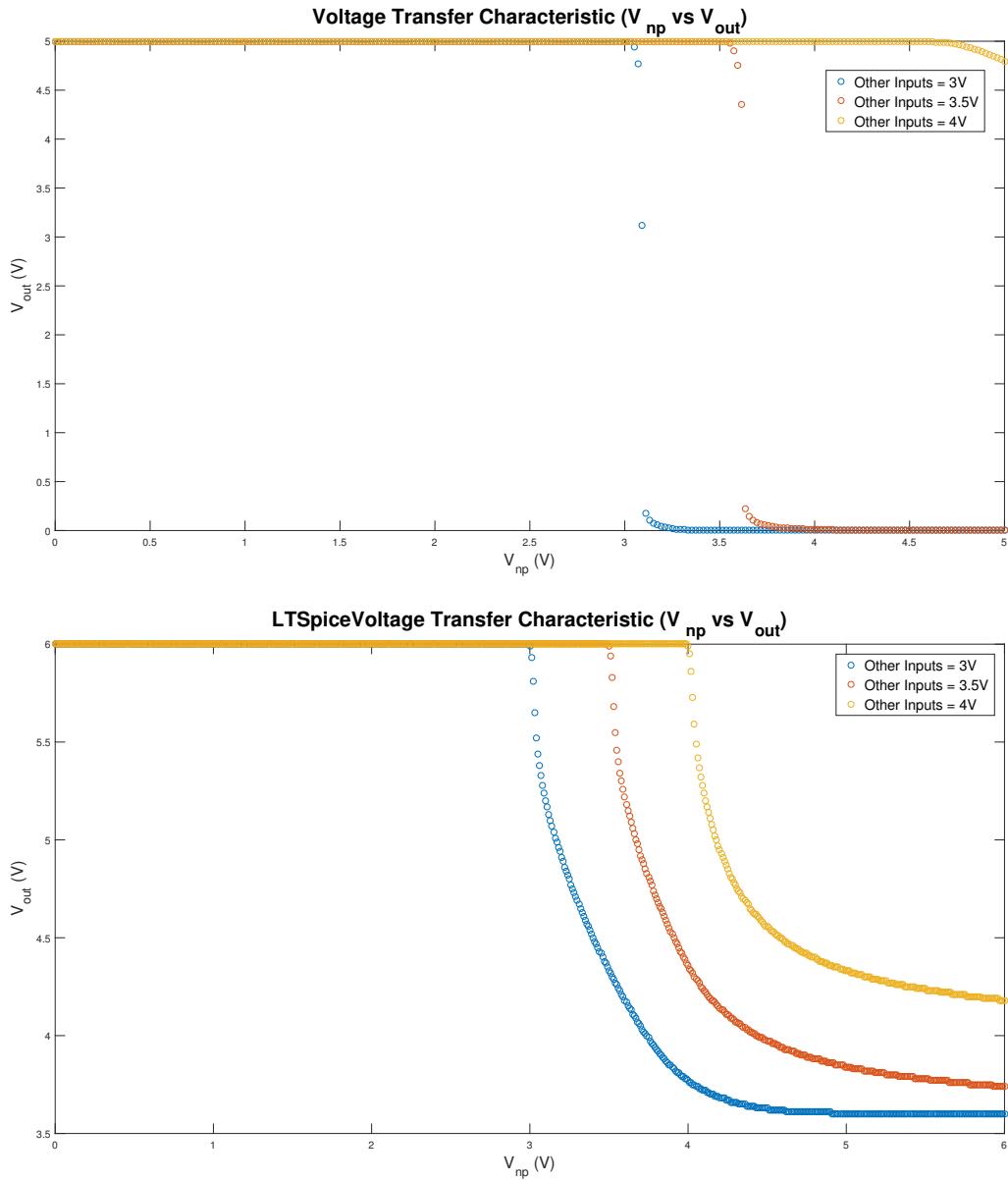


Figure 5: The voltage transfer characteristic of the circuit while sweeping an inverting input from the built circuit (top) and the LTSpice simulation (bottom). The built circuit shows a higher gain for other inputs = 3V and 3.5V, but the SMU did not capture sufficient points in that region. We are unclear what happened when other inputs = 4V.

## Circuit 1: Experiment 2

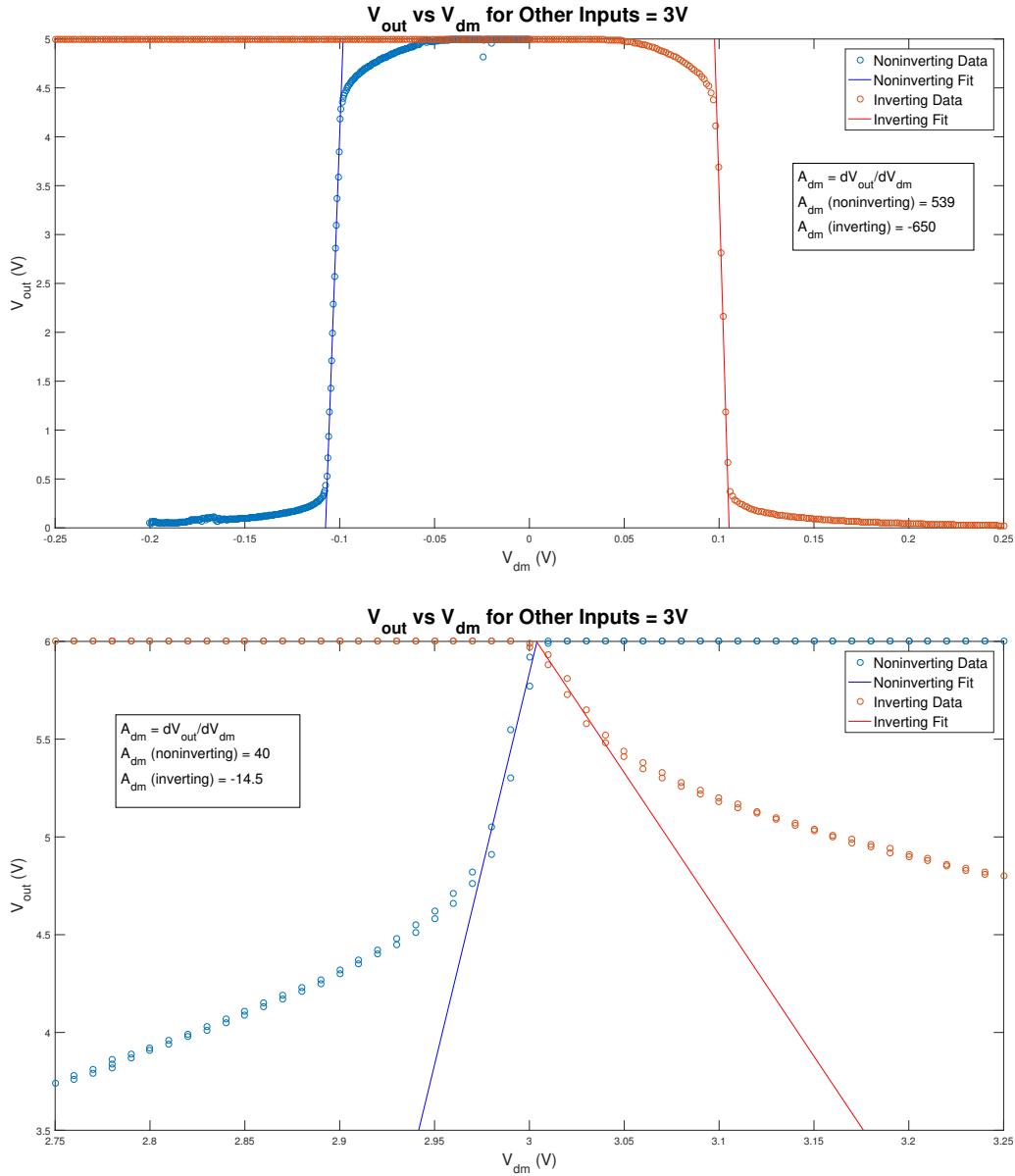


Figure 6: The built circuit (top) shows a much higher differential mode voltage gain (average absolute value of 594) than the LTSpice simulated circuit (bottom, average absolute value of 27.25). If we had taken more points in the LTSpice simulation, we may have seen a higher gain.

## Circuit 1: Experiment 3

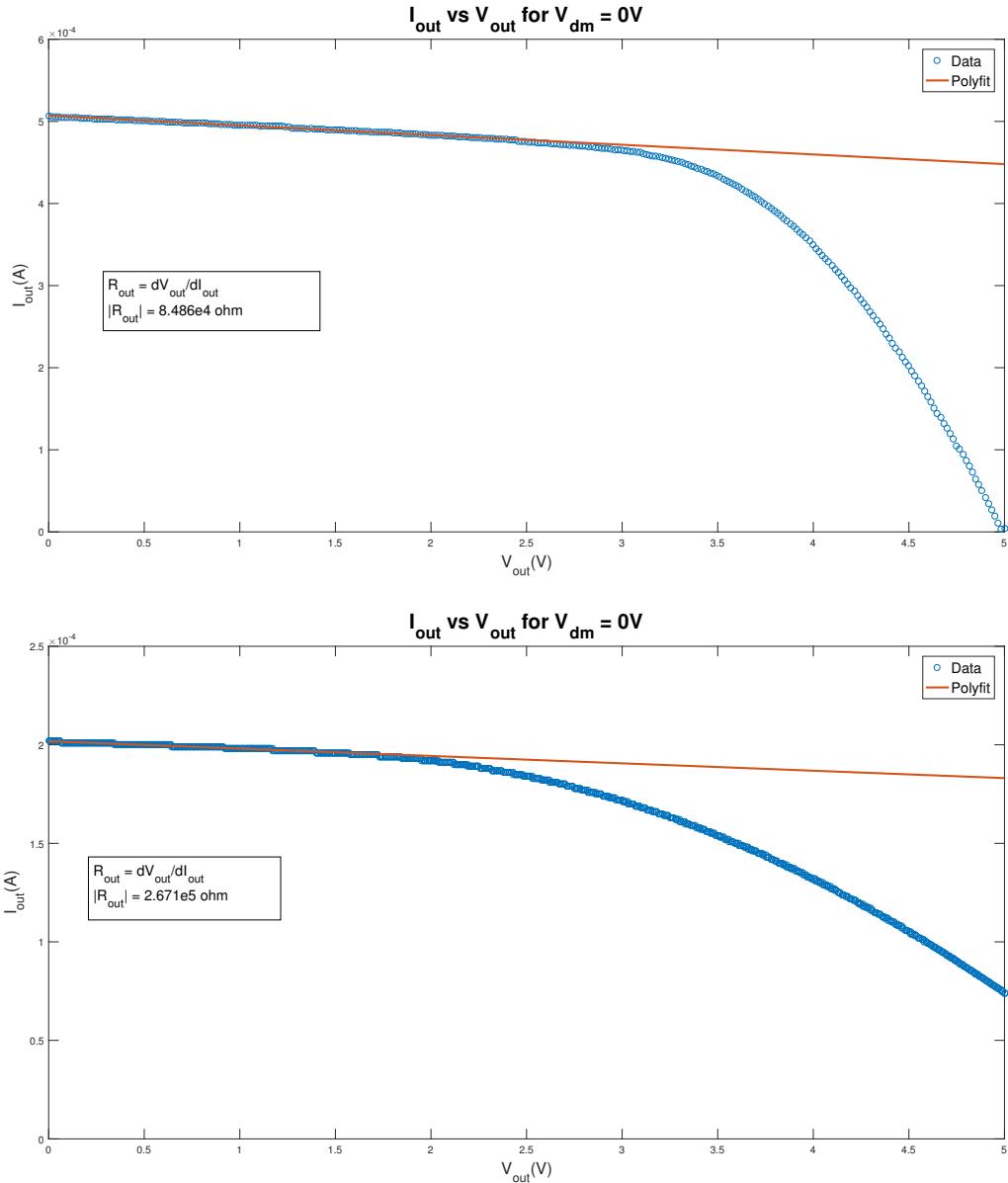


Figure 7: The LTSpice simulation data (bottom) had a higher incremental output resistance than did the built circuit (top).

## Circuit 1: Experiment 4

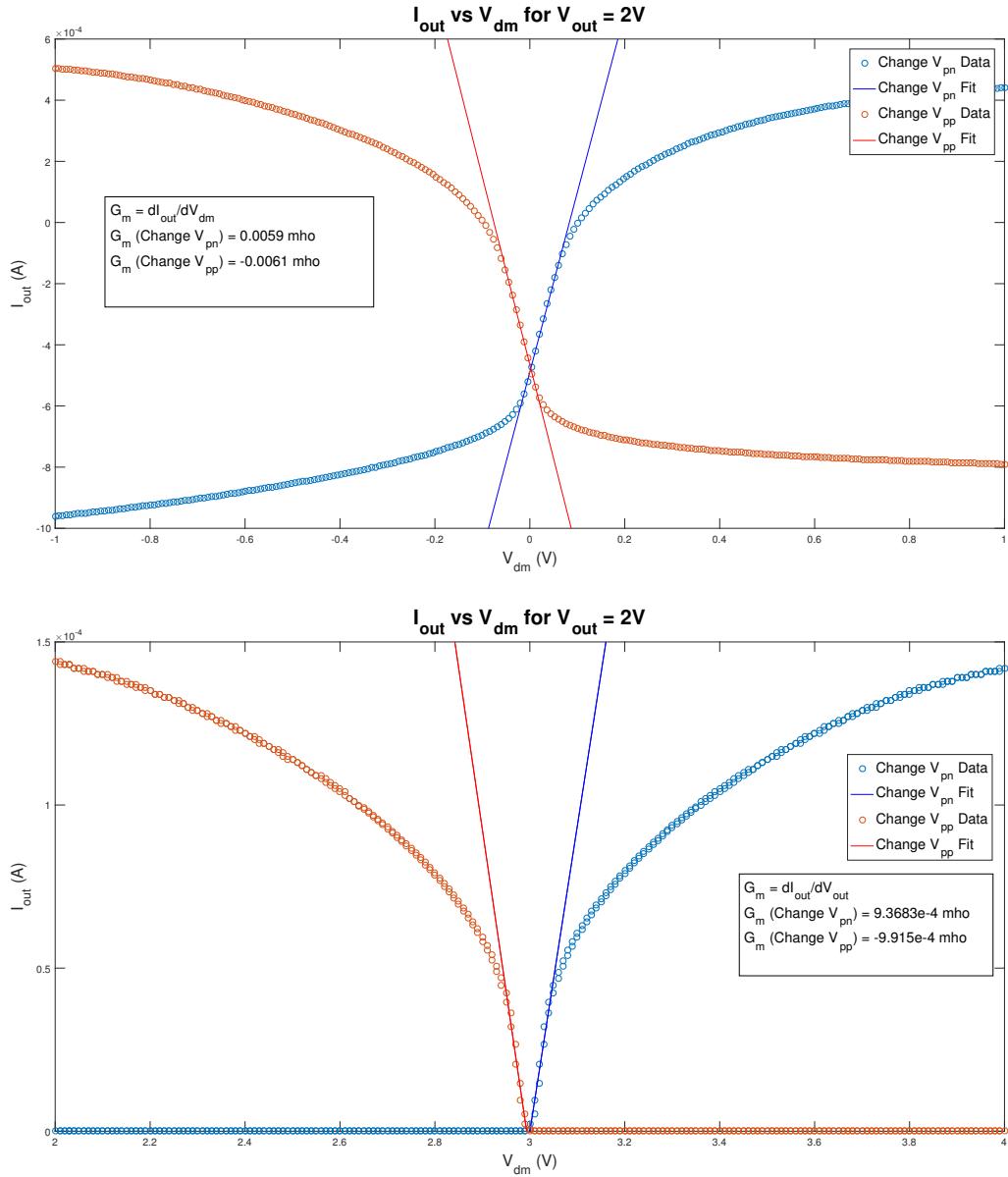


Figure 8: Measured circuit data (top) and LTSpice simulation data (bottom). We extracted the incremental transconductance gain  $G_m$ .

## Circuit 1: Experiment 5

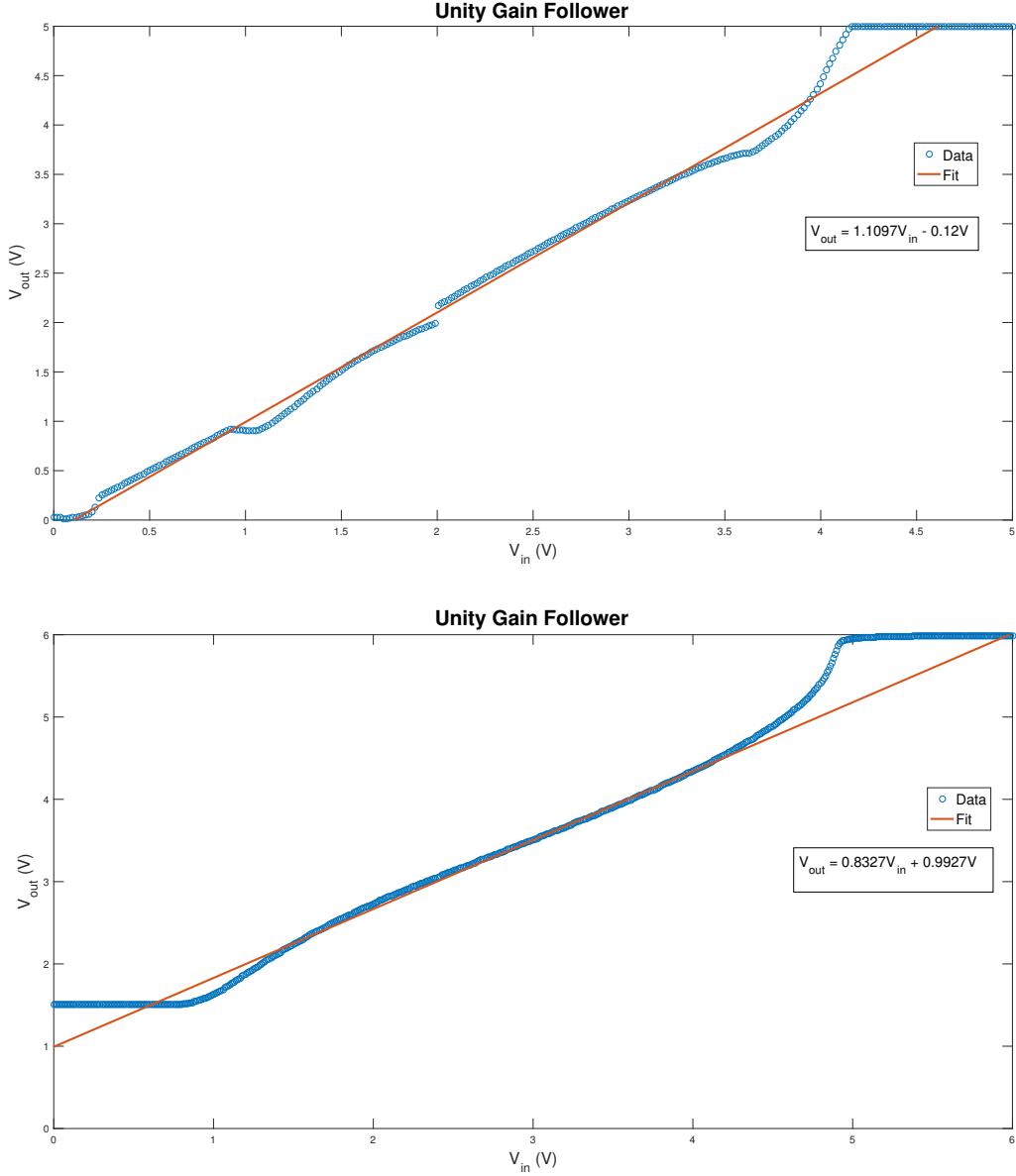


Figure 9: Collected circuit data (top) and simulated data (bottom) for the unity gain follower. This follower generally has a gain of 1 from  $V_{in} = 0.25V$  to  $V_{in} = 3.5V$ . However, the behavior is not completely linear, and jumps and then plateaus at high voltages. We do not know why this is the case.

## Circuit 2

The second circuit we built and simulated is the circuit seen in figure 10, and as built on a breadboard in 11. We ran both the built circuit and the simulation on a rail to rail voltage supply of 5V. All tests on the built circuit had a bias voltage of approximately 1.9V. To get a better understanding of the role bias voltage plays in the DDA, we ran all of our LTSpice simulations with  $V_b = 2V$

(similar to what we had built) and some additionally with  $V_b = 0.7V$  (just above threshold).

Using values we extracted in experiments 3 and 4 for  $G_m$  and  $R_{out}$  (with  $V_b \approx 2V$ , we calculated the differential-mode gain of the built and simulated circuits. We calculated that the built circuit had a gain of 15.98 and the simulated circuit had a gain of 9.44.

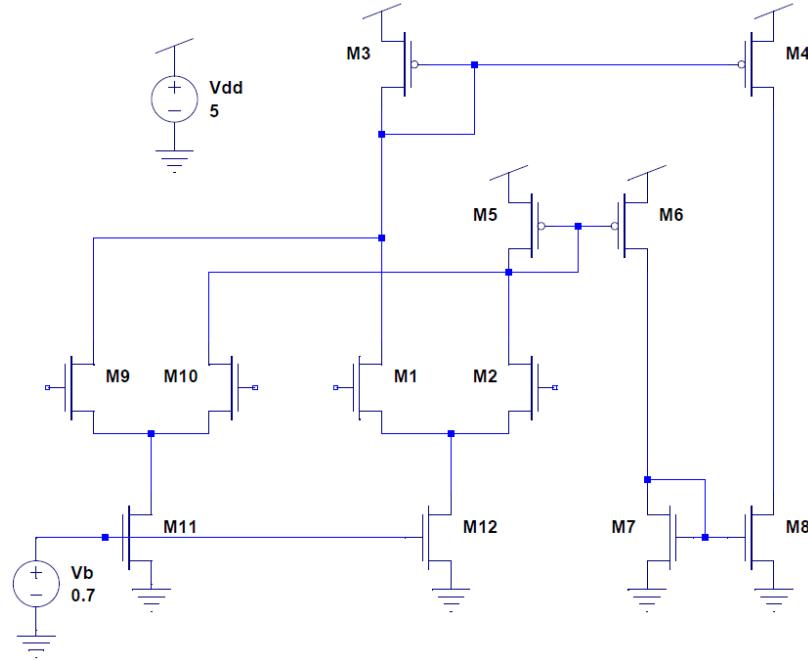


Figure 10:  $V_{out}$  was measured at the node between M4 and M8. M9 and M1 are the noninverting inputs, and M10 and M2 are the inverting inputs.

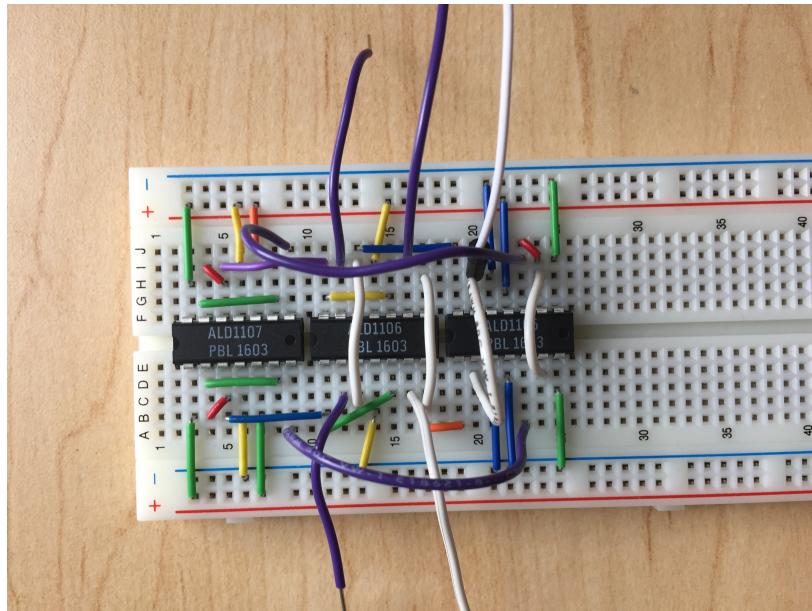


Figure 11: The circuit on a breadboard that we used for data collection.

## Circuit 2: Experiment 1

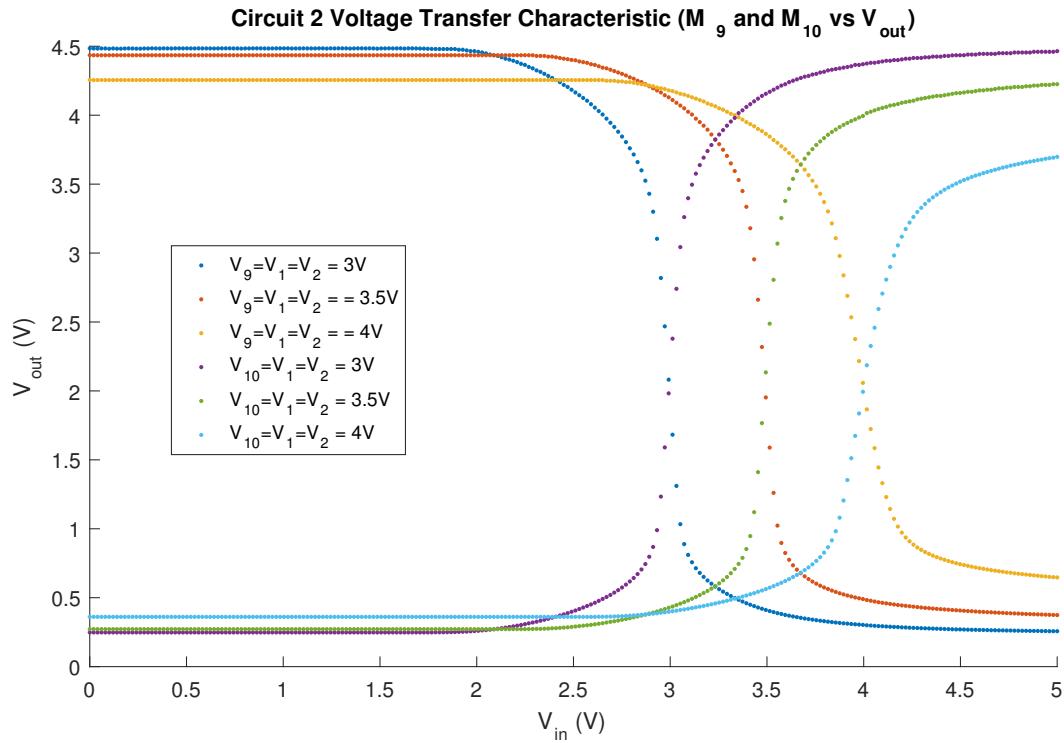


Figure 12: The voltage transfer characteristics with other inputs equal 3V, 3.5V, and 4V. As you increase  $V_{in}$ ,  $V_{out}$  increases for noninverting inputs and decreases for inverting inputs. This is actual data collected from the built circuit.

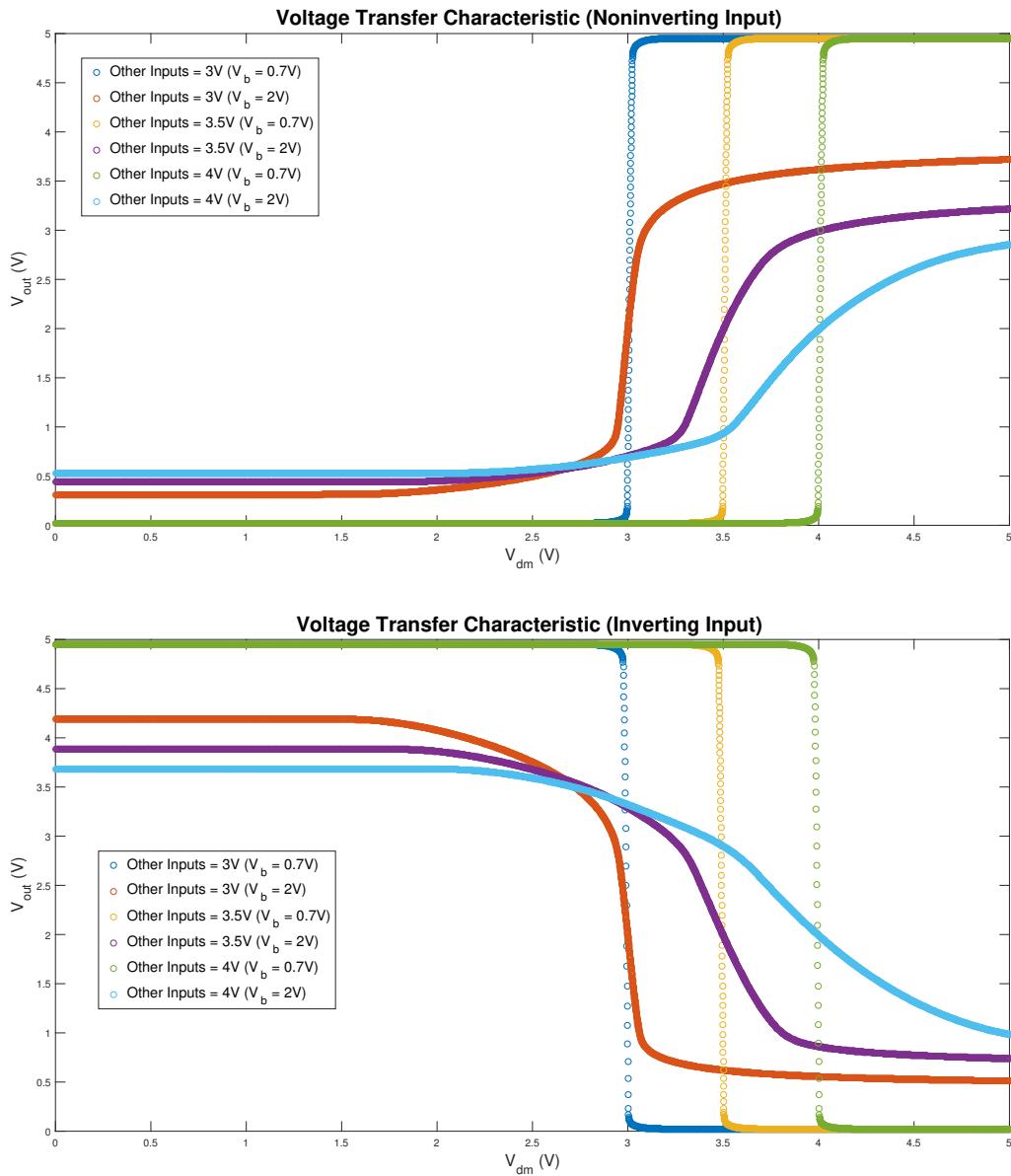


Figure 13: The LTSpice-generated voltage transfer characteristics for the noninverting case (top) and inverting case (bottom). The bias voltage has a significant effect on the voltage transfer characteristic.

## Circuit 2: Experiment 2

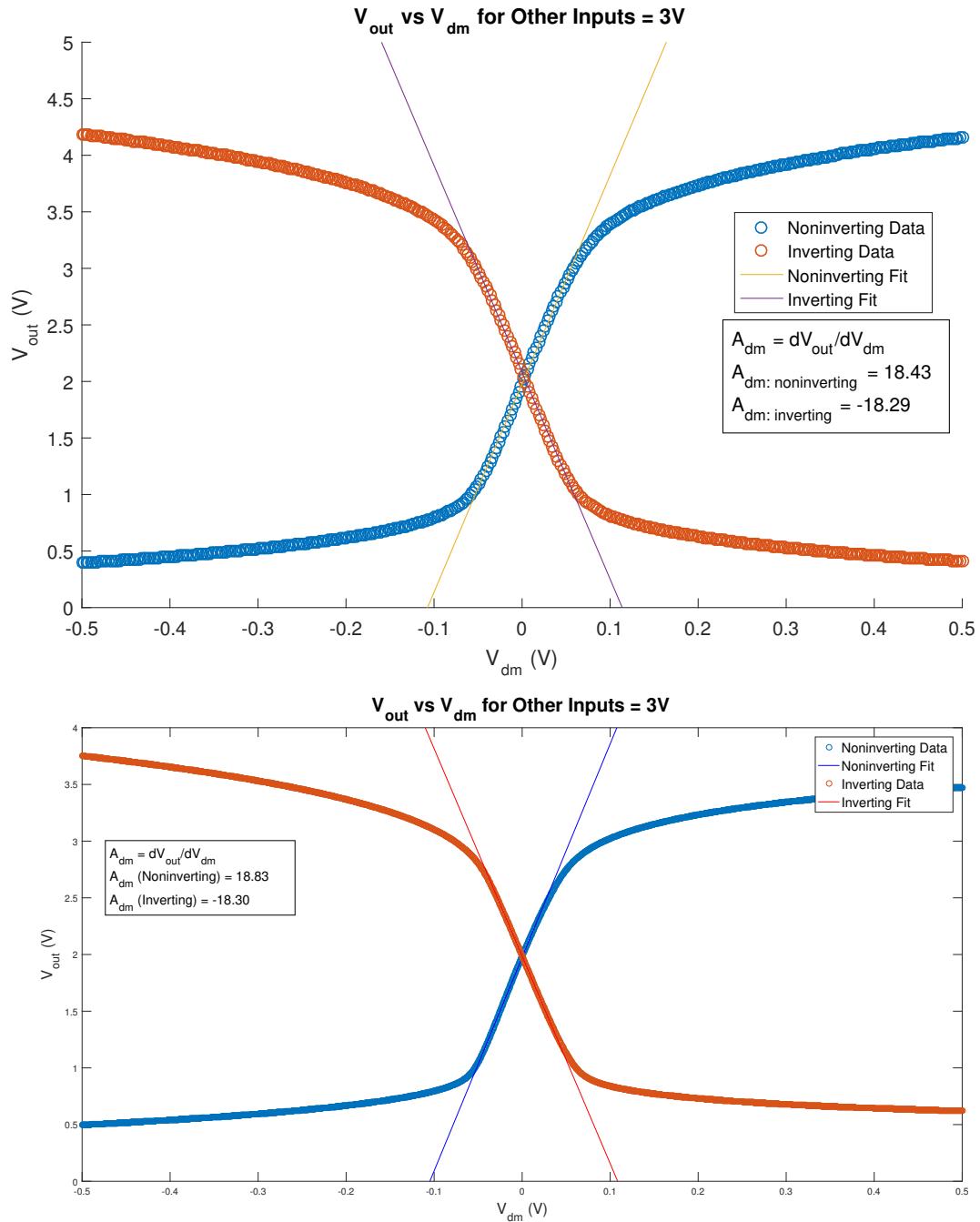


Figure 14: The differential mode voltage gain ( $A_{dm}$ ) was extracted from the built circuit (top) and the simulated circuit (bottom). The gain was much smaller for this circuit than it was for circuit 1.

## Circuit 2: Experiment 3

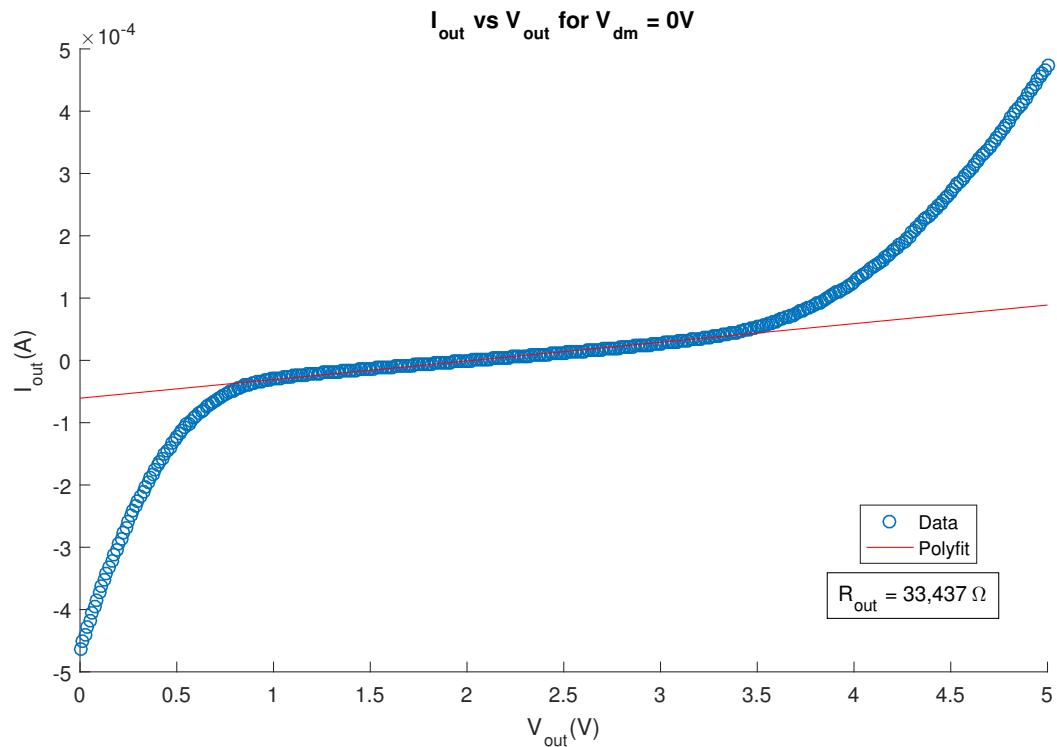


Figure 15: Collected data from our physical circuit. The inverse of the slope at the flat part is incremental output resistance ( $R_{out}$ )

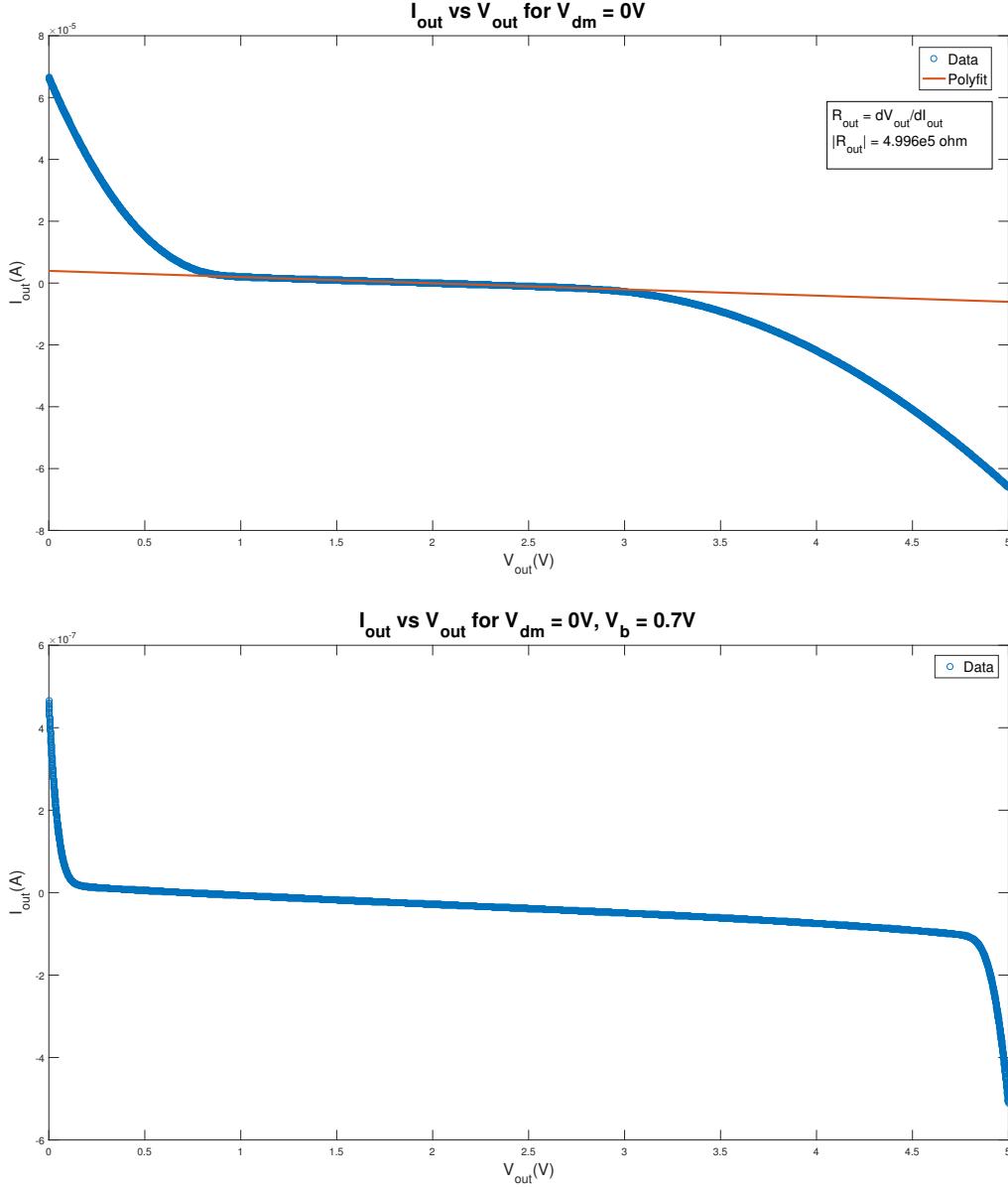


Figure 16: LTSpice simulation data. The top circuit has a bias voltage of 2V, which provides enough current for the circuit, as can be seen by the order of magnitude of the y-axis (10s of microamps). We tested the same circuit and experiment but with a bias voltage of 0.7V, which puts the bias transistors just above threshold in moderate inversion. This does not provide sufficient current for the circuit, as can be seen by the order of magnitude of the y-axis (nanoamps). This was particularly helpful to our understanding of the role of bias voltage in a circuit.

## Circuit 2: Experiment 4

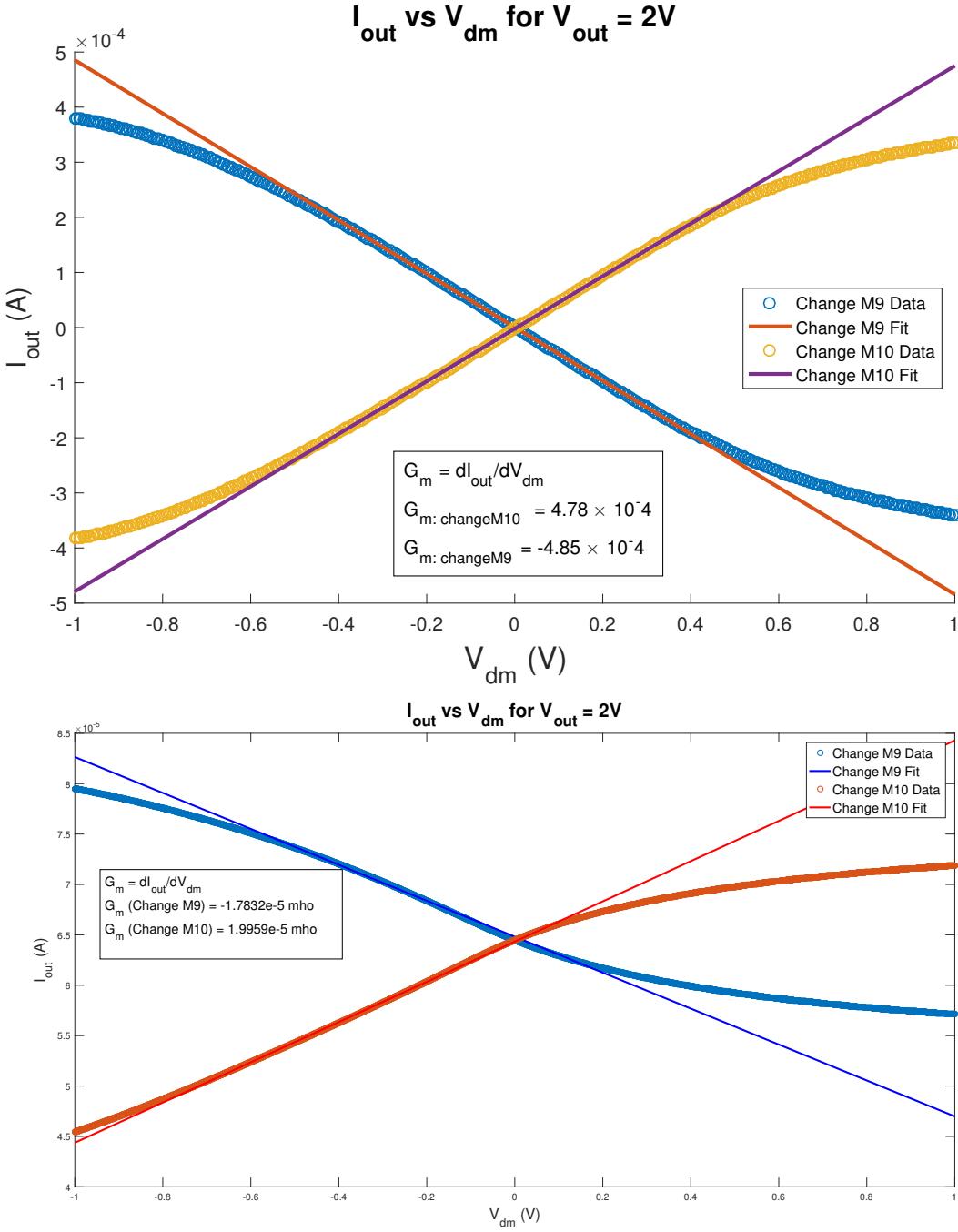


Figure 17: Measured circuit data (top) and LTSpice simulation data (bottom). We extracted the incremental transconductance gain  $G_m$ . We also ran simulations with the bias voltage  $V_b = 0.7V$ , but the data are not shown. Like in experiment 3, the current was on the order of nanoamps, not microamps, once again highlighting the importance of  $V_b$  in providing sufficient current for the circuit.

## Circuit 2: Experiment 5

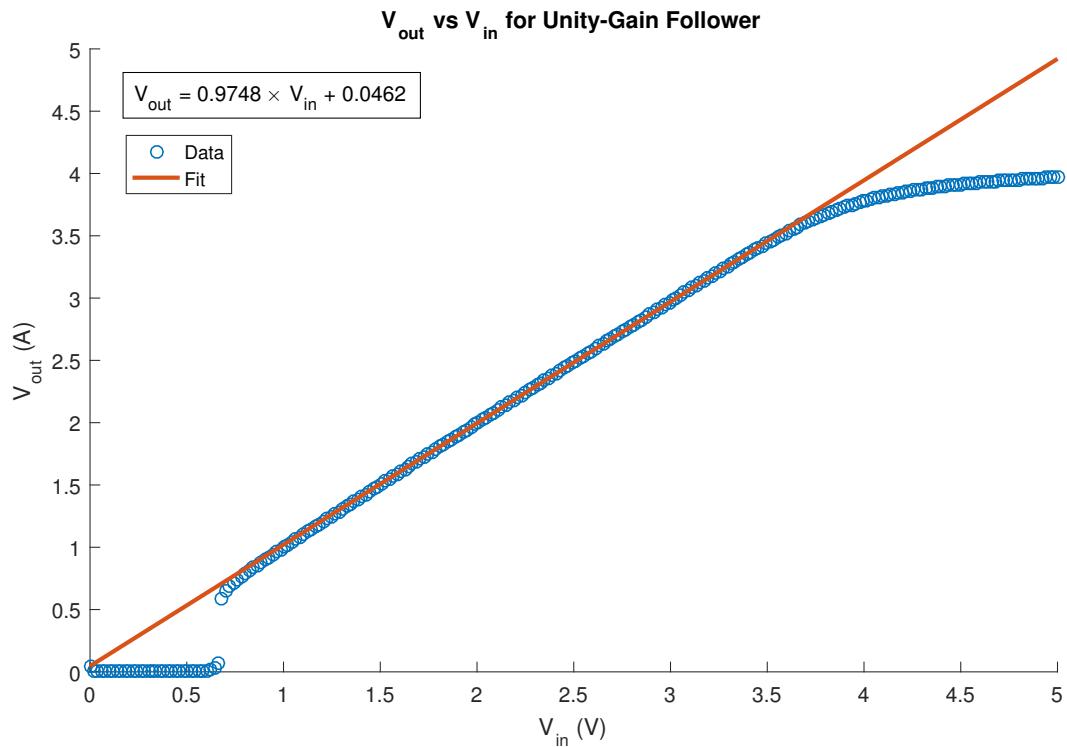


Figure 18: Collected data for the unity-gain connected built circuit.

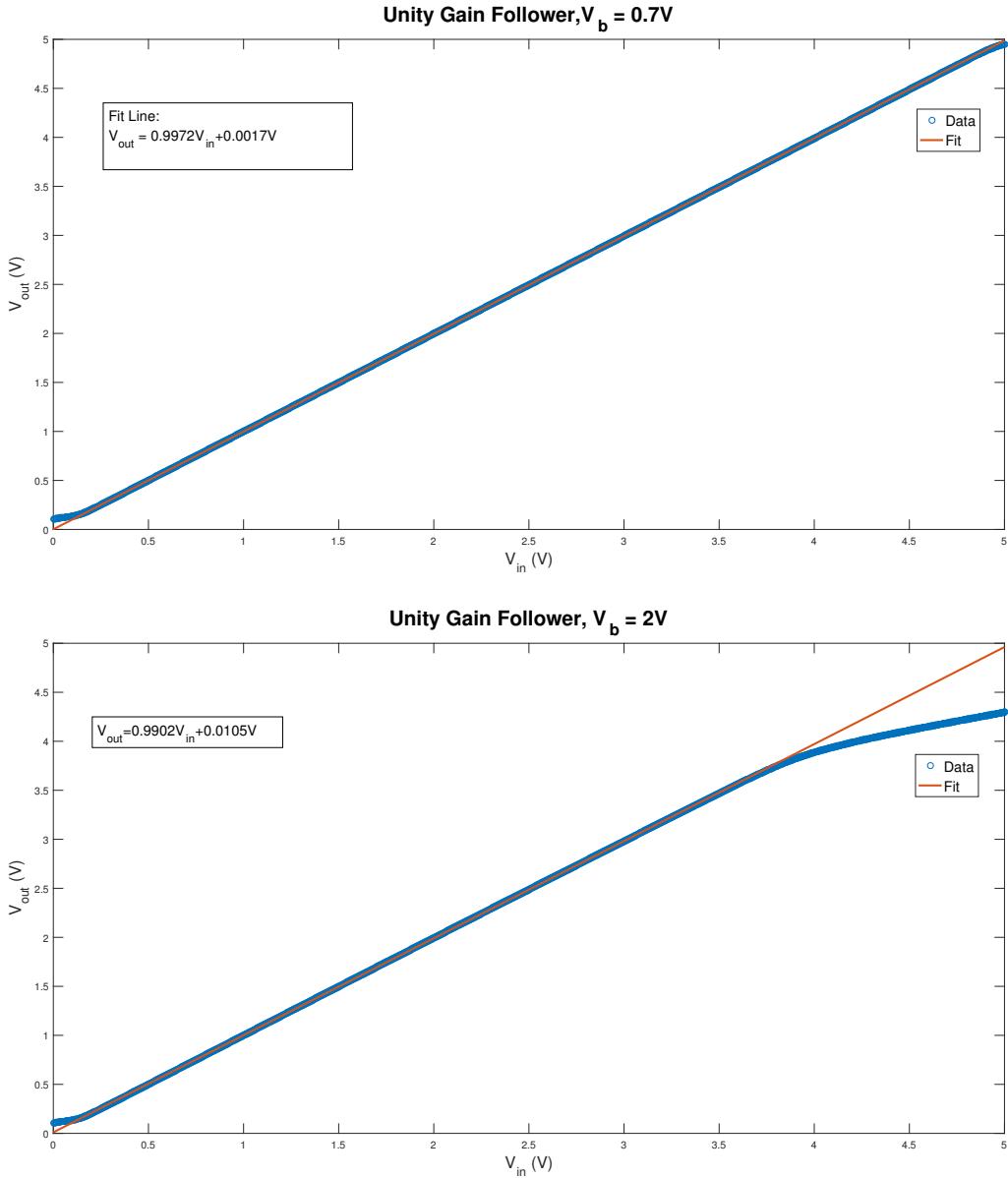


Figure 19: We tested the unity gain circuit in LTSpice using  $V_b = 0.7V$  (top) and  $V_b = 2V$  (bottom). Lower bias voltage resulted in the circuit having a unity gain for more values of  $V_{in}$ .

### Circuit 3

The final circuit we built and simulated is the circuit seen in figure 20, and as built on a breadboard in 21. We ran both the built circuit and the simulation on a rail to rail voltage supply of 5V. All tests on the built circuit had a bias voltage of approximately 0.7V.

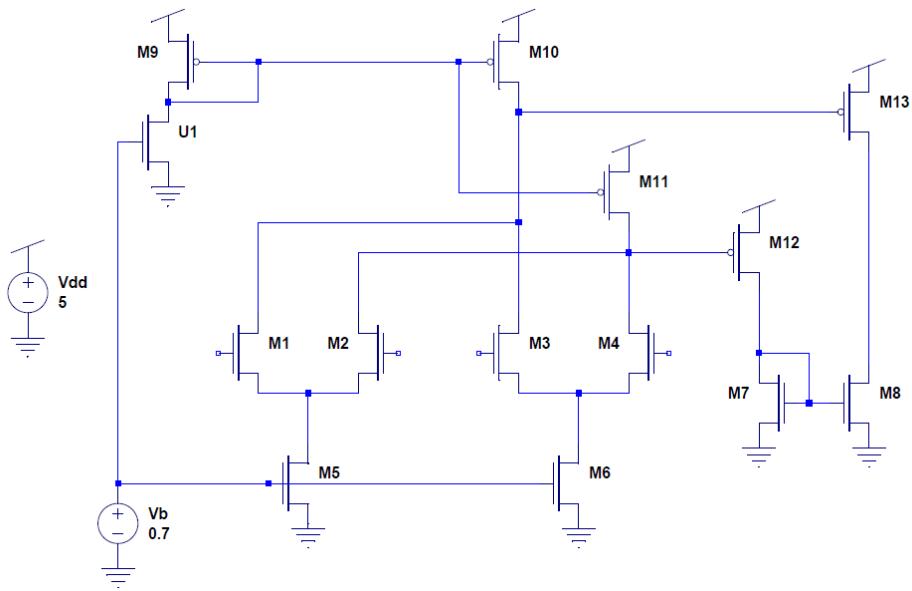


Figure 20: For this circuit, we first set  $V_b = 2V$  while building the circuit. We were unable to get data at this value - we eventually set  $V_b = 0.7V$  and conducted all of our experiments on the built circuit at this value.

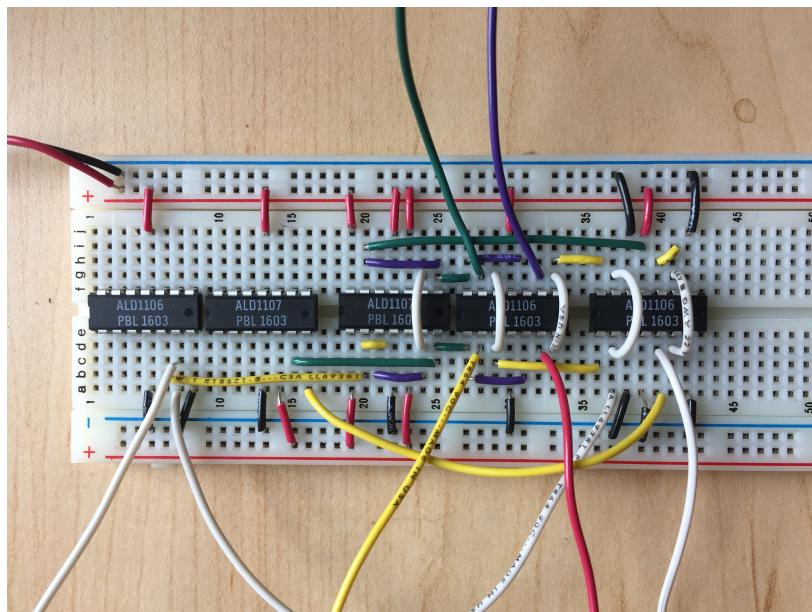


Figure 21: The circuit on a breadboard that we used for data collection.

### Circuit 3: Experiment 1

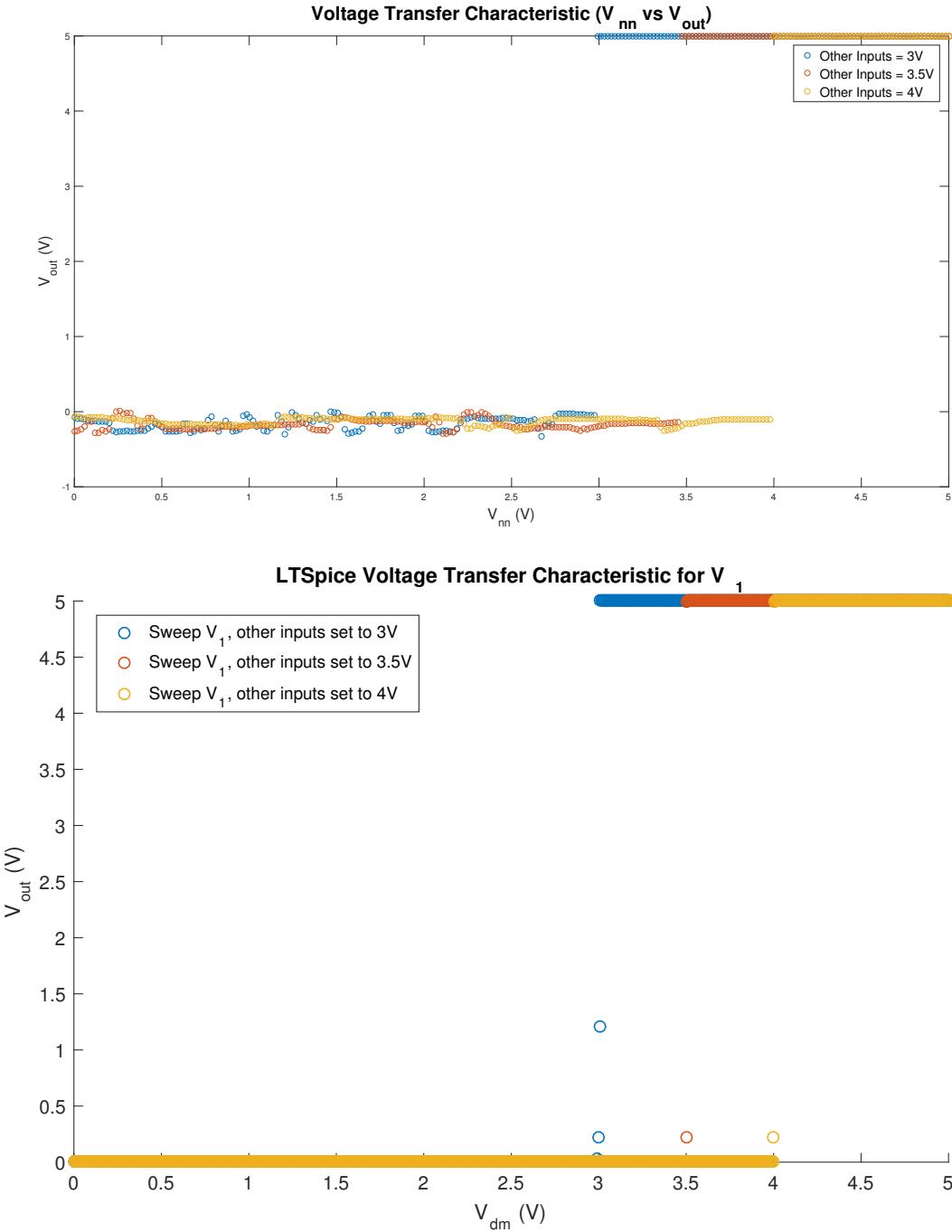


Figure 22: The voltage transfer characteristic of the circuit while sweeping a noninverting input from the built circuit (top) and the LTSpice simulation (bottom). The circuit has a very high gain, which both the built circuit and the simulation were able to capture.

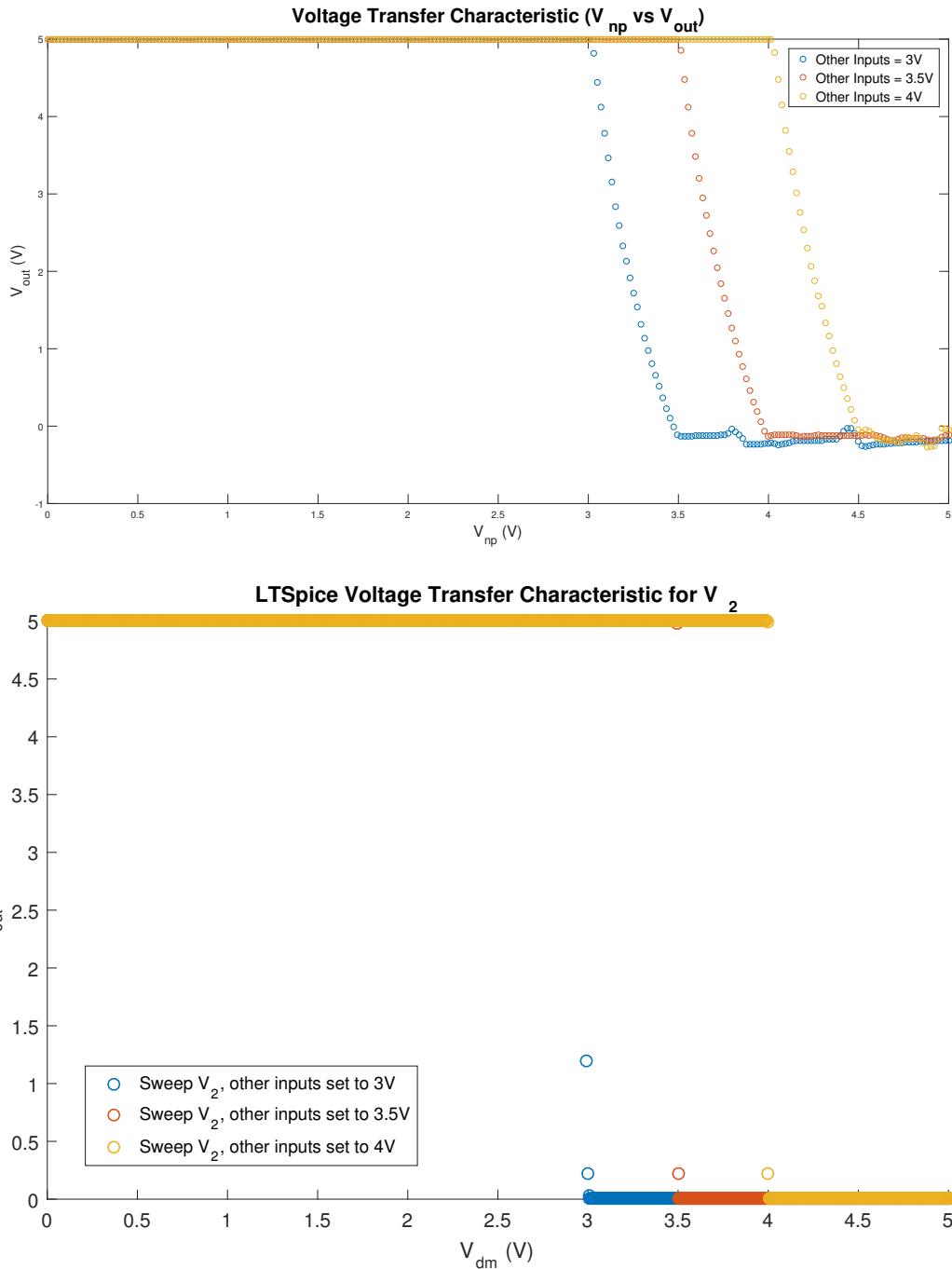


Figure 23: The voltage transfer characteristic of the circuit while sweeping an inverting input from the built circuit (top) and the LTSpice simulation (bottom). The built circuit shows a lower gain than it did in the noninverting case.

### Circuit 3: Experiment 2

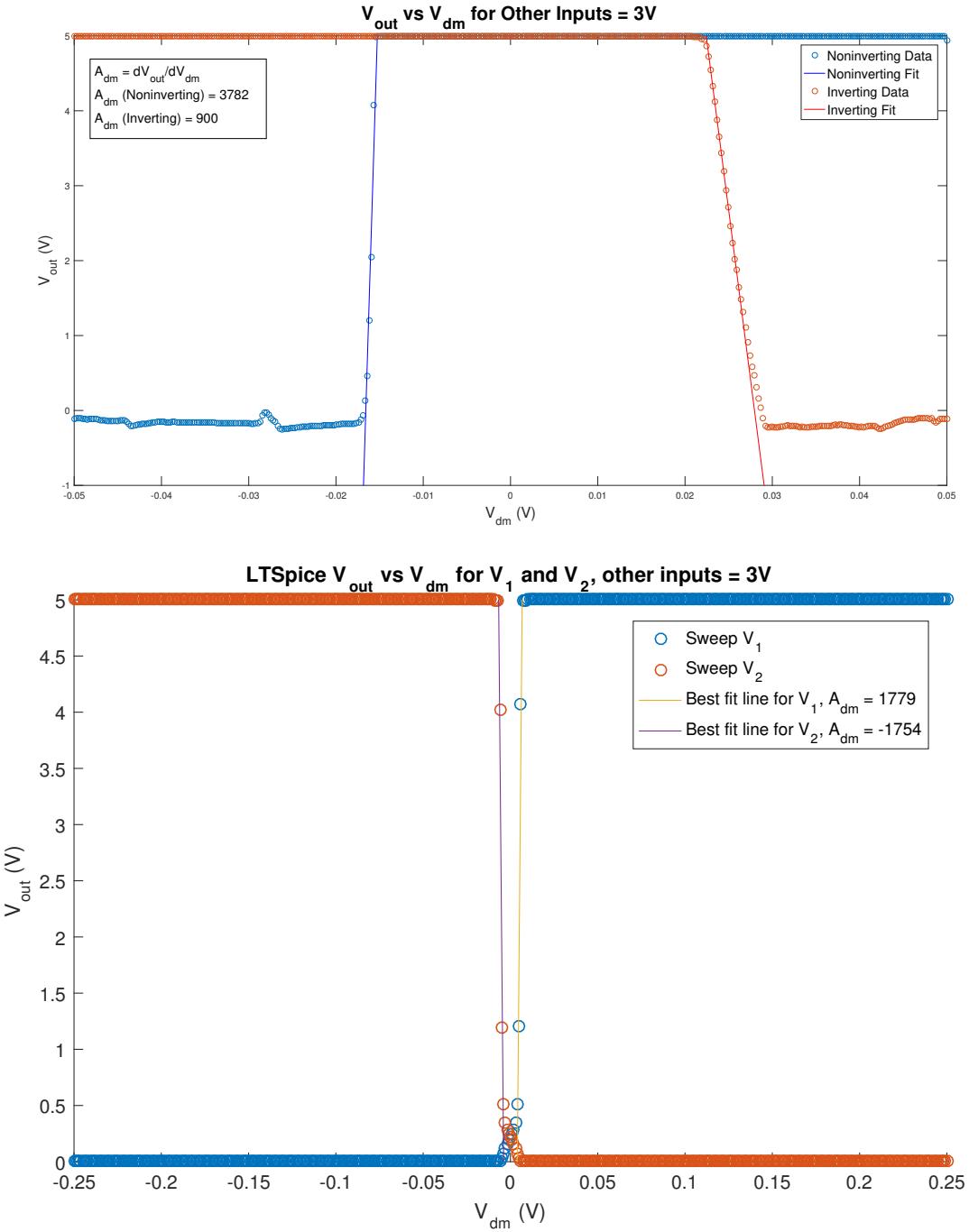


Figure 24: The differential mode voltage gain ( $A_{dm}$ ) was extracted from the built circuit (top) and the simulated circuit (bottom). The gains between these two datasets are quite different, and we observed much more consistent results in the simulation.

### Circuit 3: Experiment 3

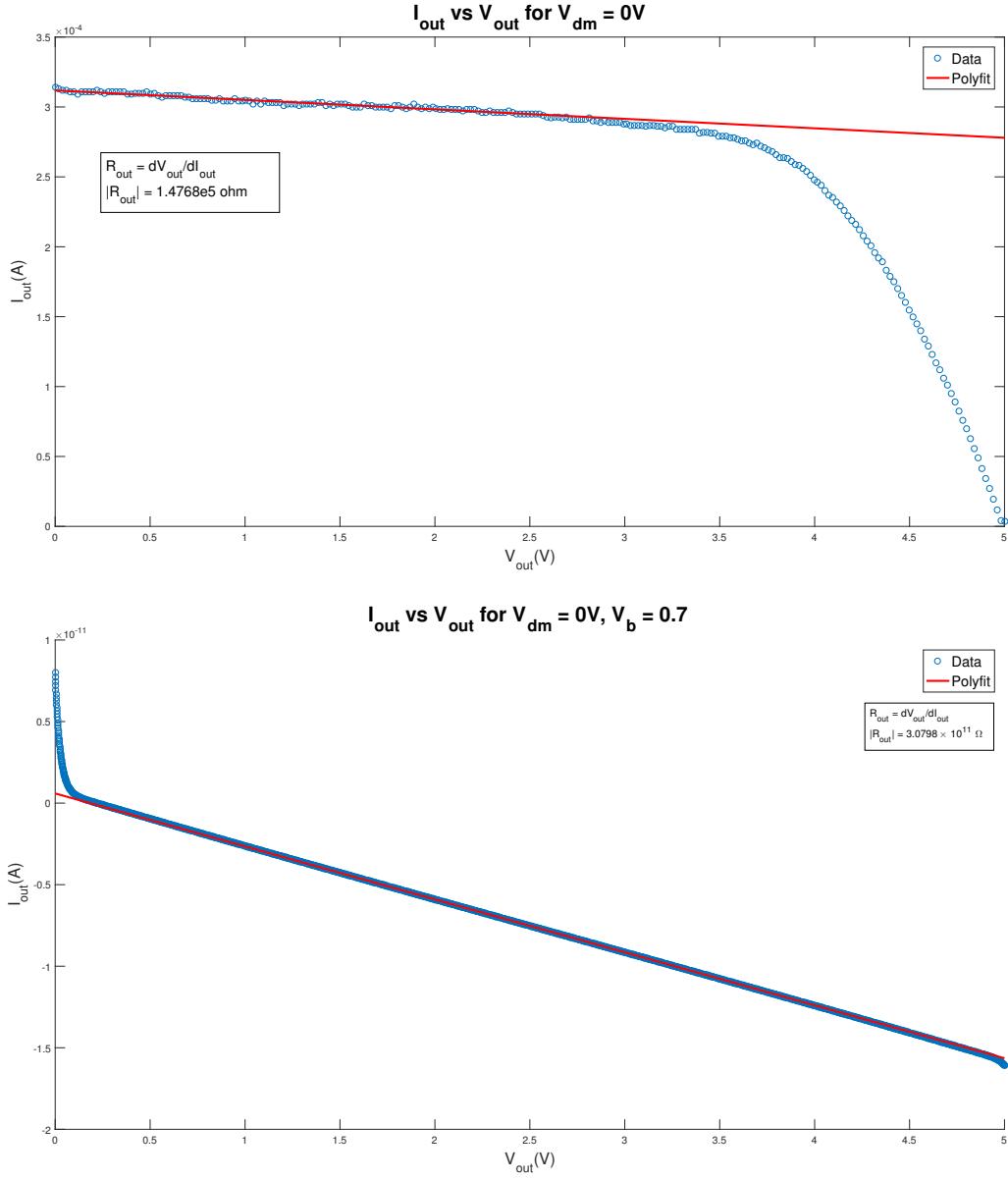


Figure 25: Collected circuit data (top) and simulated data (bottom) for experiment 3 when  $V_b = 0.7V$ . The current data we collected in the simulation was incredibly small, so we also simulated with  $V_b = 1.9V$ . This data can be seen in the next figure. The data we collected for  $V_b = 1.9V$  was much more reasonable and consistent with our experimentally measured circuit data, but for consistency in our final table we used the data for  $V_b = 0.7V$ .

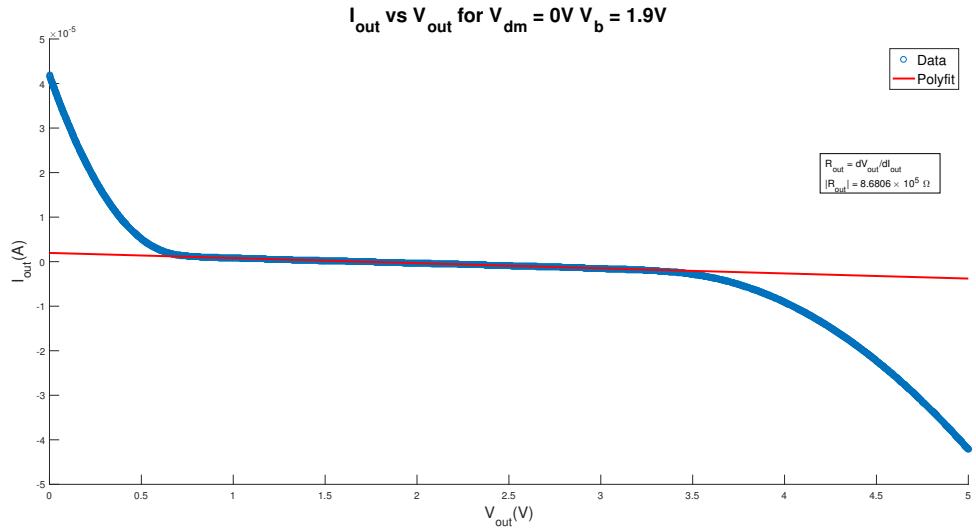


Figure 26: LTSpice simulated data for  $V_b = 1.9V$ .  $R_{out}$  for this simulation data is  $8.6806 \times 10^5 \Omega$ , which is closer to the circuit measured value.

### Circuit 3: Experiment 4

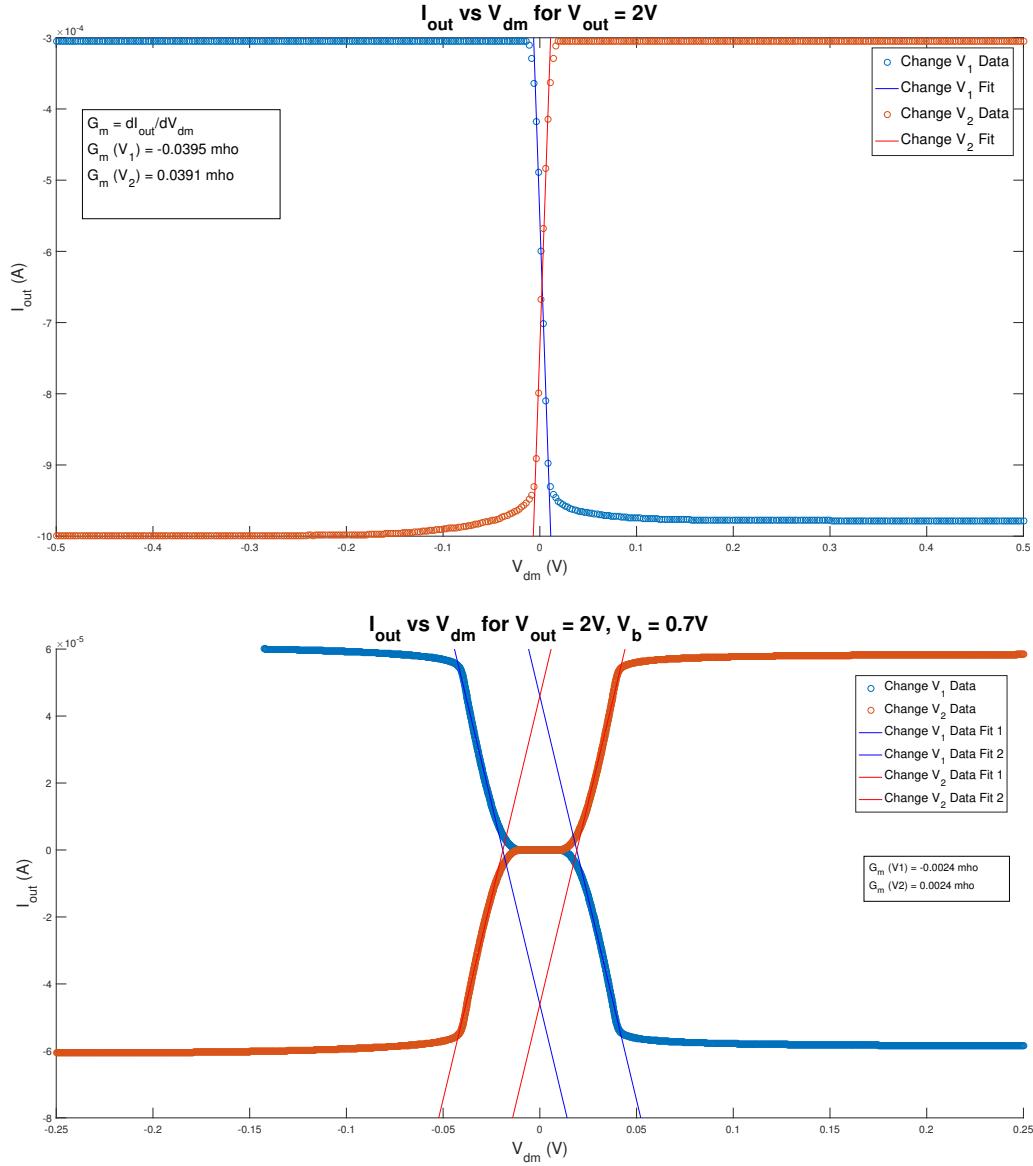


Figure 27: Transconductance gain,  $G_m$ , was extracted from the built circuit (top) and simulated circuit (bottom). As with experiment 3, we got strangely shaped data in the simulation for  $V_b = 0.7V$ . Because of this, we also collected simulation data for  $V_b = 1.9V$ . For consistency in our final table we used the data for  $V_b = 0.7V$ .

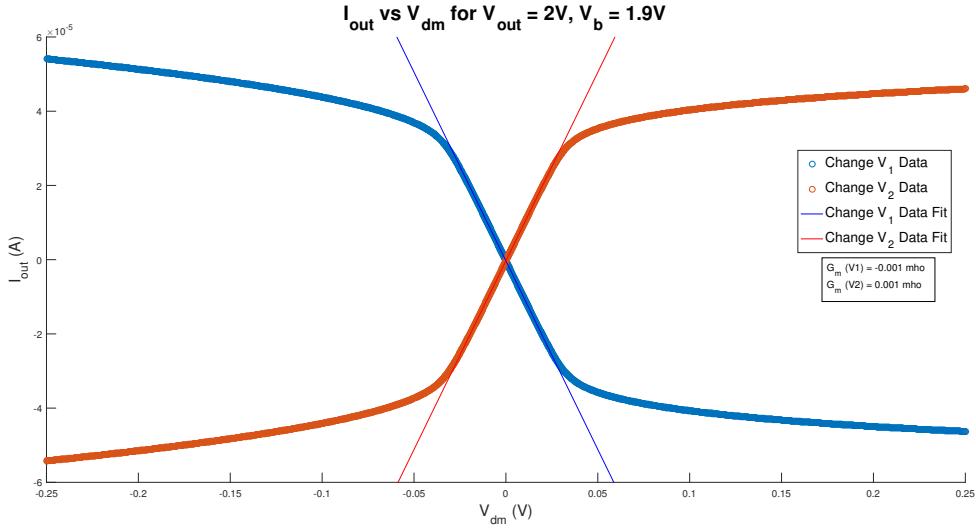


Figure 28: LTSpice simulated data for  $V_b = 1.9V$ .  $G_m$  for the simulation here is  $0.01\text{U}$ , which is closer to the circuit measured value.

As was said above,  $A_{dm} = G_m R_{out}$ . Using our extracted values, we calculated that the gain of the built circuit was 5803 and the gain of the simulated circuit was  $7.39 \times 10^8$ . However, using the values for  $G_m$  and  $R_{out}$  from the  $V_b = 1.9V$  simulation, we find that  $A_{dm} = 8681$ , which is more closely aligned with the extracted  $A_{dm}$  for the LTSpice simulation of the same voltages, as well as the extracted and calculated values of  $A_{dm}$  from the built circuit.

### Circuit 3: Experiment 5

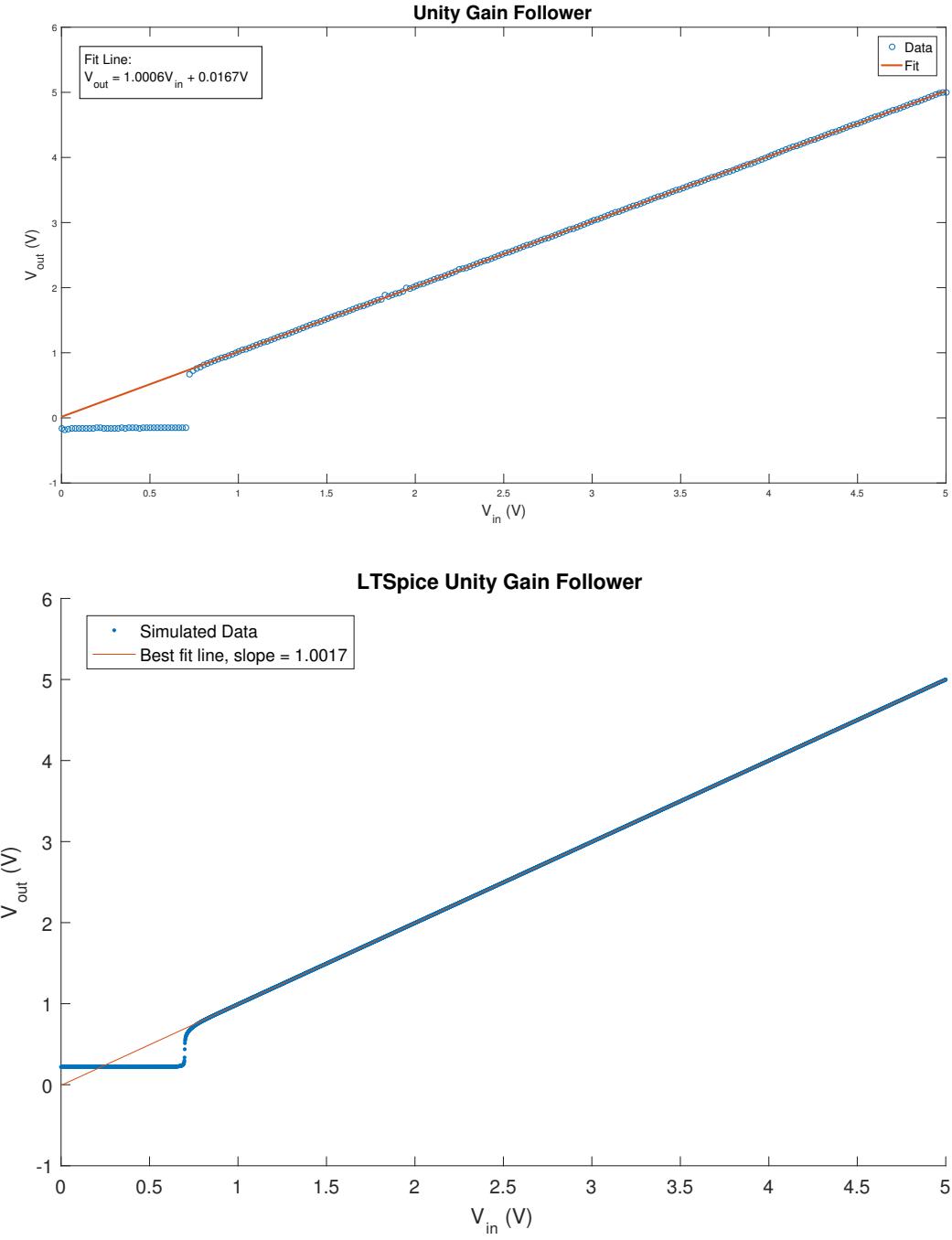


Figure 29: Unity-gain connected circuit for the built circuit (top) and simulation (bottom).

## 3 Results

We conducted and retrieved data from circuits 1 and 2 with  $V_b \approx 2V$ . When we collected data for circuit 3 (built), however, we could not get any readable signal with such a high  $V_b$ . Because of this,

	$A_{dm}$ (extracted)	$G_m$ ( $\text{V}$ )	$R_{out}$ ( $\Omega$ )	$A_{dm}$ (calculated)
<b>Circuit 1 Built</b>	594	.0060	$8.486 \times 10^4$	509.46
<b>Circuit 1 LTSpice</b>	27.25	$9.6417 \times 10^{-4}$	$2.671 \times 10^5$	257.54
<b>Circuit 2 Built</b>	18.43	$4.78 \times 10^{-4}$	$3.3437 \times 10^4$	15.9828
<b>Circuit 2 LTSpice</b>	18.565	$1.8896 \times 10^{-5}$	$4.9963 \times 10^5$	9.4408
<b>Circuit 3 Built</b>	2341	0.0393	$1.4768 \times 10^5$	5803
<b>Circuit 3 LTSpice</b>	1766.5	0.0024	$3.0798 \times 10^{11}$	$7.39 \times 10^8$

Table 1: The data we collected from the three circuits both built and simulated.

we collected all circuit 3 (built) data with  $V_b = 0.7\text{V}$ . We also performed circuit 3 (simulated) with  $V_b = 0.7\text{V}$  for consistency, but when we conducted experiment 3, we did not measure appreciable current. We redid experiment 3 with  $V_b = 1.9\text{V}$  and saw much larger currents (on the order of microamps, not picoamps). The data presented in table 1, therefore, were taken with two different bias voltages, and we are unsure if we can compare the values given because of this.

Given the information that we do have, we can confidently say that circuit 2 has a very low gain, while circuits 1 and 3 have much higher gains. We do see an inconsistency between  $A_{dm}$  (extracted) for circuit 1 built versus LTSpice that we cannot account for - perhaps we should have taken more points in the LTSpice simulation. For someone looking to use a DDA, we would caution against any of these. While circuit 2 was easy to build and worked well at  $V_b \approx 2\text{V}$ , it had the lowest gain of all three circuits. Circuit 1 has a high gain and works well at  $V_b \approx 2\text{V}$  as well, but it was much more difficult to construct. Circuit 3 has the highest gain, but functions the least consistently at  $V_b \approx 2\text{V}$ , but is also consistent at  $V_b = 0.7\text{V}$ . We are not satisfied with the  $R_{out}$  value extracted for circuit 3 in LTSpice. The measured current was very low, and we wonder if the very high  $R_{out}$  value is because there was no significant current flowing. However, we present it here for consistency.

## 4 Discussion

Differential difference amplifiers

Have many forms, of which we do not tire  
 Of the gate voltage inputs, there are four  
 Compared to an op-amp, that's many more!  
 We just wish our gains had been higher.

We were particularly surprised that with LTSpice  
 Our values did not align, they were not very nice  
 We think this has to do with math approximations  
 This made us sad, we felt many consternations  
 The data isn't perfect, but we hope our efforts suffice.

## References

- [1] Alzaher, Hussain, and Ismail, Mohammed. “A CMOS Fully Balanced Differential Difference Amplifier and Its Applications.” *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing* 48.6 (2001) 614-620. Print.

- [2] Sackinger, Eduard, and Walter Guggenbuhl. "A Versatile Building Block: The CMOS Differential Difference Amplifier." *IEEE Journal of Solid-State Circuits* SC-22.2 (1987): 287-94. Print.