

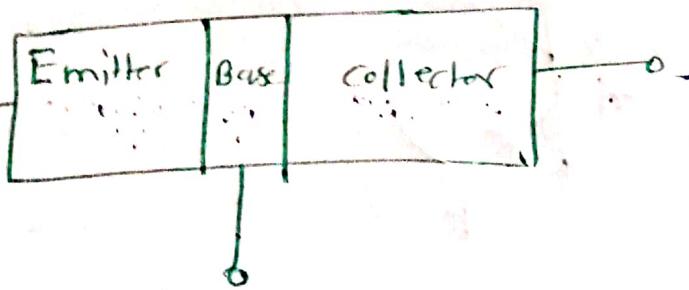
BJT

Bipolar Junction transistor → It has
Pn-Junctions
Both Electrons and holes participate in conduction

→ Low resistance & high resi.

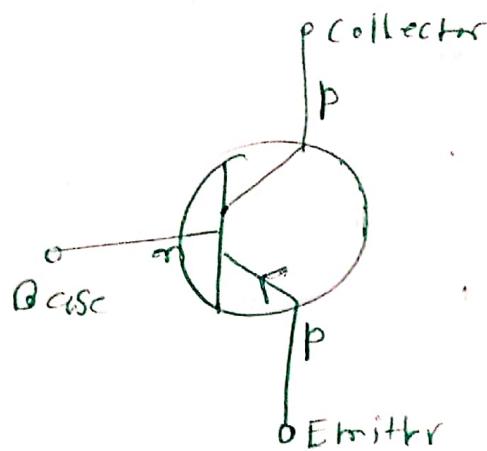
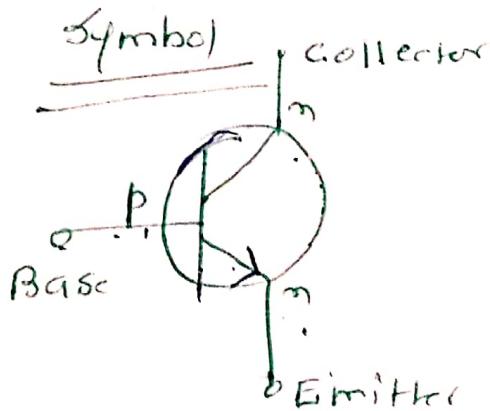
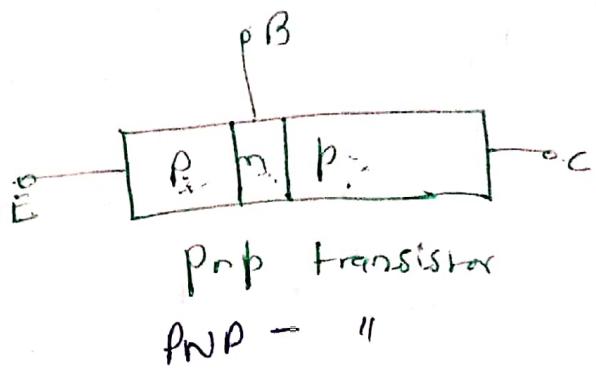
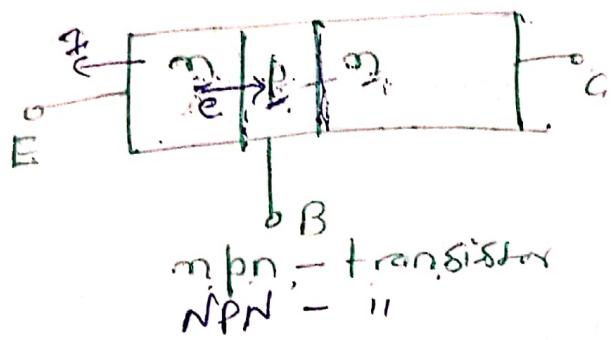
It transfers resistance.

It has three terminals:- Emitter, Base and Collector.



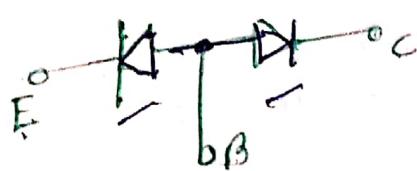
Region	Doping	Area	work/purpose
Emitter	Highly doped	Moderate	generates electrons
Base	lightly doped	thin	allows the electrons to pass through it
Collector	Moderately doped	thickest	collects electrons

Structure



m-p-n

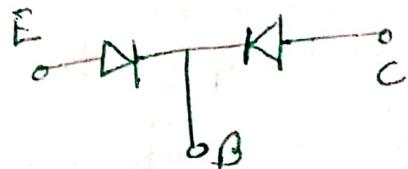
Two diode model



m-p-n

However this model is not true because of the following reason,

p-n-p

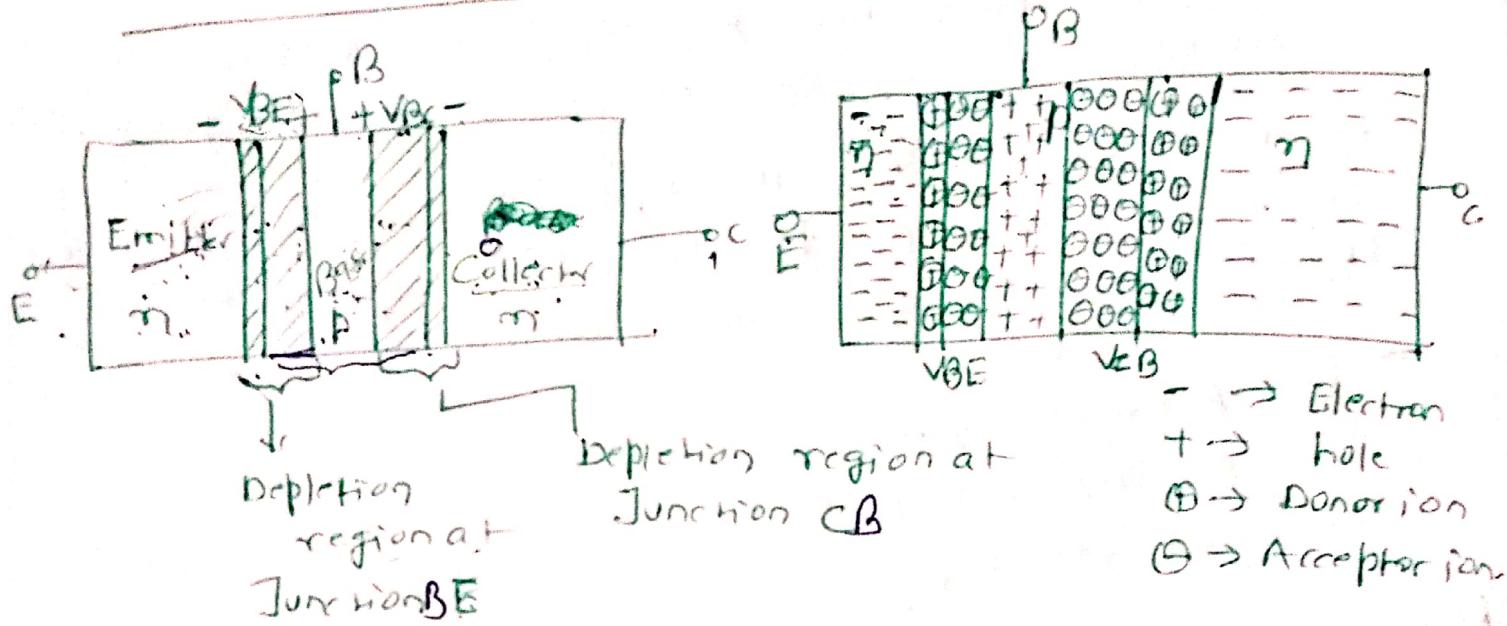


p-n-p

not true because of

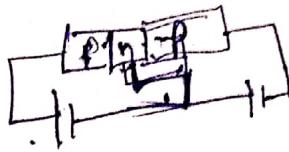
i) Relative doping of the regions must be different

ii) P-n junctions in transistor are interdependent where as in back to back connected diodes it is independent.

Unbiased transistor

- Emitter is highly doped region. In an n/pn transistor, the Emitter Base Junction is n/p type. Emitter has more no. of electrons in comparison to holes in base as base is lightly doped. So a depletion region will develop near Emitter Base Junction. Since Base is lightly doped, hence width of depletion region will be more in comparison to width in Emitter.
- similarly, near Base collector junction also, a depletion region will develop. The width of depletion region^{in base} will be more in comparison to width of depletion region in collector.

Biased transistor

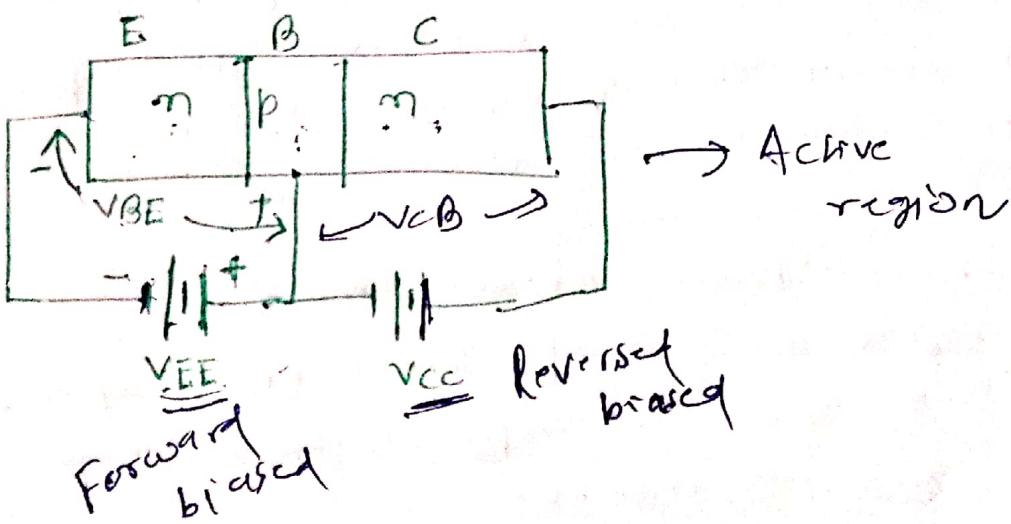


Since we have two junctions, two voltage sources are required to bias the junctions.

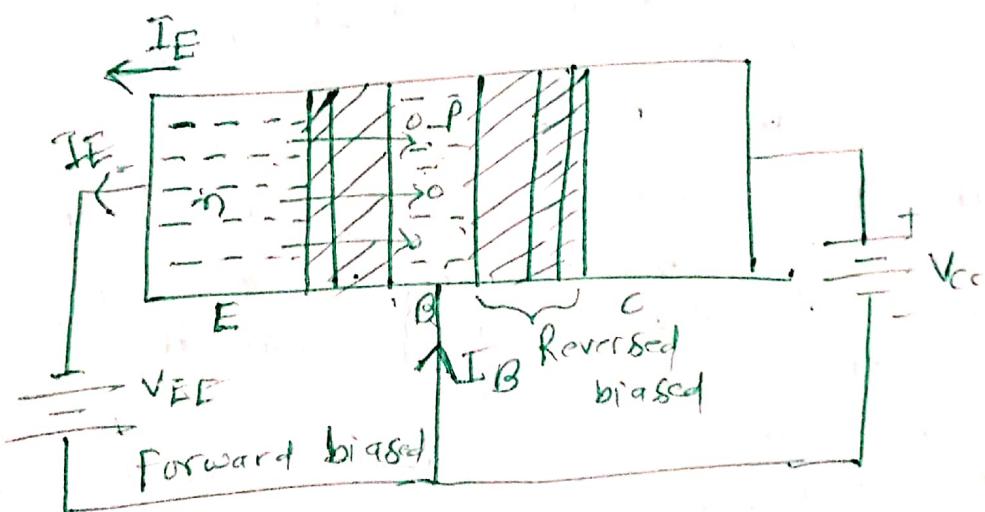
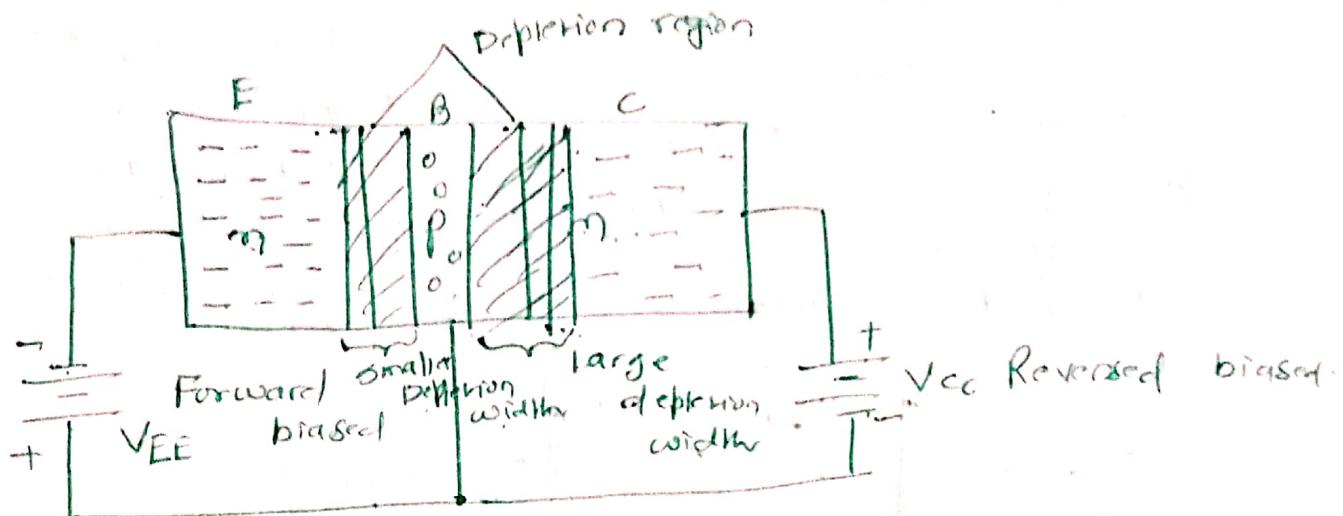
Depending on whether the two junctions are forward or reverse biased, the transistors operate in three regions which is summarized below.

- i) Active region
- ii) Saturation region
- iii) Cut off region

Region	Emitter-base Junction	Collector-base Junction	Application
Active	Forward biased	Reversed biased	As an amplifier
Cut-off	Reversed biased	Reversed biased	Switch(OFF)
Saturation	Forward biased	Forward biased	Switch(ON)



Operation of NPN transistor

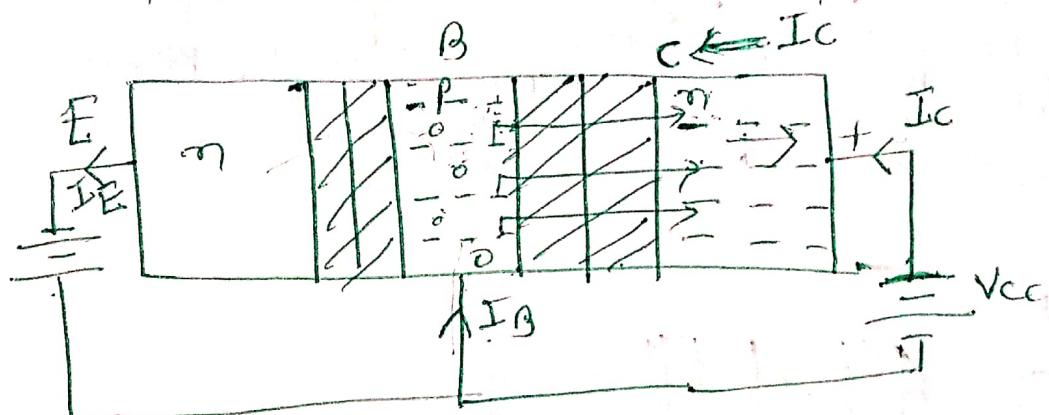


* Let us consider a npn transistor for our discussion. The base to emitter junction is forward biased and hence it has smaller depletion width. The base to collector junction is reverse biased and hence it will have larger depletion width.

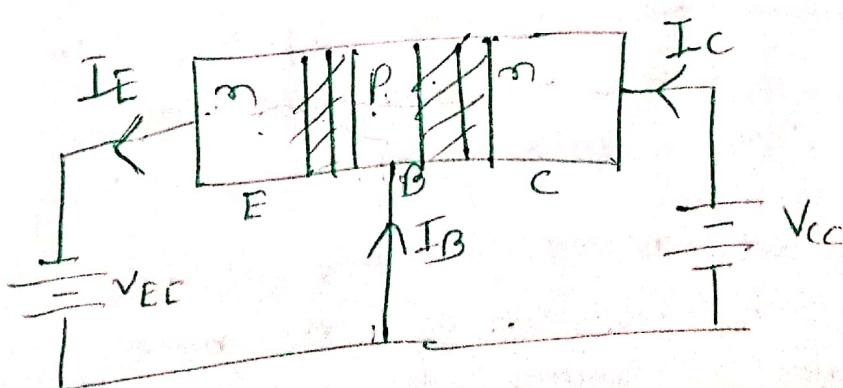
* Consider only forward biased junction at base-emitter. The negative terminal of the battery will force the electron in emitter to move towards Base.

* Since depletion region is narrow, electrons will move towards base. Base have very few holes hence few electrons will combine with it.

At positive terminal of the battery V_{EE} will attract minority electrons from base and hence it will constitute base current I_B . Since electrons will be moving away from base, the direction of base current will be towards base. Since no. of doping is smaller in base, base current will be very small.



Consider the base collector junction node. The electrons which moved from emitter to base are now attracted by +ve terminal of the battery V_{CC} . This electron will move towards the collector and it will constitute collector current. The direction of collector will be opposite to the direction of movement of electron, hence it will be from collector towards base.

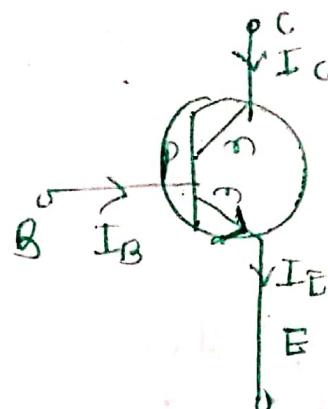
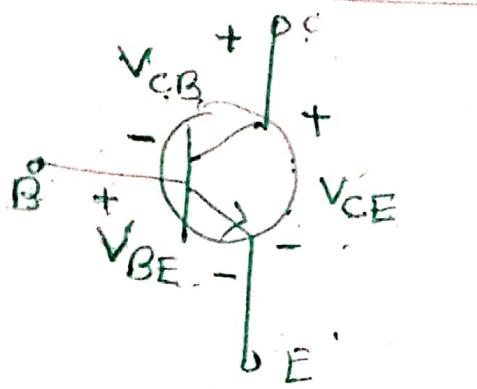


$$I_E = I_B + I_C$$

$$I_B \ll I_C$$

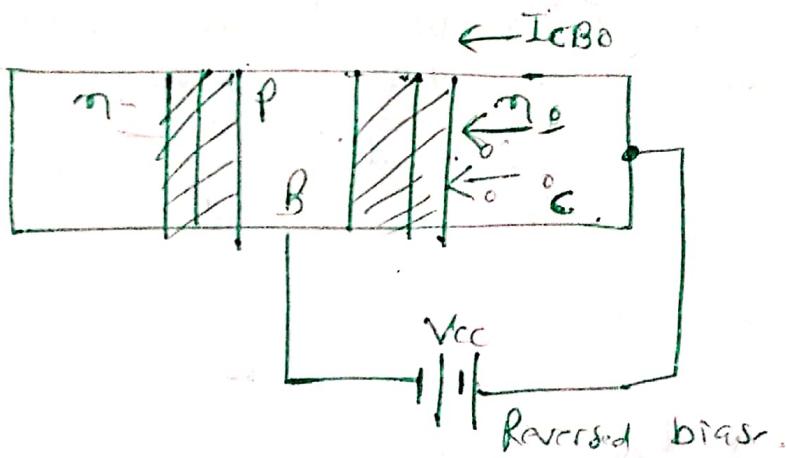
$$I_E \approx I_C$$

Transistor voltages and current



$$I_E = I_B + I_C$$

I_{CBO} (Reverse saturation current at collector-base junction).



Since collector-base junction is reversed biased, minority charge carriers of collector which are holes will move towards base and constitute of reverse saturation current. This is denoted by I_{CBO} . Hence, collector current which is flowing is due to two component

- Electrons which is moving from emitter to collector
- Minority charge carriers in collector which constitute reverse saturation current.

Definition of α and β

α (Alpha) :- It is defined as ratio of collector current to emitter current.

$$\alpha = \frac{I_C}{I_E}$$

$$I_E = I_B + I_C$$



$$I_E \approx I_C \quad \text{very small}$$

$$\alpha = \frac{I_C}{I_E} \approx 1$$

β (Beta) :- It is defined as ratio of collector current to base current.

$$\beta = \frac{I_C}{I_B} \quad \because I_B \ll I_C, \boxed{\beta \gg 1} \quad \beta \approx 100$$

Relation b/w α and β

$$I_E = I_C + I_B$$

divide both sides by I_C .

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\because \frac{I_C}{I_E} = \alpha, \quad \frac{I_E}{I_C} = \frac{1}{\alpha}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \frac{1}{\beta} = \frac{1}{\alpha} - 1$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\frac{1}{\beta} = \frac{1-\alpha}{\alpha}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

1. BIPOLAR JUNCTION TRANSISTOR

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an *npn transistor*, while the latter is called a *pnp transistor*. Both are shown in Fig. 1 with the proper dc biasing. The dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector moderately doped. The outer layers have widths much greater than the sandwiched *p*- or *n*-type material.

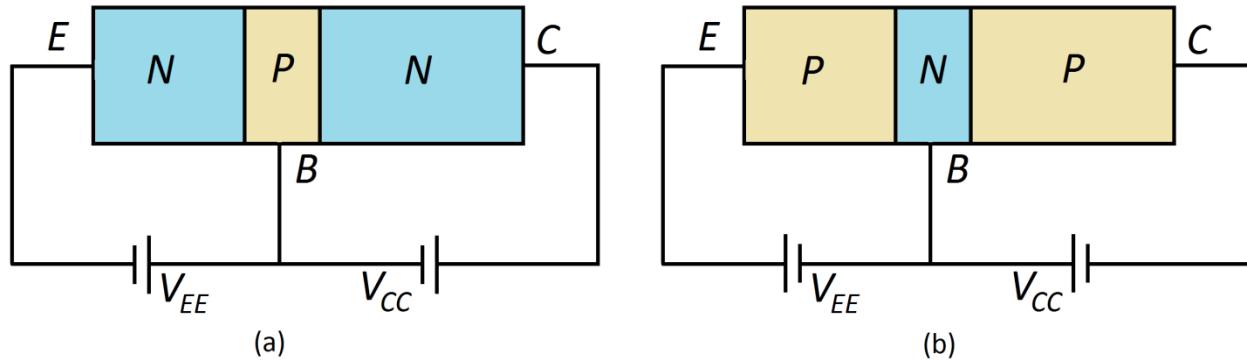


Figure 1. Types of Transistors (a) NPN (b) PNP

The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10:1 or less). These lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of “free” carriers. For the biasing shown in Fig. 1 the terminals have been indicated by the capital letters *E* for *emitter*, *C* for *collector*, and *B* for *base*. An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from *bipolar junction transistor*, is often applied to this three terminal device. The term *bipolar* reflects the fact that holes *and* electrons participate in the injection process into the oppositely polarized material.

1.1. TRANSISTOR OPERATION

The basic operation of the transistor will now be described using the *pnp* transistor as shown in Fig. 2.b. The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 2.a the *pnp* transistor has been redrawn without the base-to-collector bias. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p*- to the *n*-type material. Let us now remove the base-to-emitter bias of the *pnp* transistor as shown in Fig. 2.b. The flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 2.b. Therefore, one p-n junction of a transistor is reverse biased, while the other is forward biased.

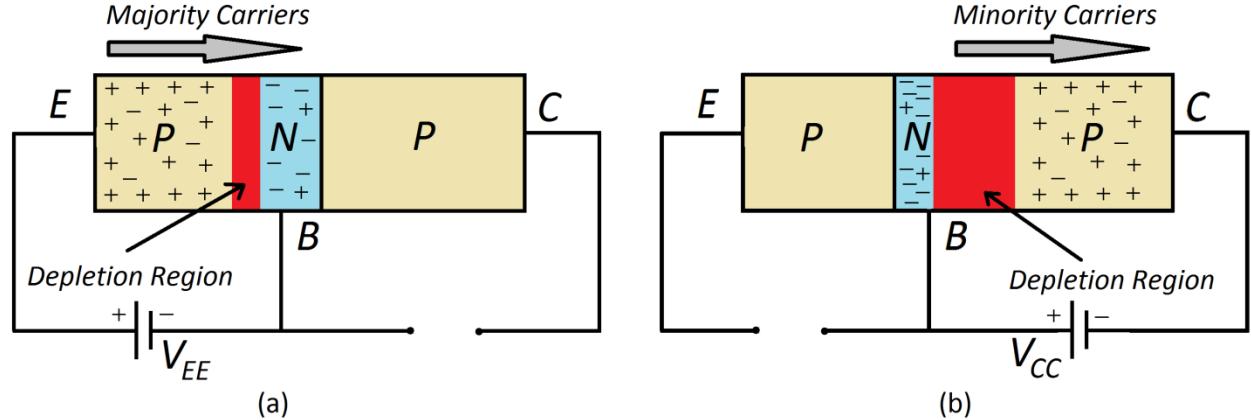


Figure 2. Biasing of a PNP Transistor (a) When collector is open (b) When emitter is open

In Fig. 3 both biasing potentials have been applied to a *pnp* transistor, with the resulting majority and minority carrier flow indicated. In Fig. 3 the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. 3, a large number of majority carriers will diffuse across the forward-biased *p-n* junction into the *n*-type material. The question then is whether these carriers will contribute directly to the base current I_B or pass directly into the *p*-type material. Since the sandwiched *n*-type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of microamperes as compared to milliamperes for the emitter and collector currents. The larger number of these majority carriers will diffuse across the reverse-biased junction into the *p*-type material connected to the collector terminal as indicated in Fig. 3. The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the *n*-type material. In other words, there has been an *injection* of minority carriers into the *n*-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 3.

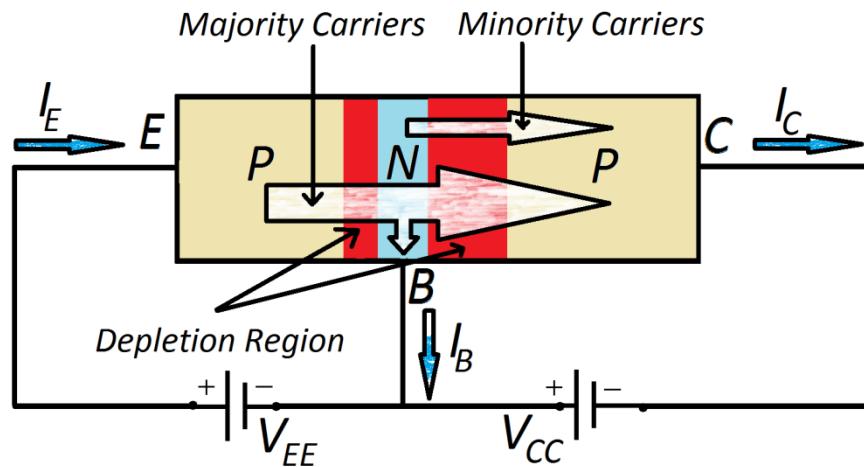


Figure 3. Majority and minority carrier flow of a PNP transistor

Applying Kirchhoff's current law to the transistor of Fig. 3 as if it were a single node, we obtain

$$I_E = I_C + I_B \quad (1.1)$$

and find that the emitter current is the sum of the collector and base currents. The collector current, however, is comprised of two components—the majority and minority carriers as indicated in Fig. 3. The minority current component is called the *leakage current* and is given the symbol I_{CO} (I_C current with emitter terminal Open).

The collector current, therefore, is determined in total by Eq. (1.2).

$$I_C = I_{C\text{majority}} + I_{CO\text{minority}} \quad (1.2)$$

For general-purpose transistors, I_C is measured in milliamperes, while I_{CO} is measured in microamperes or nanoamperes. I_{CO} , like I_s for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO} , to the point where its effect can often be ignored.

1.2. COMMON-BASE CONFIGURATION

The notation and symbols used in conjunction with the transistor in the majority of texts and manuals published today are indicated in Fig. 4 for the common-base configuration with *pnp* and *npn* transistors. The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential. The arrow in the diode symbol defined the direction of conduction for conventional current. For the transistor, the arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.

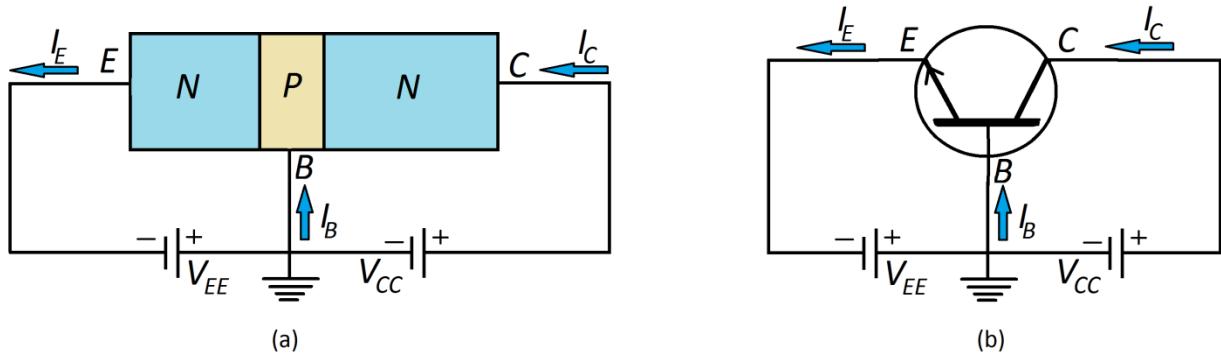


Figure 4. Notations and symbols of common base configuration

All the current directions appearing in Fig. 4 are the actual directions as defined by the choice of conventional flow. Note in each case that $I_E = I_C + I_B$. Note also that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch. That is, compare the direction of I_E to the polarity or V_{EE} for each configuration and the direction of I_C to the polarity of V_{CC} . To fully describe the behavior of a three-terminal device such as the common-base amplifiers of Fig. 4 requires two sets of characteristics—one for the *driving point* or *input* parameters and the other for the *output* side. The input set for the common-base

amplifier as shown in Fig. 5(a) will relate an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}). The output set will relate an output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E) as shown in Fig. 5(b). The output or *collector* set of characteristics has three basic regions of interest, as indicated in Fig. 5(b): the *active*, *cutoff*, and *saturation* regions. The active region is the region normally employed for linear (undistorted) amplifiers. ***In the active region the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.***

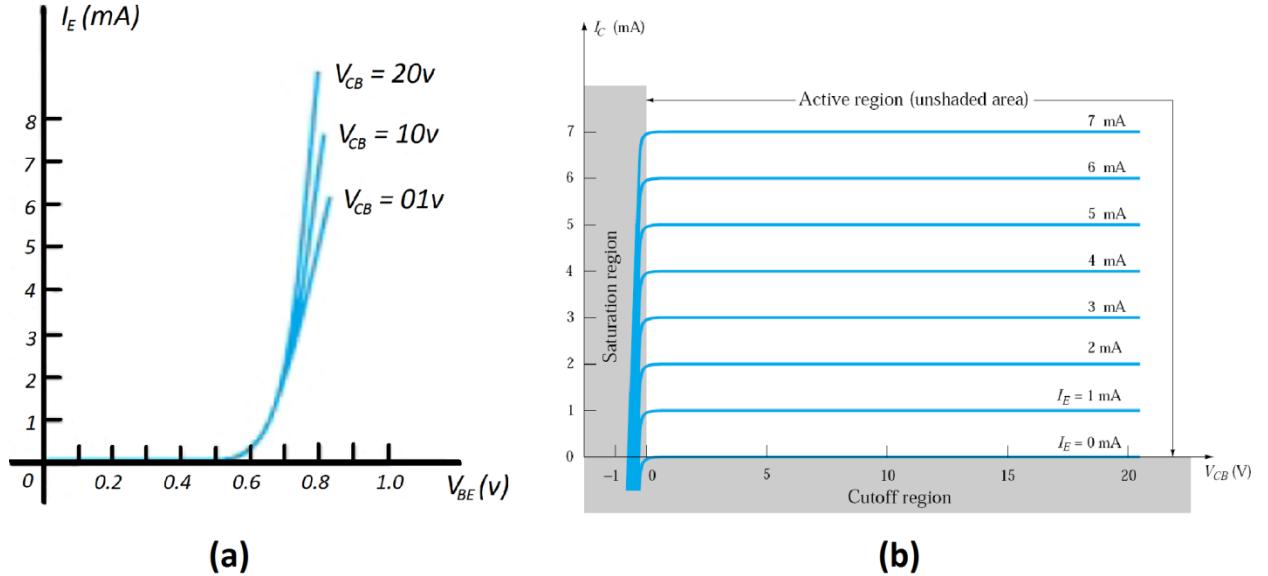


Figure 5. Characteristics for a common base configuration (a) Input characteristics, (b) Output characteristics

The active region is defined by the biasing arrangements of Fig. 4. At the lower end of the active region the emitter current (I_E) is zero, the collector current is simply that due to the reverse saturation current I_{CO} , as indicated in Fig. 5(b). The current I_{CO} is so small (microamperes) in magnitude compared to the vertical scale of I_C (milliamperes) that it appears on virtually the same horizontal line as $I_C = 0$. In addition, keep in mind that I_{CBO} , like I_s , for the diode (both reverse leakage currents) is temperature sensitive. At higher temperatures the effect of I_{CBO} may become an important factor since it increases so rapidly with temperature. Note in Fig. 5(b) that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also the almost negligible effect of V_{CB} on the collector current for the active region. The curves clearly indicate that *a first approximation to the relationship between I_E and I_C in the active region is given by*

$$I_C \approx I_E \quad (1.3)$$

As inferred by its name, the cutoff region is defined as that region where the collector current is 0 A, as revealed on Fig. 5(b). ***In the cutoff region the collector-base and base-emitter junctions of a transistor are both reverse-biased.***

The saturation region is defined as that region of the characteristics to the left of $V_{CB} = 0$ V. The horizontal scale in this region was expanded to clearly show the dramatic change in characteristics in this region. Note the exponential increase in collector current as the voltage V_{CB} increases toward 0 V. ***In the saturation region the collector-base and base-emitter junctions are forward-biased.***

1.2.1 ALFA (α)

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E} \quad (1.4)$$

where I_C and I_E are the levels of current at the point of operation. Even though the characteristics of Fig. 5(b) would suggest that $\alpha = 1$, for practical devices the level of alpha typically extends from 0.90 to 0.998, with most approaching the high end of the range. Since alpha is defined solely for the majority carriers, Eq. (1.2) becomes

$$I_C = \alpha I_E + I_{CBO} \quad (1.5)$$

For the characteristics of Fig. 5(b) when $I_E = 0$ mA, I_C is therefore equal to I_{CBO} , but as mentioned earlier, the level of I_{CBO} is usually so small that it is virtually undetectable on the graph of Fig. 5(b). In other words, when $I_E = 0$ mA, I_C also appears to be 0 mA for the range of V_{CB} values.

For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by

$$\alpha_{ac} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB} = \text{const.}} \quad (1.6)$$

The ac alpha is formally called the *common-base, short-circuit, amplification factor*. Eq. (1.6) specifies that a relatively small change in collector current is divided by the corresponding change in I_E with the collector-to-base voltage held constant. For most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for the other.

1.3. COMMON-EMITTER CONFIGURATION

The most frequently encountered transistor configuration appears in Fig. 6 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base-emitter* circuit and one for the *output* or *collector-emitter* circuit. Both are shown in Fig. 7(a) and (b).

The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is,

$$I_E = I_C + I_B$$

and

$$I_C = \alpha I_E.$$

For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

Note that on the characteristics of Fig. 7 the magnitude of I_B is in microamperes, compared to milliamperes of I_C . Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

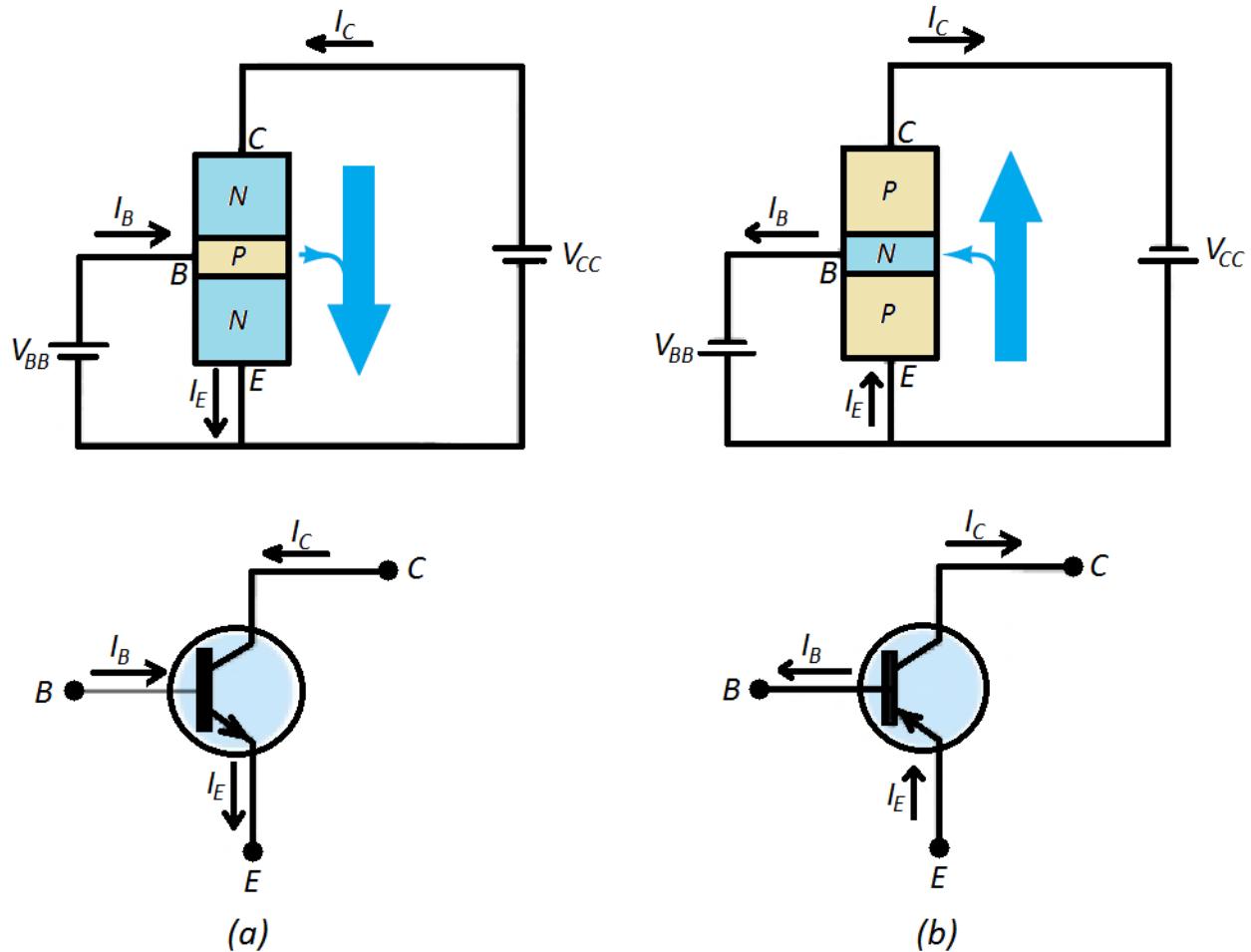


Figure 6. Notations and symbols of common emitter configuration (a) NPN transistor (b) PNP transistor

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. In Fig. 7(b) this region exists to the right of the vertical dashed line at V_{CEsat} and above the curve for I_B equal to zero. The region to the left of V_{CEsat} is called the saturation region. ***In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.***

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

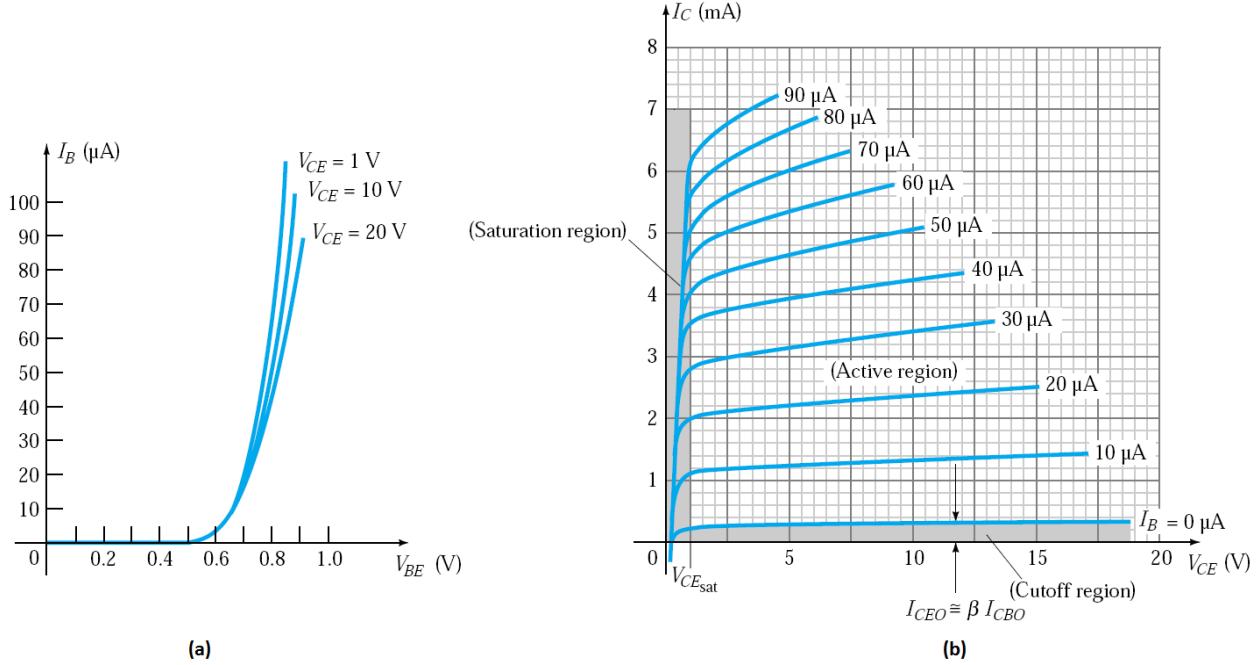


Figure 7. Characteristics for a common emitter configuration (a) Input characteristics, (a) Output characteristics

1.3.1 BETA (β)

In the dc mode the levels of I_C and I_B are related by a quantity called *beta* and defined by the following equation:

$$\beta_{dc} = \frac{I_C}{I_B} \quad (1.7)$$

where I_C and I_B are determined at a particular operating point on the characteristics. For practical devices the level is typically ranges from about 50 to over 400, with most in the midrange. For a device with a β of 200, the collector current is 200 times the magnitude of the base current.

For ac situations an ac beta has been defined as follows:

$$\beta_{ac} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE} = \text{const.}} \quad (1.8)$$

The formal name for β_{ac} is *common-emitter, forward-current, and amplification factor*. Since the collector current is usually the output current for a common-emitter configuration and the base current the input current, the term *amplification* is included in the nomenclature above.

Beta is a particularly important parameter because it provides a direct link between current levels of the input and output circuits for a common-emitter configuration. That is,

$$I_C = \beta I_B \quad (1.9)$$

and since

$$I_E = I_C + I_B$$

$$I_E = \beta I_B + I_B$$

we have

$$I_E = (\beta + 1)I_B \quad (1.10)$$

Both of the equations above play a major role in the analysis of BJT.

1.3. RELATION BETWEEN α AND β

A relationship can be developed between α and β using the basic relationships introduced thus far. Using $\beta = I_C/I_B$ we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

From equation (1.4)

$$\begin{aligned} \alpha &= \frac{I_C}{I_E} \\ I_E &= \frac{I_C}{\alpha} \end{aligned} \quad (1.11)$$

From equation (1.7)

$$\begin{aligned} \beta &= \frac{I_C}{I_B} \\ I_B &= \frac{I_C}{\beta} \end{aligned} \quad (1.12)$$

we know that

$$I_E = I_C + I_B \quad (1.13)$$

by putting equation (1.11) and (1.12) in to (1.13) we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by I_C will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{\beta + 1}{\beta}$$

$$\beta = (\beta + 1)\alpha$$

so that

$$\alpha = \frac{\beta}{1+\beta} \quad (1.14a)$$

$$\beta = \frac{\alpha}{1-\alpha} \quad (1.14b)$$

1.4. COMMON-COLLECTOR CONFIGURATION

The third and final transistor configuration is the *common-collector configuration*, shown in Fig. 8 with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{EC} for a range of values of I_B . The input current, therefore, is the same for both the common-emitter and common collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \approx 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

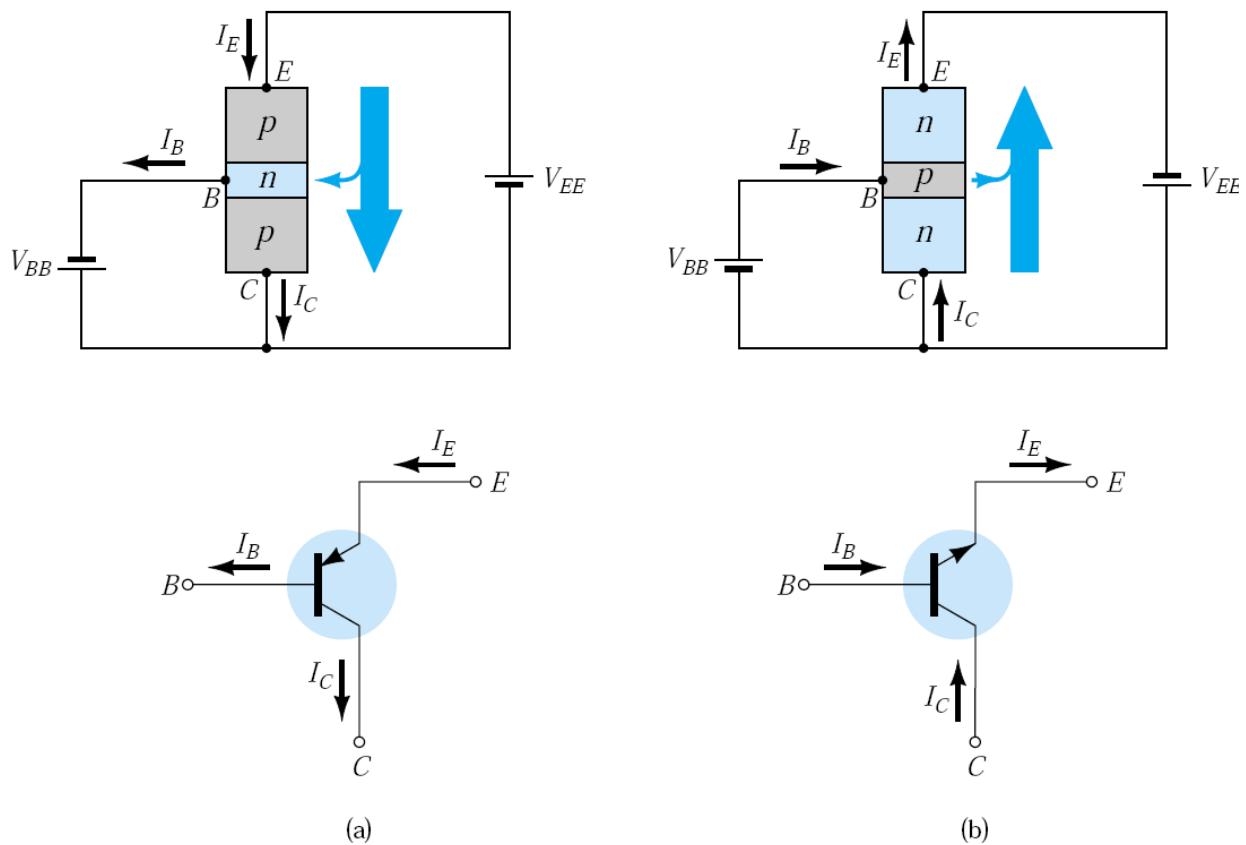
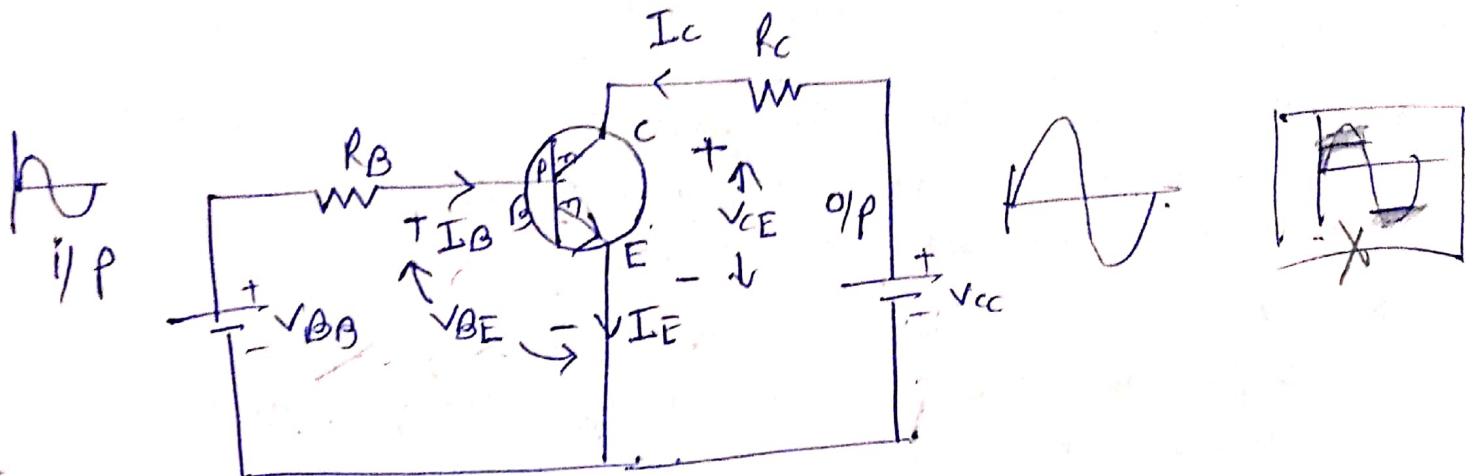


Figure 8. Notations and symbols of common collector configuration (a) PNP transistor (b) NPN transistor

DC Load Line

- * When we use transistor as an amplifier it requires the knowledge of DC and AC response of the system.
 - * AC and DC analysis can be done separately, but choices of DC parameter affects the AC analysis and vice versa.
 - * After that we can construct a network which tells you about a desired operating point. This type of analysis requires biasing.
- Biasing:-** Biasing is defined as application of external DC voltage to select an appropriate operating point. These networks are known as biasing networks.
- * Transistors are operated in Active region to work as amplifiers. So we have to apply DC biasing in such a way that operating points of transistors should remain in active region.
 - * For this particular analysis throughout the discussion we will use NPN common emitter transistor.
 - * CE has high current amplification.



We need to amplify the weak signal faithfully, means without distortion. O/p signal should not have any parts clipped.

Operating points:-

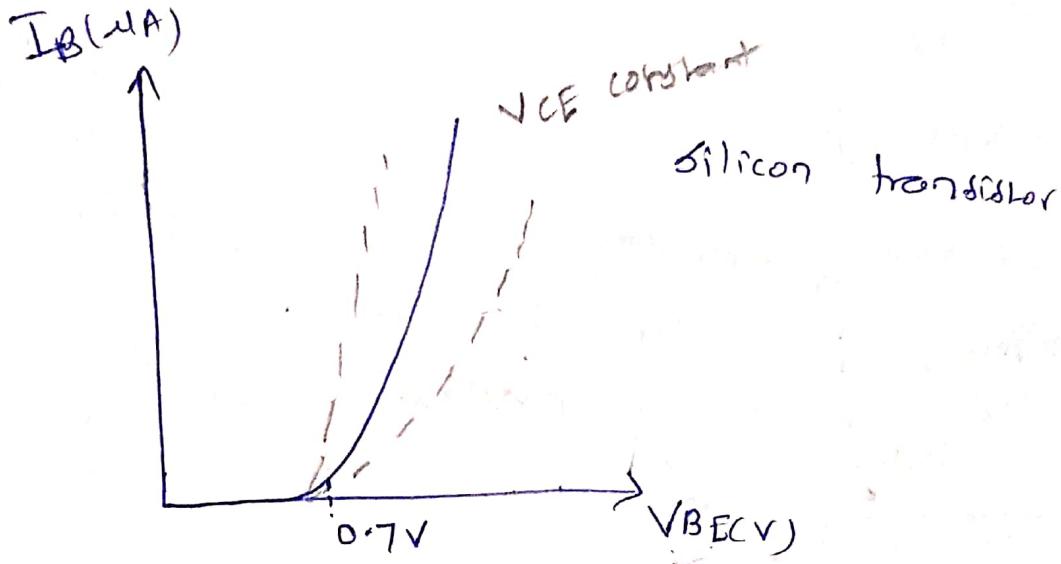
Transistors have two ~~op~~ ports, so it has two types of operating point. Those are i/p and o/p operating points.

⑧

I/p operating point:-

It is defined as the coordinates obtained by intersection of ~~the~~ load line with transistor I/p characteristics for a particular value of o/p voltage (V_{ce}).

We have to apply KVL in i/p loop. We also have to draw i/p characteristics of a CE transistor.



If we apply KVL in the i/p loop of previous circuit, then we will have

$$V_{BB} - I_B R_B - V_{BE} = 0 \quad \text{--- (1)}$$

If you look at the i/p characteristics curve, we have V_{BE} as x -axis and I_B as y -axis. So we have to write a straight line equation $y = mx + c$ using equation (1),

$$I_B R_B = V_{BB} - V_{BE}$$

$$I_B = \frac{V_{BB}}{R_B} - \frac{V_{BE}}{R_B} \quad \text{--- (2)}$$

$$I_B = -\frac{V_{BE}}{R_B} + \frac{V_{BB}}{R_B}$$

$$y = -mx + c$$

$$m = -\frac{1}{R_B}$$

$$c = \frac{V_{BB}}{R_B}$$

Let us consider two points to draw the load line.

$$P_1(0, y_1), P_2(x_2, 0)$$

To find P_1

$$\frac{x=0, \text{ using eq. (1)}}{V_{BE}=0}$$

$$I_B = \frac{V_{BB}}{R_B} = y_1$$

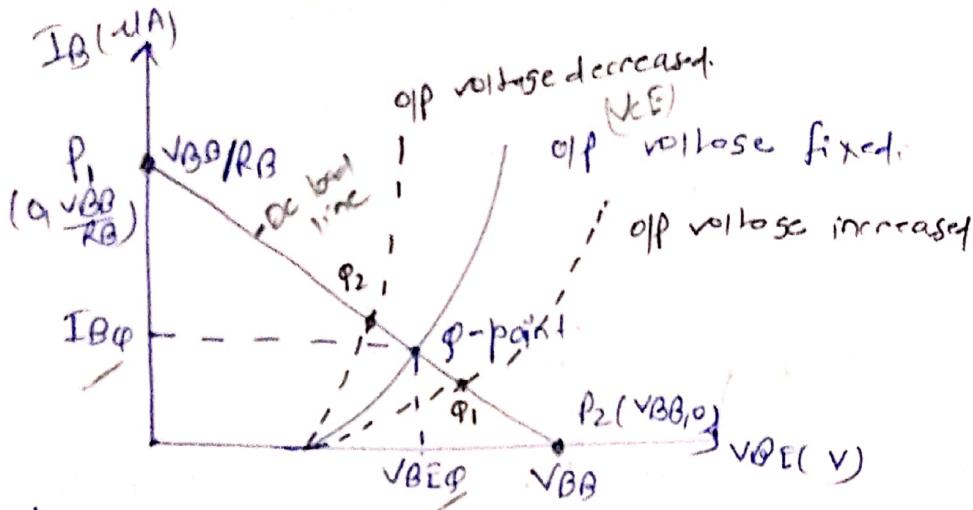
To find P_2

$$\frac{y=0, \text{ using eq. (1)}}{I_B=0}$$

$$V_{BE} = V_{BB} = x_2$$

$$P_1 = \left(0, \frac{V_{BB}}{R_B} \right)$$

$$P_2 = (V_{BB}, 0)$$



line connecting P_1 and P_2 is load line which intersects i/p characteristics at a point (φ).

This intersection point is known as i/p operating point.

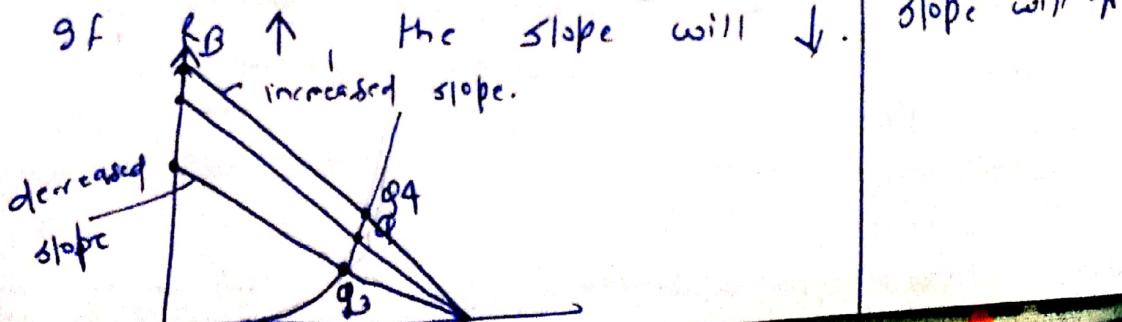
corresponding to φ -point, we have y-coordinate $I_{B\varphi}$ and x-coordinate is $V_{BE\varphi}$. These are the operating points of i/p for a particular o/p voltage.

* what if we increase the o/p voltage.

If we increase the o/p voltage, the i/p characteristics shifts to right side and φ points also shift to right (φ_1). For decreased o/p voltage, the operating point shifts to the left (φ_2).

Slope of the curve = $-1/R_B$

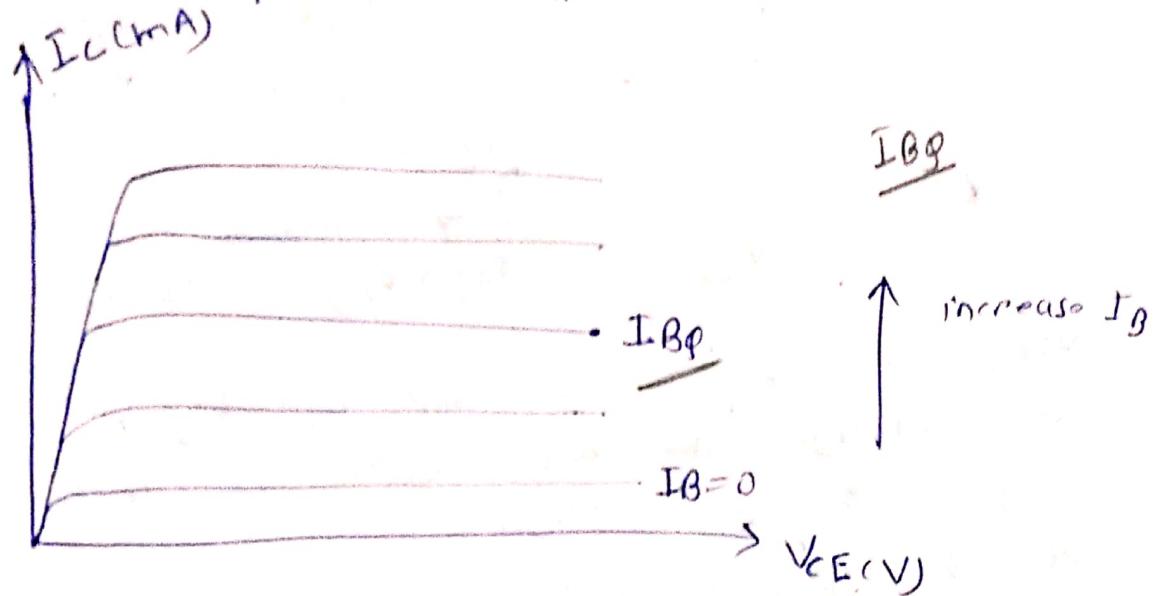
If $R_B \uparrow$, the slope will \downarrow .



If $R_B \downarrow$, slope will \uparrow

Output operating point

It is given by intersection of DC load line for with o/p characteristics curve for a particular i/p current.



If we use KVL in o/p loop of the circuit

$$V_{cc} - I_c R_c - V_{ce} = 0$$

$$I_c R_c = V_{cc} - V_{ce}$$

$$I_c = -\frac{V_{ce}}{R_c} + \frac{V_{cc}}{R_c} \quad (1)$$

$$y = mx + c$$

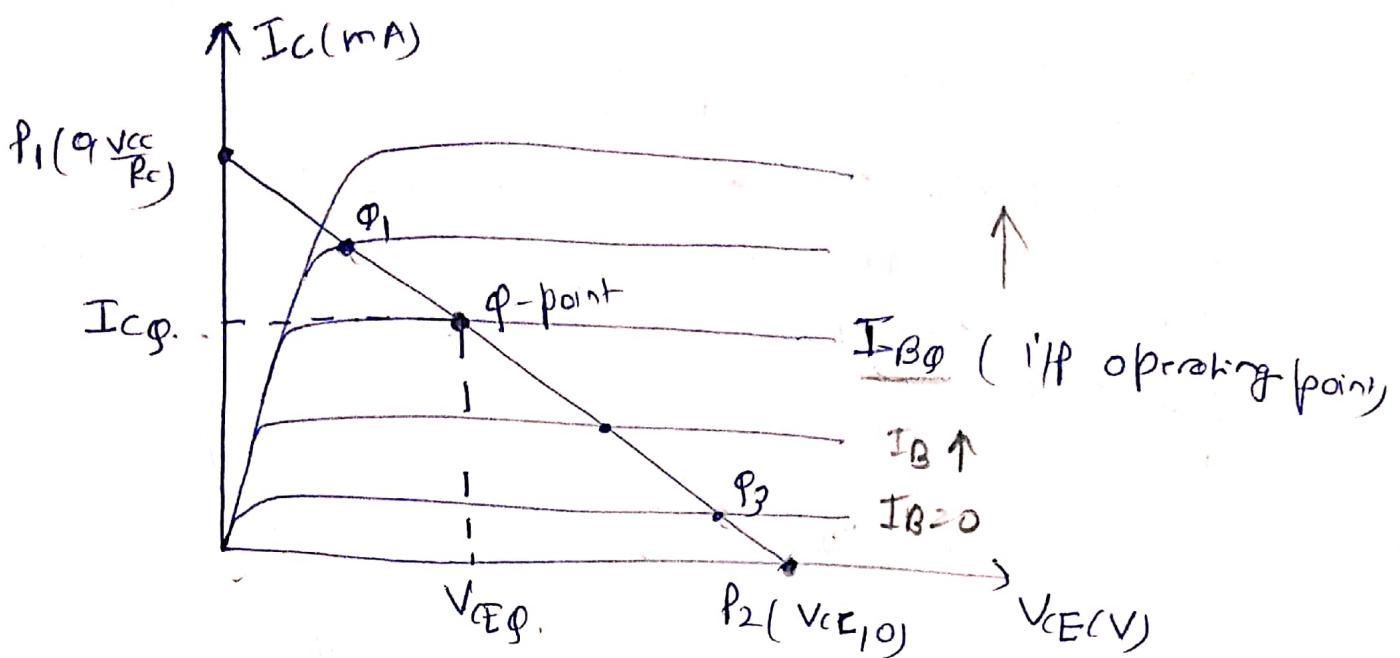
$$P_1(0, y_1), P_2(x_2, 0)$$

$$\frac{P_1}{P_2} \quad x=0; V_{ce}=0, \text{ from eq (1)}$$

$$\boxed{I_c = V_{cc}/R_c}, \quad P_1(0, V_{cc}/R_c)$$

$$\frac{P_2}{P_1} \quad y=0, I_c=0$$

$$\boxed{V_{ce} = V_{cc}} \quad P_2(V_{cc}, 0)$$



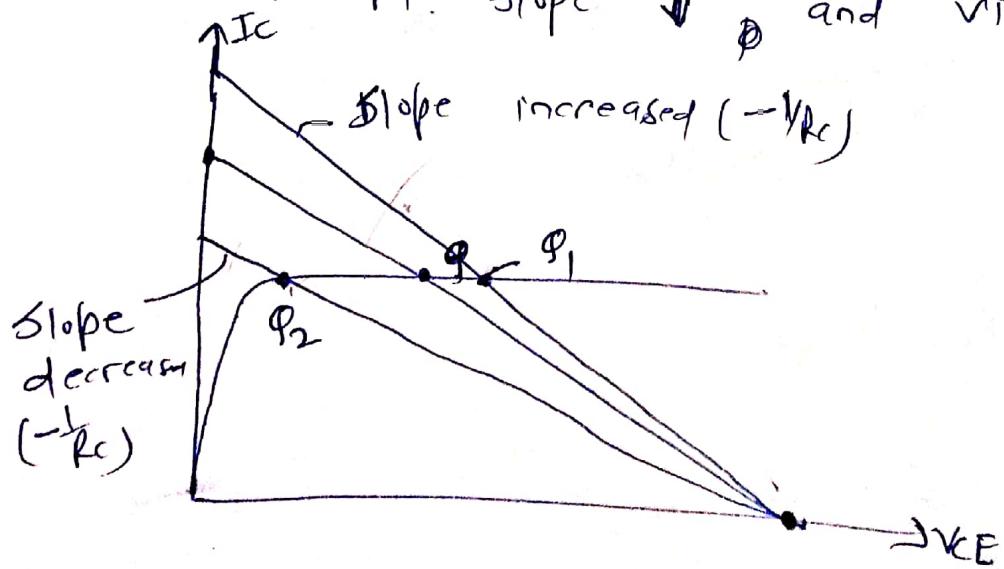
$V_{CE\phi}$ and $I_{C\phi}$ are O/P operating point. If we change the base current I_B then operating point φ - will change.

If $I_B \uparrow$, φ will shift up

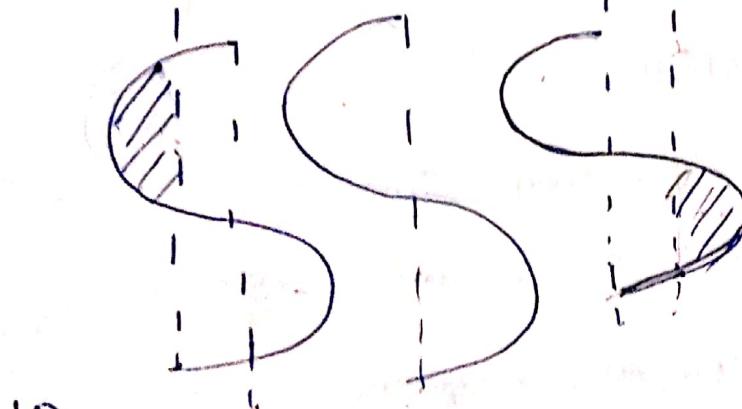
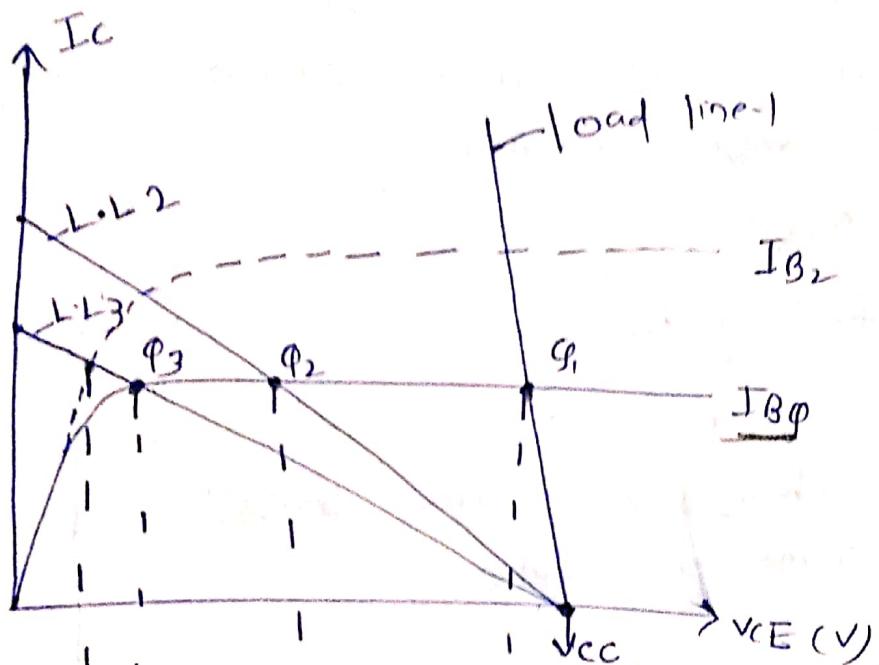
If $I_B \downarrow$, φ point will shift down

$$\text{at } \varphi_1, \text{ slope} = -\frac{1}{R_C}$$

If $R_C \uparrow$, slope \downarrow φ and vice versa



Setting off operating point is very important.
~~Q-point~~ should be in the middle of
Active region of Q-point is near to saturation
 or cut off region of o/p characteristics, then
 we will get distorted signal.



QD

O/p voltage can be less than or equal to supply voltage Vcc. But in case of Q_1 , the o/p voltage is greater than Vcc (shading). Hence positive cycle of the o/p waveform will be clipped.

Similarly, for Q_3 -operating-point, negative portion of the o/p waveform will be clipped. The o/p will be distorted.

Q_2 is in the middle of active region and hence we can see that it is distortion free. We should always maintain the g-point in the middle of active region.

Once one point is selected, it should not change with change in collector current.

Now collector current changes because of two reasons,

i) Change in β .

$$I_c = \beta \cdot I_B$$

$\beta \uparrow, I_c \uparrow$

How β changes? Two transistor can not have same β value.

ii) Change in temperature.

$$I_c = \beta I_B + (1/\beta) I_{B0}$$

$I_{B0} \rightarrow$ Reverse Saturation Current

Depends on minority charge carriers



Depends on Temperature

If Temp. $\uparrow, I_{B0} \uparrow, I_c \uparrow$

If I_c changes, the load line will change and also the g-point will change.

* To avoid the change in I_c which changes the change in g-point, we use biasing circuits.