Final Project

Logic Design

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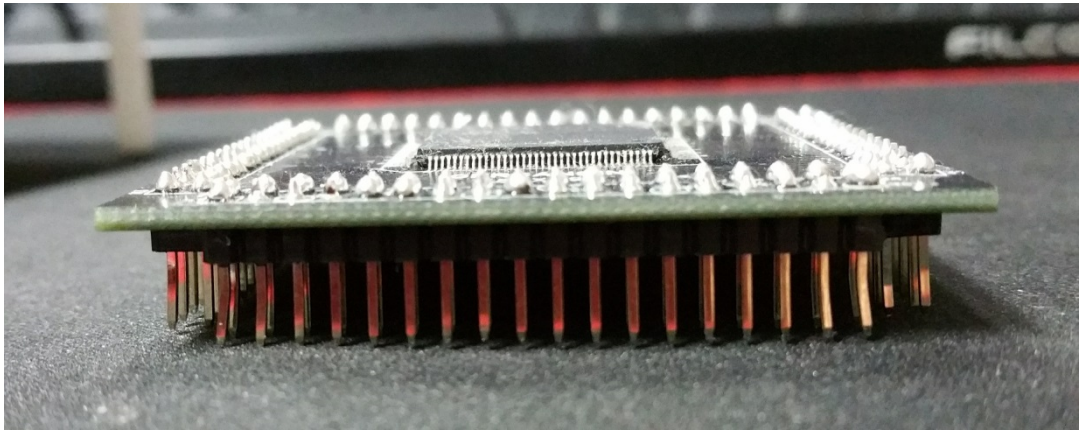
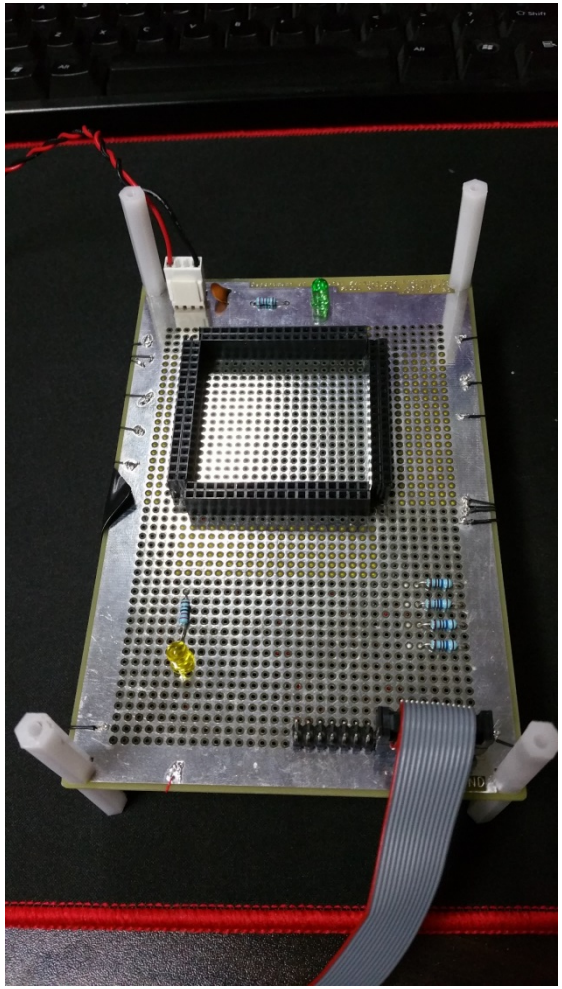
FPGA

FPGA – Spartan 3AN (1/2)



FPGA – Spartan 3AN (2/2)



Board

JTAG – DS300

FPGA Board

- Spartan 3AN / DS300 Datasheet 확인하여 Programming board 구현
  - Proper voltage, pin number 등등 확인

Table 62: **Types of Pins on Spartan-3AN FPGAs *(Cont'd)***

Type with Color Code	Description	Pin Name(s) in Type(1)
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. The In-System Flash memory is powered by VCCAUX. All must be connected to +3.3V.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination.	N.C.

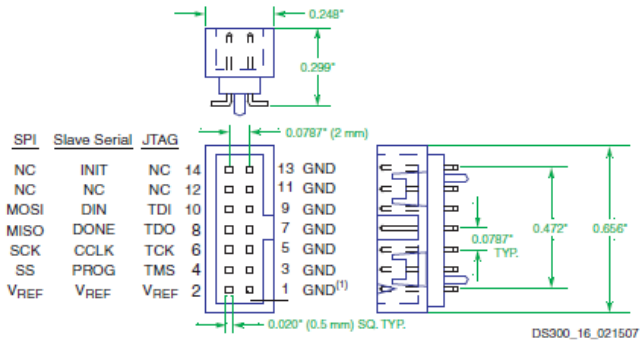
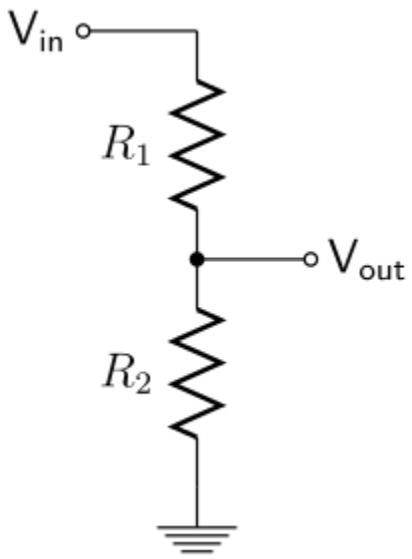


Figure 17: **Target Interface Connector Dimensions and Signal Assignments**

Voltage Divider



Final Project

Project Description

- Implementing Multi-function watch with Xilinx FPGA
  - Control inputs(Mode, Reset, Start , … etc.), and a clock signal input
  - Various function of watch should be displayed on a series of 7-segment displays

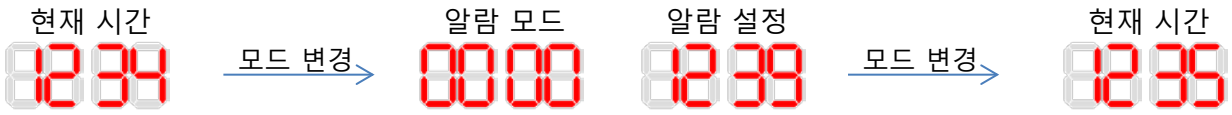
Specifications (1/2)

- Basic function (3 modes)
  - Time
    - 시간 설정
    - 7-segment를 이용하여 현재 시간(시, 분, 초) 표시
  - Alarm
    - 알람 시간 설정
    - 설정한 시간이 되면 알림
  - Stop watch
    - Start / Stop / Reset 등의 기능을 통해 시간 측정

- Extra implementation
  - No limitation
    - 자유롭게 흥미로운 추가 기능을 생각하여 구현
    - 단, 보드나 FPGA를 추가로 사용하는 것은 불가능

Specifications (2/2)

- Details
  - 시계 기능
    - Oscillator의 clock을 modulation 하여 현재 시간을 정확히 증가하게 해야 함
    - 버튼을 이용하여 현재 시간을 새롭게 설정할 수 있어야 함 (minute 단위까지)
  - 알람 기능
    - 버튼을 이용하여 알람이 동작할 시간을 설정할 수 있어야 함 (minute 단위까지)
    - 현재 시간과 설정한 시간이 같아지면 이를 알 수 있어야 함 (e.g. LED 점등)
  - 모드 변경
    - 모드 변경 시에도 다른 모드의 기능은 정상적으로 동작해야 함
    - E.g. 시계 기능에서 알람 기능으로 변경하여 알람을 설정하고, 다시 시계 기능으로 변경하여도 시간은 정상적으로 증가하고 있어야 함



Components

- XC3S50AN-4TQG144C FPGA
- 7-segment displays (you may use a 4-digit 7-segment display)
- LEDs
- Tactile switches (for input button)
- 1 MHz crystal oscillator
- Schmidt trigger inverter (to get rid of chattering)
- BCD-to-7-segment decoder

Project Grading

- **Due: 7pm, June 15th**

- **Behavior Correctness (60%)**
  - Partial points for incomplete implementation

- **Wiring / Soldering Quality (15%)**

- **Report (25%)**
  - 1 for each group (Not per person)

- **Extra credit (max. 20%)**