

Lab 11

Logic Design
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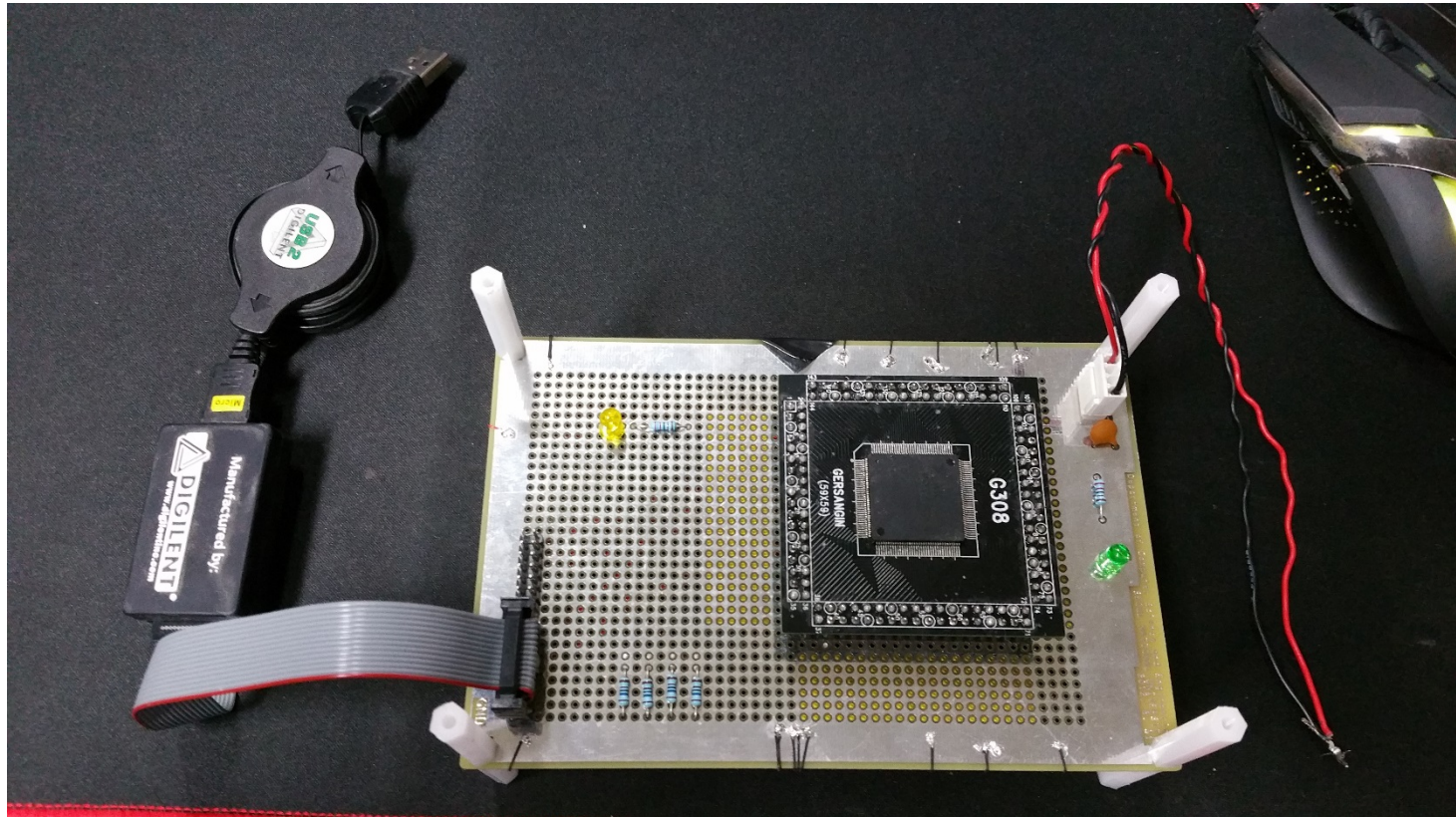
Overview

- **FPGA on a universal board**
- **Running on the board**
- **Practice**
- **Report**

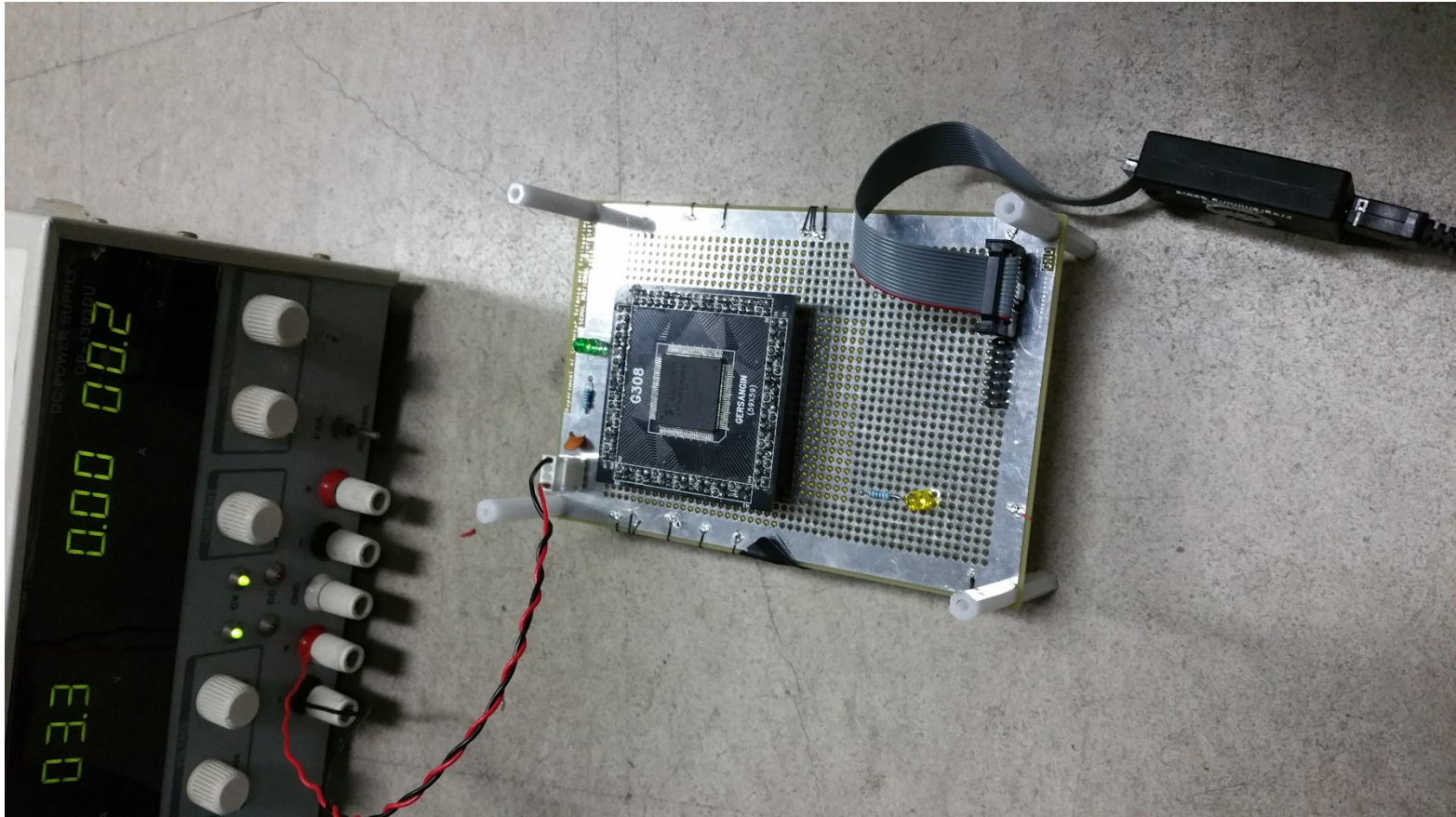
FPGA – JTAG (DS300)



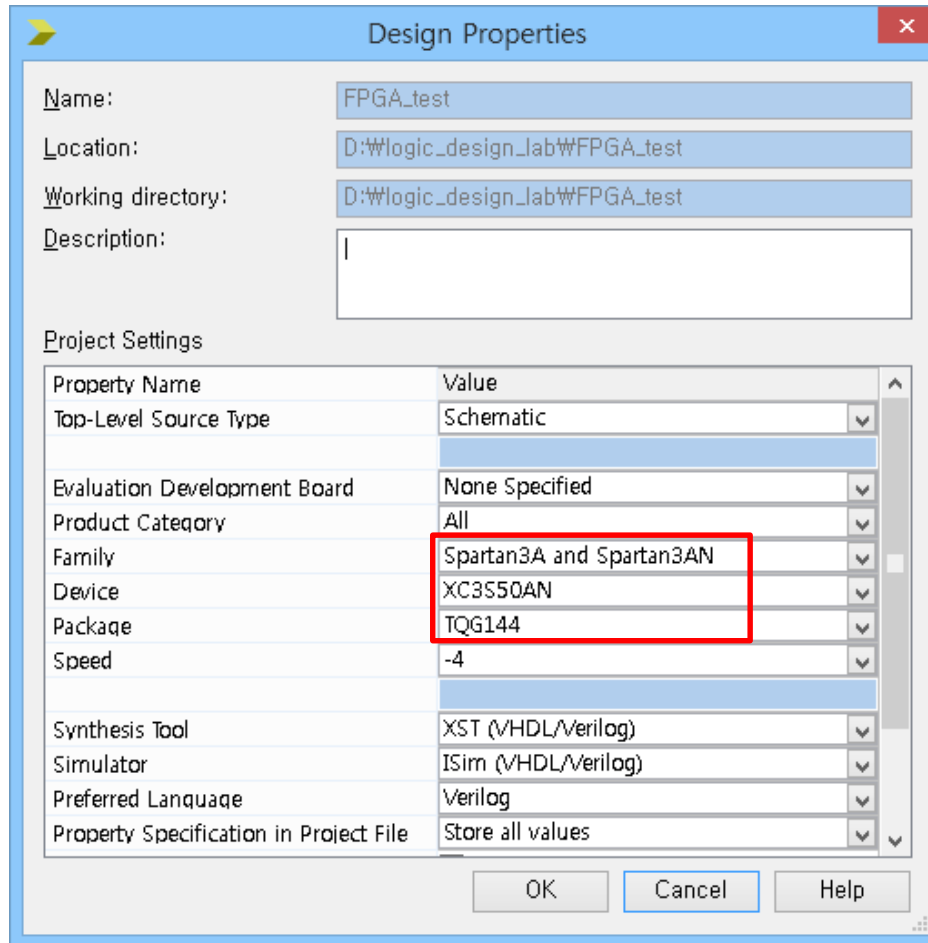
FPGA



FPGA



Running on the board



The image shows a 'Design Properties' dialog box with a blue title bar and a red close button. It contains several input fields and a table of project settings.

Name: FPGA_test

Location: D:\Wlogic_design_lab\FPGA_test

Working directory: D:\Wlogic_design_lab\FPGA_test

Description: |

Project Settings

Property Name	Value
Top-Level Source Type	Schematic
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3A and Spartan3AN
Device	XC3S50AN
Package	TQG144
Speed	-4
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values

Buttons: OK, Cancel, Help

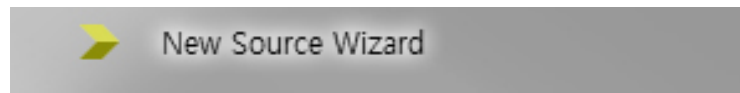
Running on the board

- **Implement Verilog code and test bench**

- Check the syntax for device
- Make sure it works properly in simulation

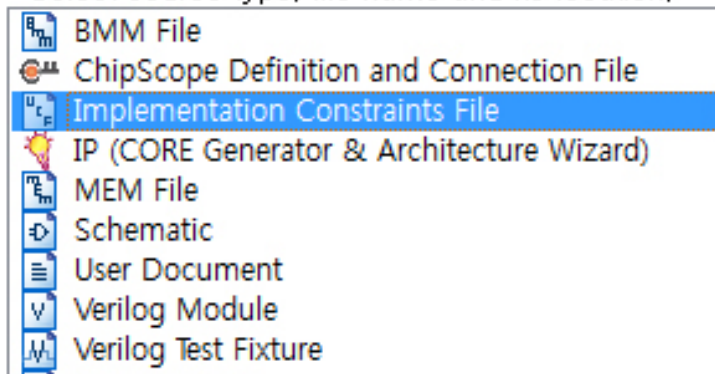
- **Make constraints file for the device**

- 코드를 통해 만든 input/ output을 실제 디바이스에 연결하기 위한 규칙을 설정할 텍스트 파일



Select Source Type

Select source type, file name and its location.



- New source > Implementation Constraints File

- Write filename and click OK, then ucf file will be generated

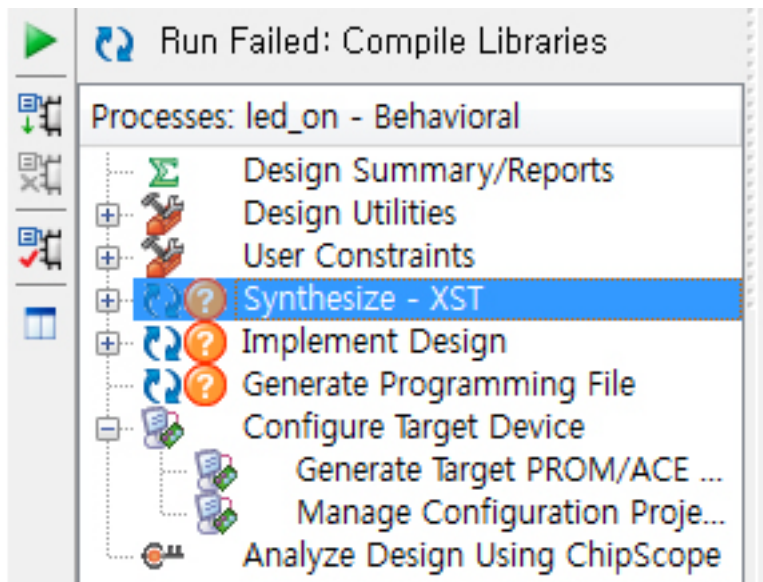
Running on the board

- Example of user constraint files

```
NET "LED_O[0]" LOC = P42 | IOSTANDARD = LVTTTL;  
NET "LED_O[1]" LOC = P46 | IOSTANDARD = LVTTTL;
```

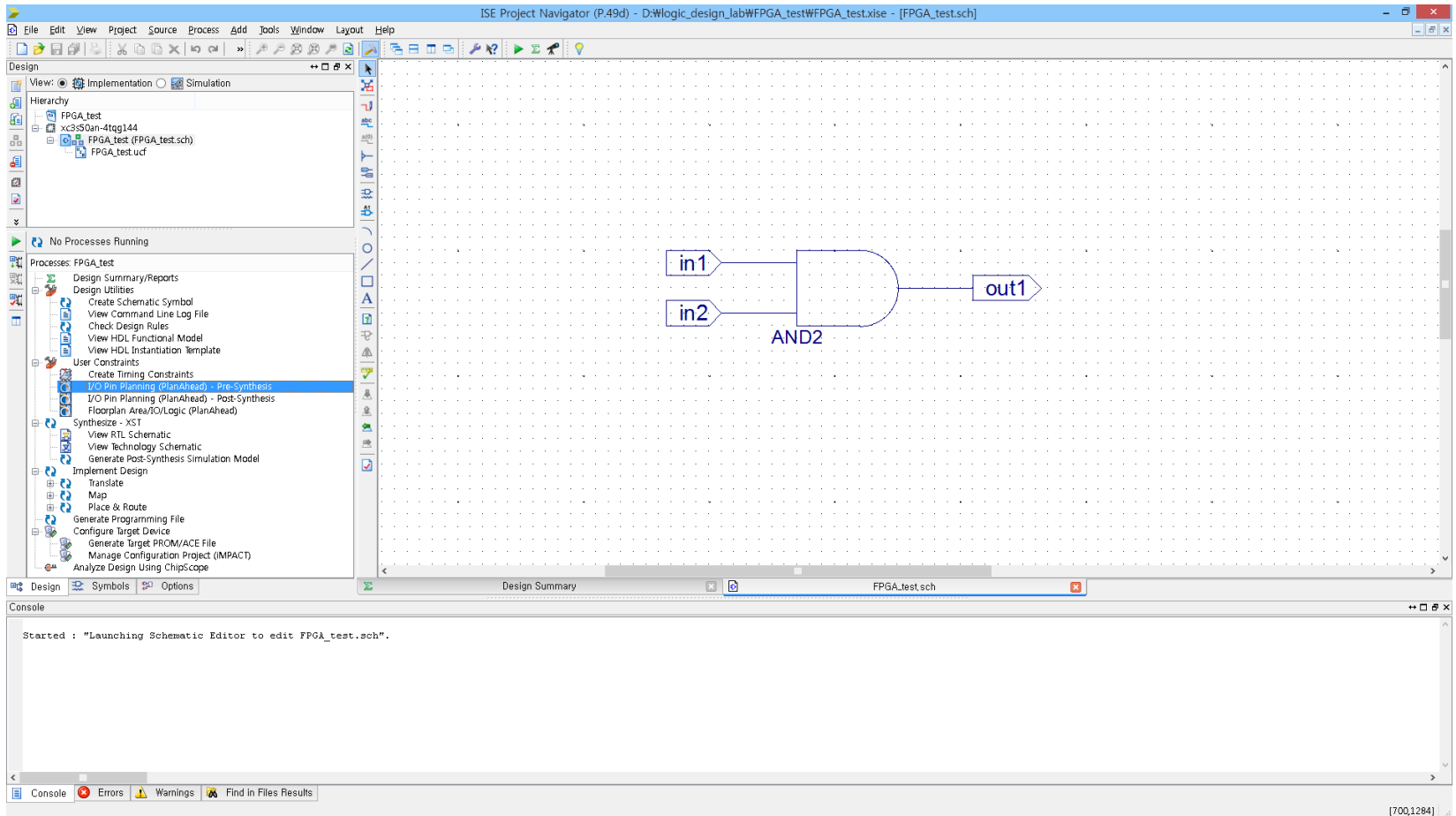
- 핀 번호와 관련된 사항은 etl의 datasheet 참조

- Compile design and generate programming file

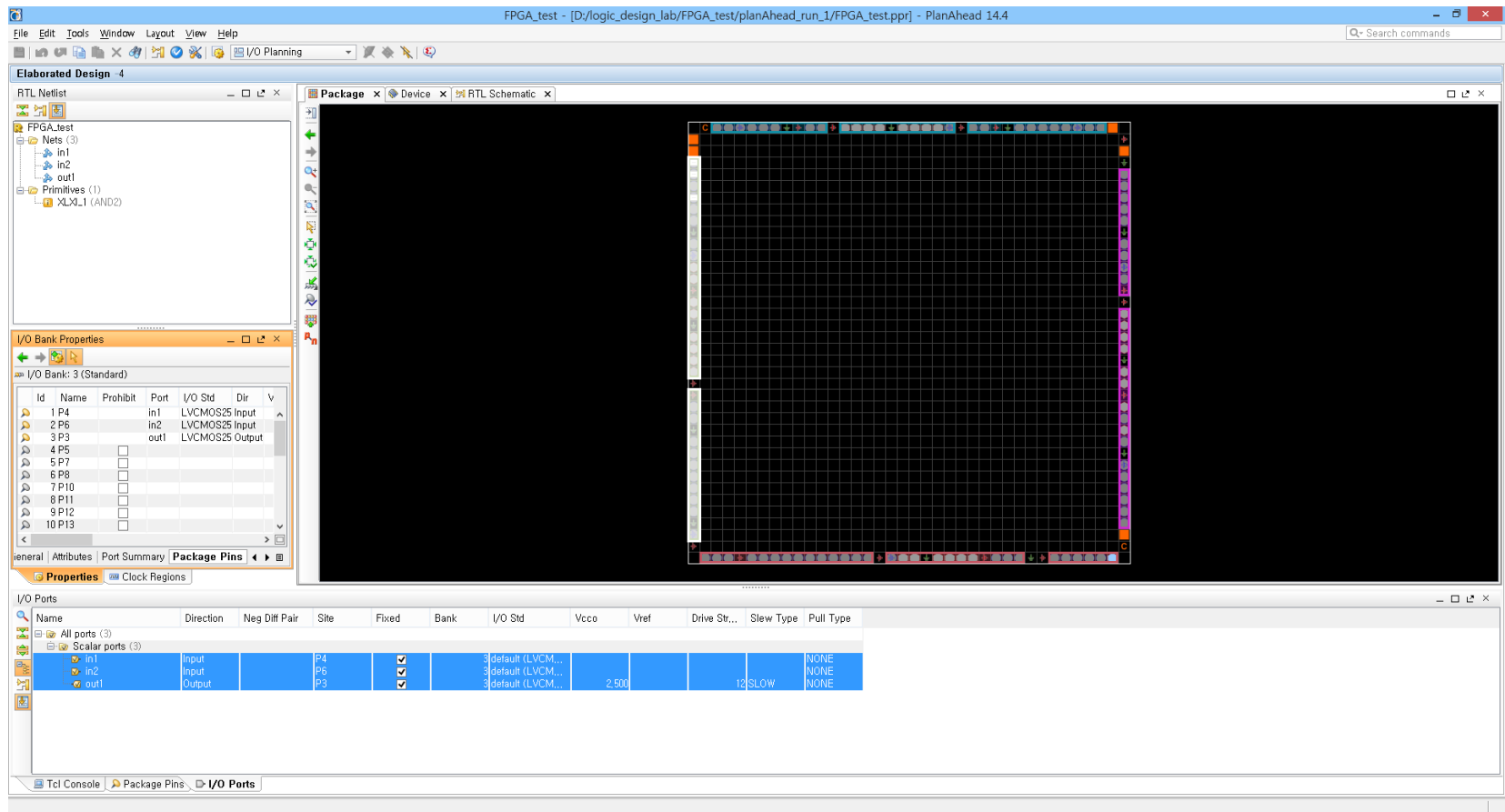


- Run Synthesize, Implement Design, and Generate Programming file
- Now we can see **.bit** file are generated in your project directory

Running on the board

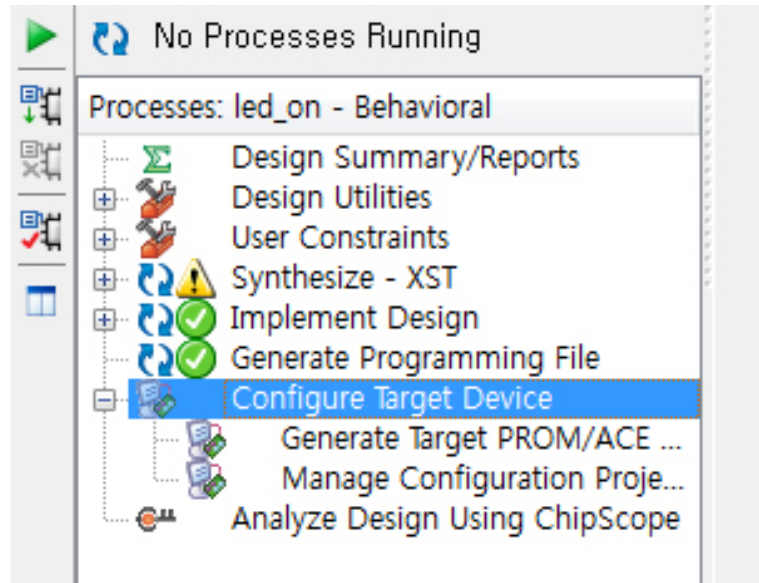


Running on the board

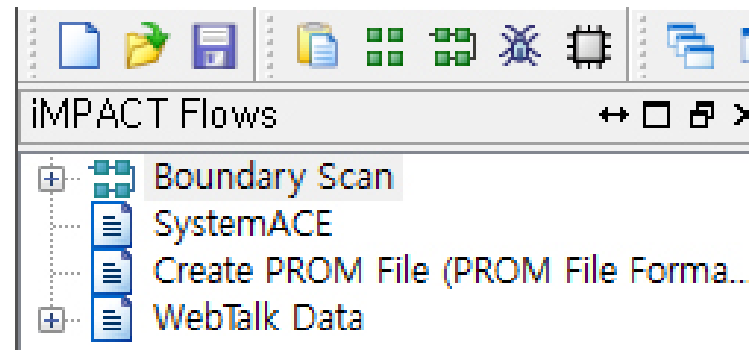


Running on the board

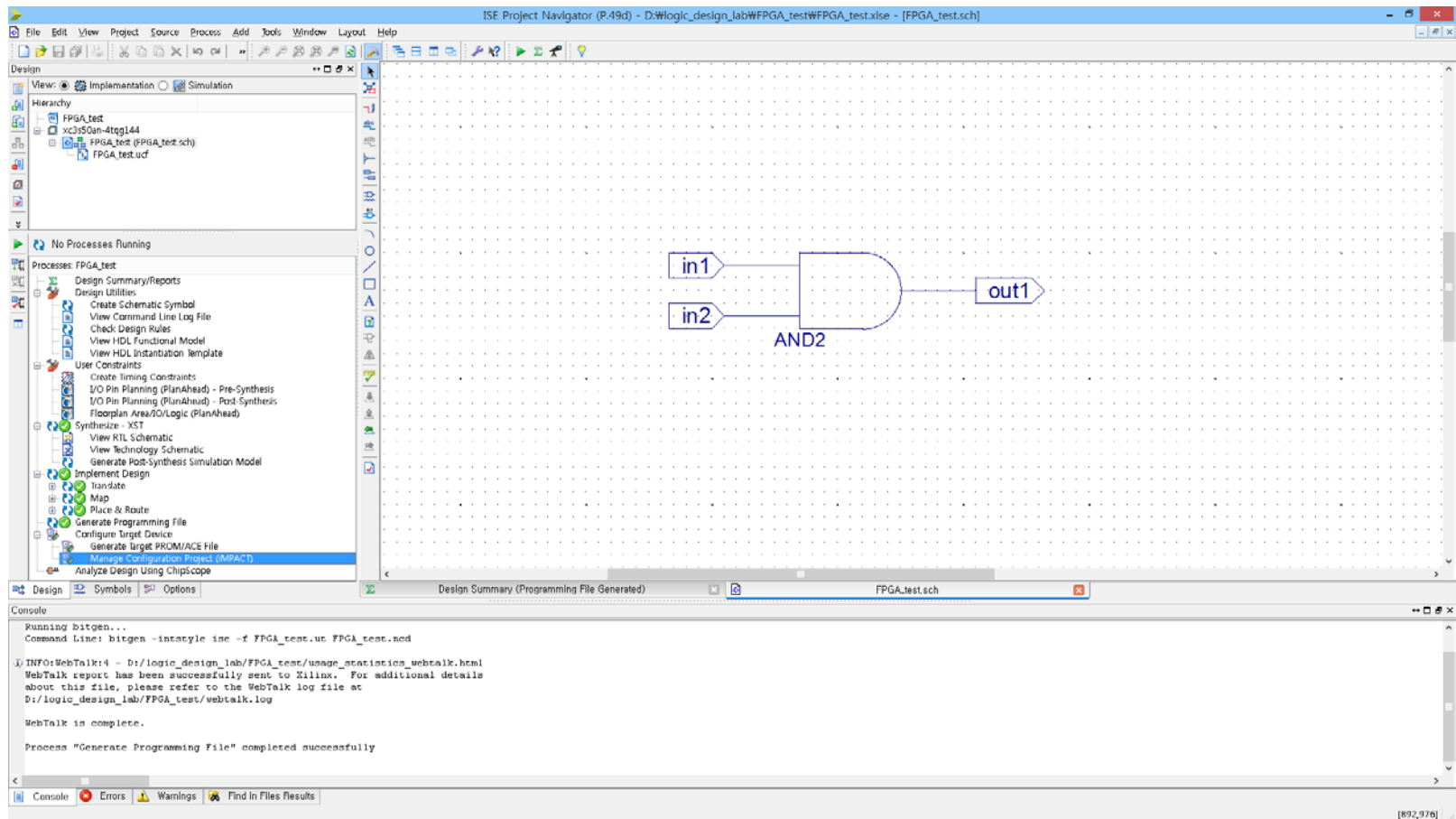
- **Configure Target Device**



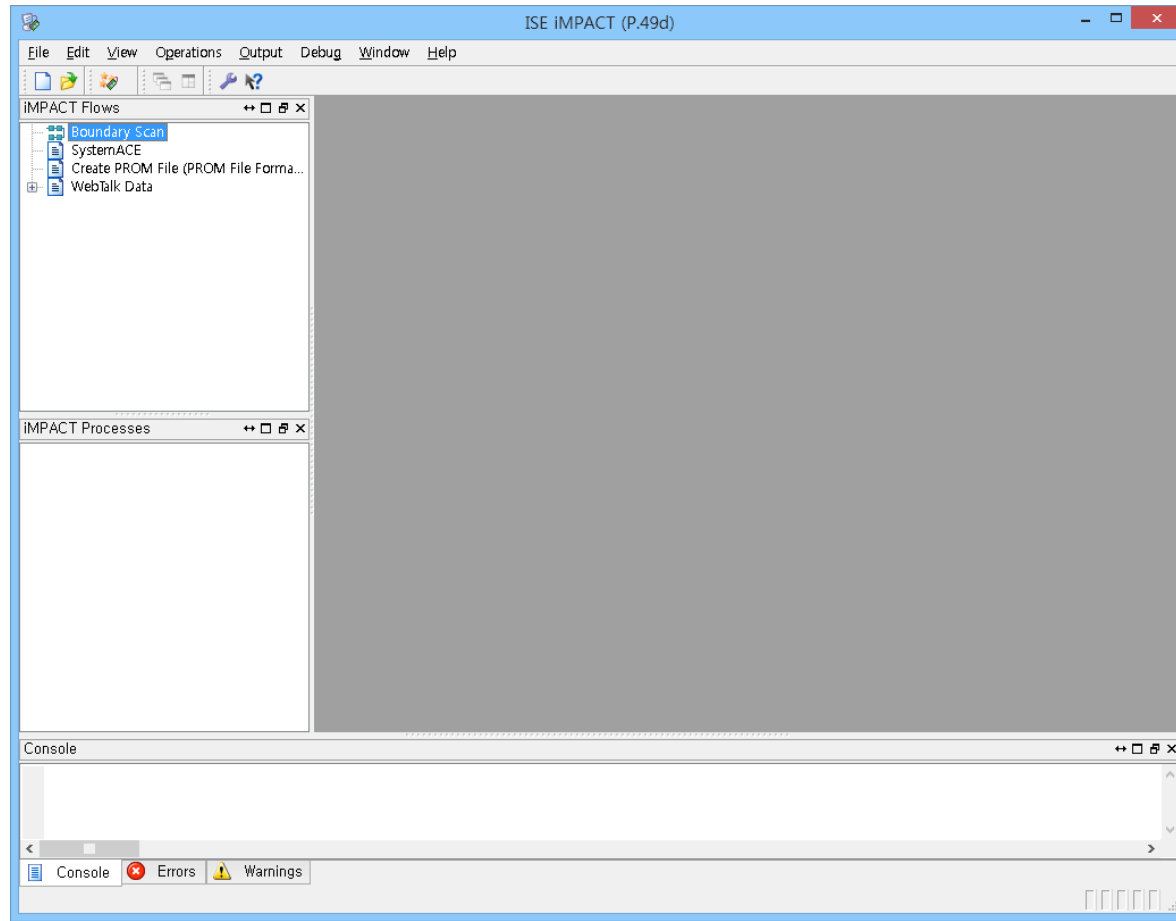
- Processes 탭에서 Configure Target Device 를 더블 클릭한다.
- ISE IMPACT 라는 창이 나타나면, IMPACT Flow에서 Boundary Scan을 더블 클릭한다.



Running on the board

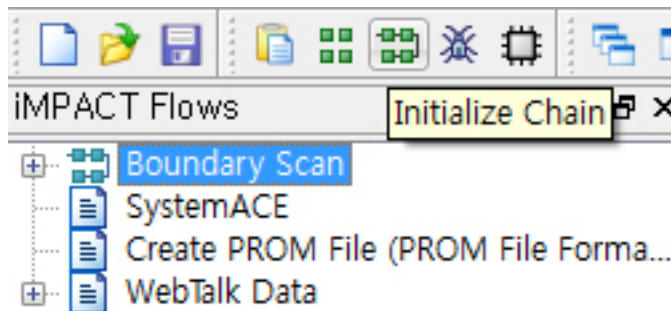


Running on the board

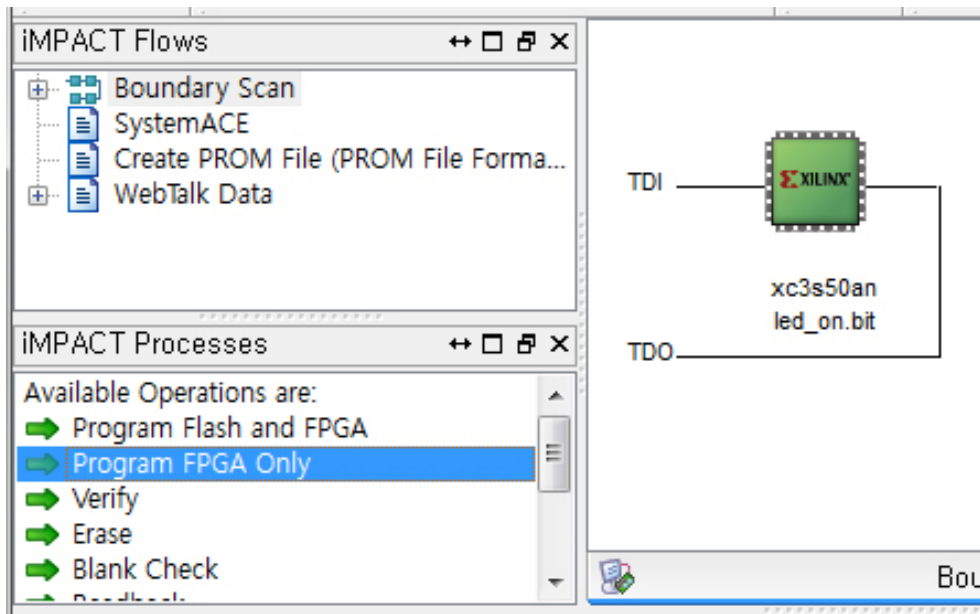


Running on the board

- **Configure Target Device**



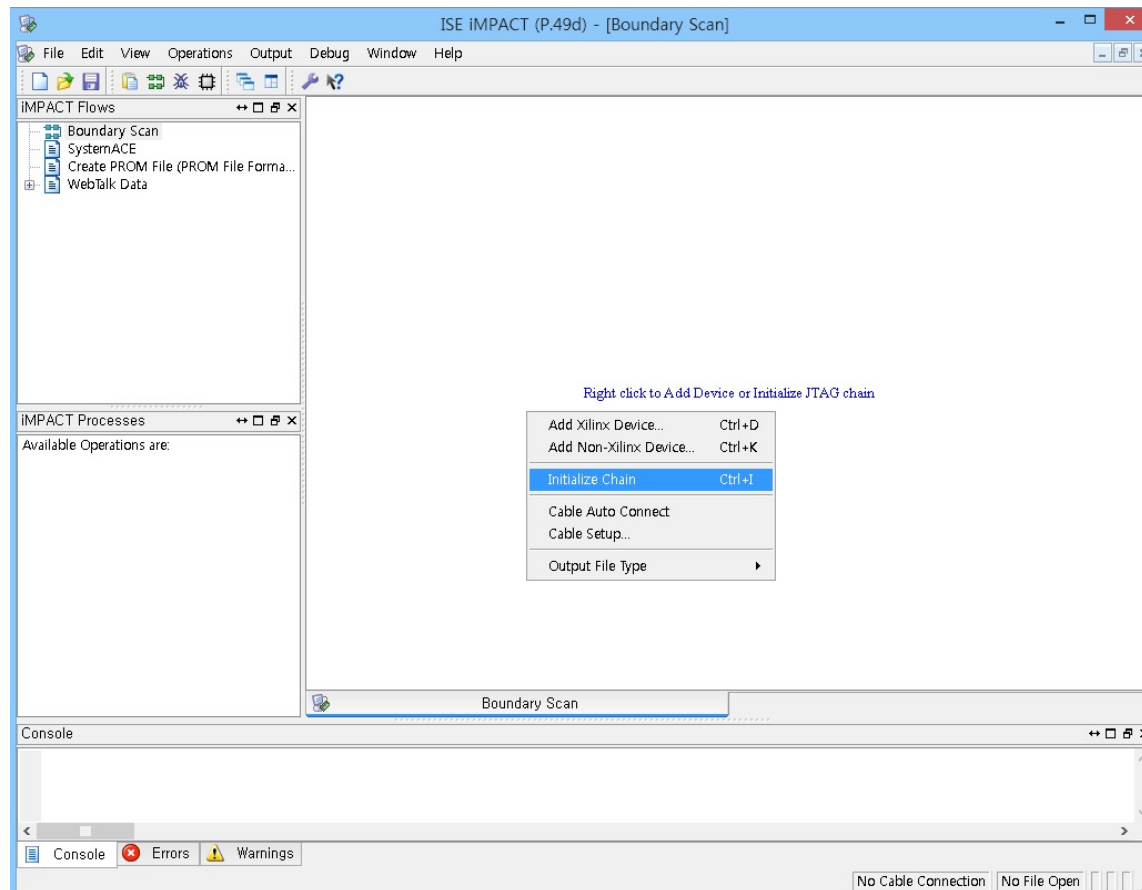
- Initialize Chain 버튼을 클릭하거나 흰 화면을 우클릭 한다.
- 파일 다이얼로그가 나타나면 앞서 생성한 .bit 파일을 선택한다.



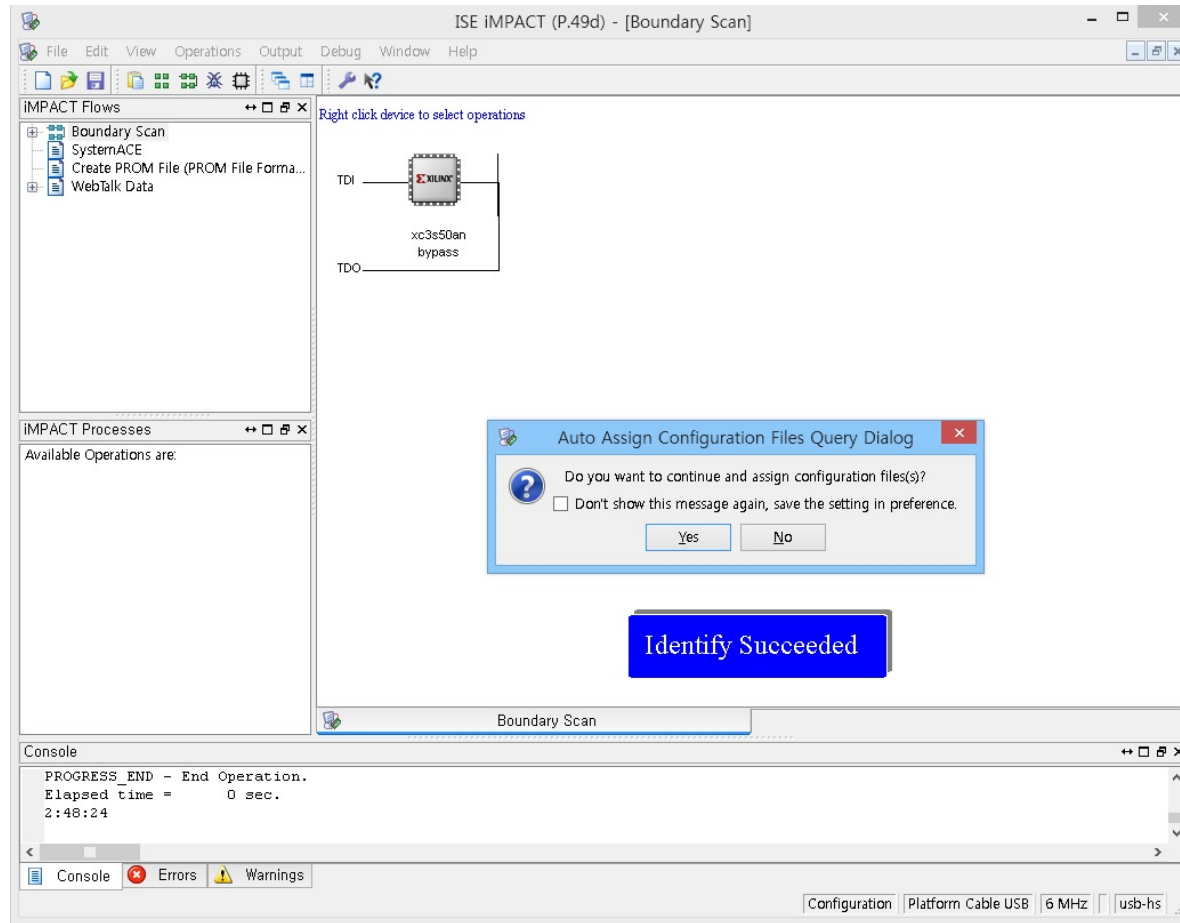
- FPGA가 1개 존재하는 보드임을 확인 할 수 있음
- 칩에 우클릭하거나 IMPACT Processes 에서 Program FPGA Only를 수행한다.

Program Succeeded

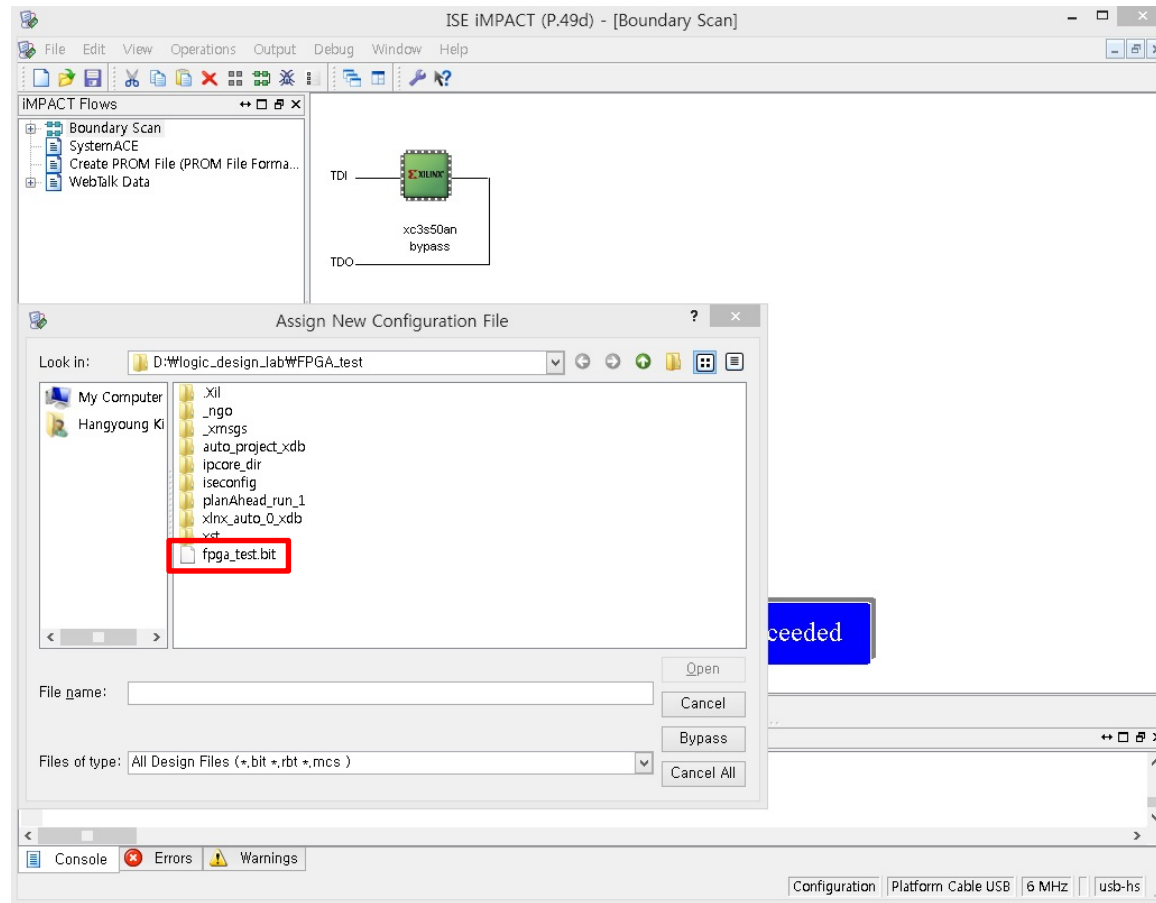
Running on the board



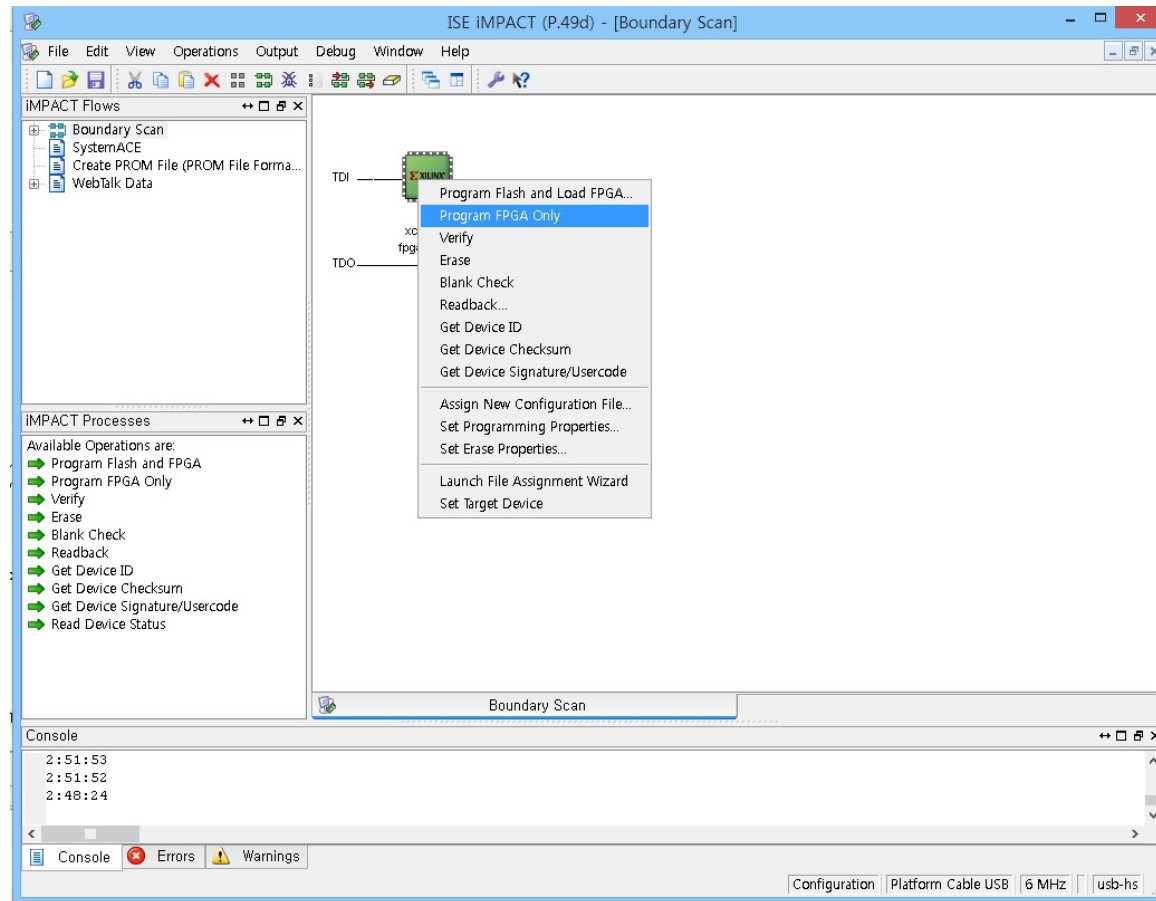
Running on the board



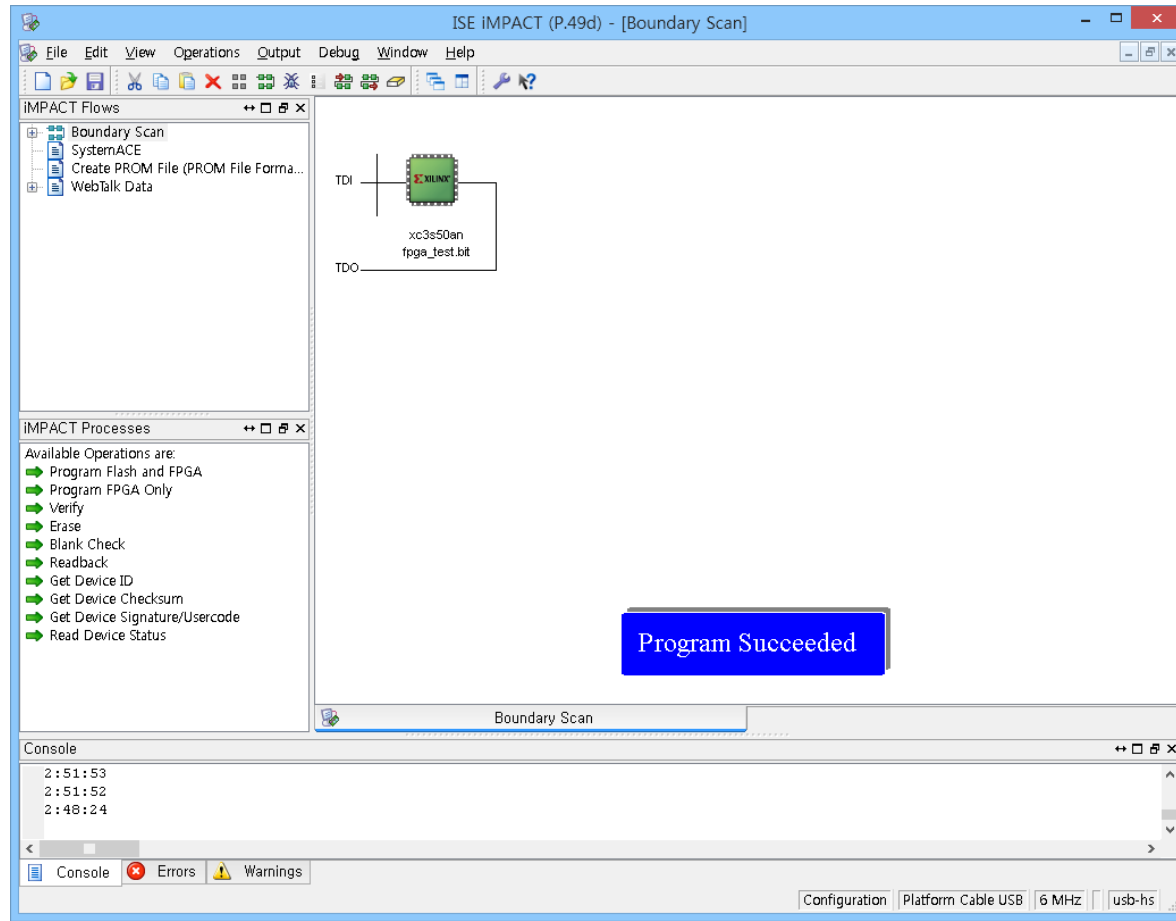
Running on the board



Running on the board



Running on the board



Practice

- **Implement FPGA on a universal board**
 - Take a good care of the Spartan chipset
 - Inventory is not enough
- **Deploy your stop watch code on FPGA board**
 - Make sure your simulation works perfectly

Report

- No report on today's practice
- Stop watch is a part of Final term project
- Merge today's result into your final term project
- This is the final class before the final term project
- All report scores will be uploaded before **6/15**