ISE

Synthesis Options

The following properties apply to the Synthesize process using the Xilinx® Synthesis Technology (XST) synthesis tool. These options are for VHDL or Verilog designs and for FPGA and CPLD devices, unless otherwise noted.

- **Optimization Goal**

  Specifies the global optimization goal for area or speed.

  Select an option from the drop-down list.
  - **Speed**

    Optimizes the design for speed by reducing the levels of logic.
  - **Area**

    Optimizes the design for area by reducing the total amount of logic used for design implementation.

  By default, this property is set to Speed.
- **Optimization Effort**

  Specifies the synthesis optimization effort level.

  Select an option from the drop-down list.
  - **Normal**

    Optimizes the design using minimization and algebraic factoring algorithms.
  - **High**

    Performs additional optimizations that are tuned to the selected device architecture. "High" takes more CPU time than "Normal" because multiple optimization algorithms are tried to get the best result for the target architecture.

  By default, this property is set to Normal.
- **Power Reduction (Virtex®-4 and Virtex-5 only)**

  When set to Yes (checkbox is checked), XST optimizes the design to consume as little power as possible. Power Reduction is allowed whether the Optimization Goal is set to Area or Speed, but its use may have negative affects on the final overall area and speed of the design.

  By default, this property is set to No (checkbox is blank).
- **Use Synthesis Constraints File**

  Specifies whether or not to use the constraints file entered in the previous property. By default, this constraints file is used (property checkbox is checked).
- **Synthesis Constraints File**

  Specifies an Xilinx constraints file (XCF) for XST synthesis constraints. For more information on entering XST constraints or using the synthesis constraints file, see the XST User Guide.

  By default, this property is blank. Enter the location and file name of the constraints file you want to use during synthesis, or click the Browse button and browse to the constraints file.
- **Library Search Order (Advanced)**

  Specifies a custom library search order file (*.lso) which defines the order in which source files are compiled. If no file is specified here, a default library search order file called `<design>.lso` is created. You can modify the default file, but then you must specify the modified file in this property.
- **Keep Hierarchy (Advanced)**

  Specifies whether or not the corresponding design unit should be preserved and not merged with the rest of the design. You can specify Yes, No and Soft. Soft is used when you wish to maintain the hierarchy through synthesis, but you do not wish to pass the keep_hierarchy attributes to place and route.

  By default, this property is set to No.
- **Netlist Hierarchy (Advanced)**

  Controls the form in which the final NGC netlist is generated. Netlist Hierarchy allows you to write the hierarchical netlist even if the optimization was done on a partially or fully flattened design.

  Select an option from the drop-down list.
  - **As Optimized**

XST takes into account the KEEP_HIERARCHY constraint, and generates the NGC netlist in the form in which it was optimized. If As Optimized is selected, some hierarchical blocks can be flattened, and some can maintain hierarchical boundaries.

- **Rebuilt**

  XST writes a hierarchical netlist, regardless of the KEEP_HIERARCHY constraint.

By default, this property is set to As Optimized.

- **Global Optimization Goal (FPGA only)**

  Specifies the global timing optimization goal. For more information about global timing constraints support, see the Timing Constraints section in the "Design Constraints" chapter in the XST User Guide.

  Select an option from the drop-down list.

  - **AllClockNets**

    Optimizes the period of the entire design.
  - **Inpad to Outpad**

    Optimizes the maximum delay from input pad to output pad throughout an entire design.
  - **Offset In Before**

    Optimizes the maximum delay from input pad to clock, either for a specific clock or for an entire design.
  - **Offset Out After**

    Optimizes the maximum delay from clock to output pad, either for a specific clock or for an entire design.
  - **Maximum Delay**

    Global optimization will be set to maximum delay constraints for paths that start at an input and end at an output. This option incorporates the goals of all the above options.

  By default, this property is set to AllClockNets.
- **Generate RTL Schematic**

  Generates a pre-optimization RTL schematic of the design. Values for this property are Yes, No, and Only. Only stops the synthesis process before optimization, after the RTL schematic has been generated.

  The default value is Yes.
- **Read Cores (Advanced) (FPGA only)**

  Specifies whether or not black box cores are read for timing and area estimation in order to get better optimization of the rest of the design. When set to True (checkbox is checked), XST parses any black boxes that have been instantiated in your code to extract timing and resource usage information. Decisions about optimizations to the logic surrounding the black boxes are made with this information. The black box netlists are not modified or re-written. When set to False (checkbox is blank), cores are not read.

  By default, this property is set to True (checkbox is checked).
- **Cores Search Directories (Advanced) (FPGA only)**

  Specifies the locations of the black box netlists (EDIF, NGC, NGO) specified for the Read Cores property. To specify multiple search paths, type in multiple paths, using the pipe (|) symbol to separate each path. You can also click the Browse button to browse to the first path and type in subsequent paths, using the pipe (|) symbol to separate each path.
- **Write Timing Constraints (FPGA only)**

  Specifies whether or not to place timing constraints in the NGC file. The timing constraints in the NGC file will be used during place and route, as well as synthesis optimization.

  By default, this property is set to False (checkbox is blank).
- **Cross Clock Analysis (Advanced) (FPGA only)**

  Enables the timing analysis of related synchronous elements that are driven by different clocks.

  By default, this property is set to False (checkbox is blank), and timing analysis is not performed.
- **Hierarchy Separator (Advanced)**

  Specifies the hierarchy separator character which will be used in name generation when the design hierarchy is flattened. The default setting is '/'. The underscore character '_' can be specified.
- **Bus Delimiter (Advanced)**

  Specifies the delimiter type used to define the signal vectors in the resulting netlist. Select from a variety of delimiters. The default bus delimiter is <>.
- **Slice Utilization Ratio (Advanced) (All FPGAs except Virtex-5)**

Specifies the area size (in %) that XST will not exceed during timing optimization. If the area constraint cannot be satisfied, XST will make timing optimization regardless of the area constraint. The default ratio is 100%. You can disable automatic resource management by entering -1 here.

- **LUT-FF Pairs Utilization Ratio (Advanced) (Virtex-5 only)**

  Specifies the area size (in %) that XST will not exceed during timing optimization. If the area constraint cannot be satisfied, XST will make timing optimization regardless of the area constraint. The default ratio is 100%. You can disable automatic resource management by entering -1 here.
- **BRAM Utilization Ratio (Advanced) (FPGA only)**

  Specifies the number of BRAM blocks (in %) that XST will not exceed during synthesis. The default percentage is 100%. You can disable automatic BRAM resource management by entering -1 here.
- **DSP Utilization Ratio (Advanced) (Virtex®-4, Virtex-5, and Spartan®-3A D only)**

  Specifies the number of DSP 48 blocks (in %) that XST will not exceed during synthesis. The default percentage is 100%.
- **Case (Advanced)**

  Specifies the case used for the instance and net names in the final netlist. You can select between using lower case, upper case or maintaining the current case. By default, this property is set to Maintain.
- **Work Directory (Advanced)**

  Specifies where the intermediate HDL files will be compiled.

  By default, this property displays ./xst, and the project directory is `%XILINX%/xst/work/`.
- **HDL INI File (Advanced)**

  Specifies a library mapping file that contains the library name and the directory where the library is compiled.
- **Verilog 2001**

  Specifies whether or not to interpret Verilog source code as the Verilog 2001 standard. By default, this property is set to True (checkbox is checked), and Verilog source code is interpreted as Verilog 2001 standard.
- **Verilog Include Directories (Advanced)**

  Specifies the discrete paths to your Verilog include Directories. To specify multiple paths, type in multiple paths, using the pipe (|) symbol to separate each path. You can also click the Browse button to browse to the first path and type in subsequent paths, using the pipe (|) symbol to separate each path. There is no default.
- **Generics, Parameters (Advanced)**

  Allows you to redefine generic (VHDL) or parameter (Verilog) values defined in the top-level design block. When the design is synthesized, the generics/parameters you specify here will override the ones in the HDL source. To specify multiple generics or parameters, type in multiple entries, using the pipe (|) symbol to separate each generic or parameter (for example, **`company="Xilinx" | width=5 | init_vector=b100101`**). There is no default.
- **Verilog Macros (Advanced)**

  Allows you to define or redefine Verilog macros for the design. When the design is synthesized, the macros you specify here will override the ones in the HDL source. To specify multiple macros, type in multiple entries, using the pipe (|) symbol to separate each macro (for example, **`macro1="Xilinx" | macro2="Xilinx Virtex 4"`**). There is no default.
- **Custom Compile File List (Advanced)**

  Specifies a custom compile list file (a text file). The user-defined compile list file that you define in this property is used to generate the compile instructions for synthesis. When the property is not set, the ISE® generated compile file list is used.

  The custom compile file lists the design files to be compiled and the libraries associated with each file. Each file and library pair is separated by a new line. The order of the design files determines the compile order. The following is an example of the file format:

  ```
  <library_name>;<file_name>

  [<library_name>;<file_name>]

   ...
  ```

  Note A library name is required. For Verilog files, you must specify the work library. You cannot create your own Verilog libraries.

  For more information about the custom compile file list, see Creating a Custom Compile List for Synthesis.
- **Other XST Command Line Options (Advanced)**

Enter additional command line options. Multiple options are separated with a space. The options entered in this property appear first on the command line, before all other property options specified in the graphical user interface. Avoid setting duplicate property options.

For more information about command line options, see the XST User Guide.