ISE

Place & Route Properties

The following properties apply to the Place & Route process and Implement Design process. These properties are the same for all FPGA devices.

- **Place and Route Mode**

  Specifies the type of place and route you want implemented in your design.

  Select an option from the drop-down list.
  - **Normal Place and Route**

    Runs PAR with effort levels you specify, or with default options.
  - **Place Only**

    Runs PAR with effort levels you specify, or with default options. The router will not run. The PAR process must be run at least once to use this option.
  - **Route Only**

    Runs PAR with effort levels you specify, or with default options. The placer will not run (current placement is kept). The PAR process must be run at least once to use this option.
  - **Reentrant Route**

    Placement and routing are kept. The router runs one time in reentrant mode using the existing routing if any as a starting point. The router is controlled by the effort level.

    Note This setting is for advanced flows and is normally not recommended.
  - **Multi Pass Place and Route**

    Runs PAR with effort level specified (High is recommended) for the specified number of iterations to provide the best possible placement for your design.

  For Virtex®-5 devices, only the Route Only and Reentrant Route options are available.

  By default, this property is set to Route Only for Virtex-5 devices, and Normal Place and Route for all other devices.
- **Place and Route Effort Level (Overall)**

  Specifies the effort level you want to apply to the Place & Route process. The effort level controls the placement and route times by selecting a more or less CPU-intensive algorithm for placement and routing. You can set the overall level from Standard (fastest run time) to High (best results).

  Note This property is not available for Virtex-5 devices.

  Select an option from the drop-down list.
  - **Standard**

    Gives the fastest run time with the lowest place and route effort. Appropriate for a less complex design.
  - **Medium**

    Gives a medium run time with equal place and route optimization.
  - **High**

    Gives the longest run time with the best place and route results. Appropriate for a more complex design.

  By default, this property is set at Standard.
- **Placer Effort Level (Overrides Overall Level) (Advanced)**

  Specifies the placement effort level used when placing your design. Specifying this property will override the placement effort level set in the Place and Route Effort Level (Overall) property.

  Note This property is not available for Virtex-5 devices.

  Select a property from the drop-down list.
  - **None**

    No placer effort level is applied.
  - **Standard**

    Gives a fast run time with lowest place effort. Appropriate for a less complex design.
  - **Medium**

    Gives a slower run time with some placing optimization.
  - **High**

Gives the best placing results, but will incur the longest run time. Appropriate for a more complex design.

By default, this property is set to None.

- **Router Effort Level (Overrides Overall Level) (Advanced)**

  Specifies the router effort level used when routing your design. Specifying this option will override the router effort level in the Place and Route Effort Level (Overall) option.

  Note This property is not available for Virtex-5 devices.

  Select an option from the drop-down list.
  - **None**

    No router effort level is applied.
  - **Standard**

    Gives a fast run time with lowest routing effort. Appropriate for a less complex design.
  - **Medium**

    Gives a slower run time with some routing optimization.
  - **High**

    Gives the best routing results, but will incur the longest run time. Appropriate for a more complex design.

  By default, this property is set to None.
- **Extra Effort (Highest PAR level only) (Advanced)**

  PAR spends additional run time in an effort to meet difficult timing constraints.

  Note The Extra Effort property is available only when the **Place and Route Effort Level** property is set to High.

  Select an option from the drop-down list.
  - **None**

    No extra effort level is applied.
  - **Normal**

    Runs until timing constraints are met unless they are found to be impossible to meet. This option focuses on meeting timing constraints.

    Note This setting may lead to very long run times. Design performance is not guaranteed to be better than when the **Place and Route Effort Level** property is set to High.
  - **Continue on Impossible**

    Continues working to improve timing until no more progress is made, even if timing constraints are impossible. This option focuses on getting close to meeting timing constraints.

    Note This setting may lead to very long run times. Design performance is not guaranteed to be better than when the **Place and Route Effort Level** property is set to High.

  By default, this property is set to None.
- **Starting Placer Cost Table (1-100)**

  Specifies a placement initialization value with which to begin the place and route attempts. Each subsequent attempt is assigned an incremental value based on the placement initialization value.

  Note This property is not available for Virtex-5 devices.

  The number you choose corresponds to a cost table index and results in different place and route strategies. Cost tables assign weighted values to relevant factors such as constraints specified in the input file (for example, certain components must be in certain locations), the length of connections, and the available routing resources. Cost-based placement is described in the "PAR Process" section in the "PAR" chapter in the Development System Reference Guide.

  Select a number from 1 to 100. By default, this property is set to 1.
- **Ignore User Timing Constraints**

  This property controls the use of timing constraints during place and route. The primary method of specifying timing requirements is by entering them in constraints files (UCF and PCF). For detailed information about timing constraints, see the Constraints Guide.

  If this property is not selected (checkbox is blank), PAR places and routes in accordance with any timing constraints specified in the Physical Constraints File (PCF).

  If this property is selected (checkbox is checked), timing constraints in the PCF are ignored when PAR runs.

The setting of the Timing Mode property (described below) determines whether PAR will automatically generate timing constraints to control placement and routing or will run without timing constraints.

- **Timing Mode**

  This property is enabled when the Ignore User Timing Constraints property (see above) is selected.

  The Timing Mode property specifies whether PAR will generate timing constraints automatically to control placement and routing or will run without timing constraints

  Select an option from the drop-down list.

  - **Performance Evaluation**

    This selection triggers the "Performance Evaluation" mode. In this mode timing constraints specified in the Physical Constraints File (PCF) are ignored. Instead, timing constraints for all internal clocks are generated automatically and dynamically adjusted during PAR to increase performance. This mode is used to evaluate realistic performance targets for the design.

    Performance Evaluation is described in the "PAR" chapter in the Development System Reference Guide.

  - **Non Timing Driven**

    In this mode, timing constraints specified in the Physical Constraints File (PCF) are ignored but no timing constraints are generated automatically to replace them. This selections will make the Place & Route process run faster, but will not take into account timing constraints while generating the resulting output.

- **Use Bonded I/Os**

  Specifies whether or not PAR places internal I/O logic into bonded I/O sites in which the I/O pad is not used. This option also allows PAR to route through bonded I/O sites.

  Note Before setting this option, ensure this logic is not placed in bonded sites connected to external signals, power or ground.

  By default, this property is set to False (checkbox is blank).

- **Generate Asynchronous Delay Report**

  Specifies whether or not to generate an asynchronous delay report when the PAR process is run. This report contains a list of all nets in the design and the delays of all loads on the net. Run the Asynchronous Delay Report process to view the report.

  By default, this property is set to False (checkbox is blank) and the report is not generated.

- **Generate Clock Region Report (Advanced)**

  Specifies whether or not to generated a clock region report when the PAR process is run. This report contains information on the resource utilization of each clock region and lists any clock conflicts between global clock buffers in a clock region.

  By default, this property is set to False (checkbox is blank) and the report is not generated.

- **Generate Post-Place & Route Static Timing Report**

  Specifies whether or not to generate a post-place & route static timing report which contains a list of calculated worst-case timing for all signal paths in your design. When this property is set, the post-place & route static timing report is generated after the design is placed and routed. To view the report, run the Post-Place & Route Static Timing Report process. The properties settings in the Post-Place and Route Static Timing Report Properties dialog box are applied to the report.

  By default, this property is set to True (checkbox is checked), and the report is generated.

- **Generate Post-Place & Route Simulation Model**

  Specifies whether or not to generate the post-place & route simulation model. When this property is set, the post-place & route simulation model is generated after the design is placed and routed. The property settings in the Simulation Model Properties dialog box are applied to the generated simulation model.

  By default, this property is set to False (checkbox is blank), and the simulation model is not generated.

- **Number of PAR Iterations (0 - 100)**

  Specifies the number of times PAR attempts to place and route signals on your design.

  Note This property is not available for Virtex-5 devices.

  Enter a number from 0 to 100. If you enter 0 (zero), PAR will run until your design either meets timing or all 100 cost tables have been completed, whichever comes first.

  By default, this property is set to 3.

- **Number of Results to Save (0 - 100)**

Specifies the number of NCD files to keep. All results are compared to each other and the best number of NCD files is saved. A score assigned to each output design determines the best outputs.

Note This property is not available for Virtex-5 devices.

By default, this property is blank. You can choose a number from 0 to 100. If you enter 0 (zero), all results are kept.

- **Save Results in Directory (.dir will be appended)**

  Specifies the directory location to which the multi-pass place and route reports will be saved.

  Note This property is not available for Virtex-5 devices.

  By default, this property is set to `mppr_result`. You can enter a directory name of your choice.

- **Nodelist File (UNIX Only)**

  Specifies the Nodelist file that you created. This file allows you to use multiple machine nodes that are networked together to run the place and route process. For more information on generating a nodelist file and setting up environmental tables, see the "Turns Engine (PAR Multi-Tasking Option)" section in the "PAR" chapter of the Development System Reference Guide.

  Note This property is not available for Virtex-5 devices.

  Enter the location and file name of the Nodelist file you created, or click the browse button and browse to the file in the Select dialog box.

- **Power Reduction**

  Specifies whether or not to optimize routing to reduce power consumption. By default, this property is set to False (checkbox is blank), and routing is not optimized for power reduction.

  Note This option will add significant run time to PAR.

- **Power Activity File (Advanced) (Spartan-3, Spartan-3A, Spartan-3E, and Virtex-4 only) (Advanced)**

  This property allows you to specify a simulation file, *.vcd or *.saif, to guide PAR when it optimizes the design for power reduction.

  This file is the output of a simulation run on the design. For power reduction, PAR uses this file to set frequencies and activity rates of internal signals, which are signals that are not inputs or outputs but internal to the design.

  Note Simulation is the most accurate method of determining the exact activity rates. Back-annotated post-place and route simulation provides the best data for determining activity rates since it most closely represents physical implementation.

  By default, this property is blank (no file name).

- **Other Place & Route Command Line Options (Advanced) (Spartan-3, Spartan-3A, Spartan-3E, and Virtex-4 only)**

  Enter additional command line options. Multiple options are separated with a space. The options entered in this property appear first on the command line, before all other property options specified in the graphical user interface. Avoid setting duplicate options.

  For more information about command line options, see the Development System Reference Guide.