ELEC 4320 Homework #1, Fall 2019

Due on Oct.4th

Submission: You can submit softcopy through the course website or hardcopy in the class.

1) Performance Metrics (25 marks)

a) The designer wants to design a circuit to process a set of 2K inputs. One input contains 16bit data. If the pipelined circuit could work at 200MHz frequency, and it takes 10 clock cycles to process the first input and generate the first output. After that, it takes one clock cycle to process one input, what is the total execution time to finish all the data processing and what are the overall throughput and maximum throughput in the unit of bits/second?

b) IC development cost is determined by direct material cost, lead time, salary and quantity. In this problem, we try to decide the best design choice among the three IC design technologies, FPGA, standard cells, and custom design, according to the development cost. Assume the engineer salary is $10k per week, and the other costs for the four design technologies are shown in the table.

Table 1 Parameters for different design technologies

IC	FPGA	6' Std Cell	8' Custom
Lead time	2 weeks	20 weeks	30 weeks
Gates	60k	10k/mm^2	20k/mm^2
Wafer areas	Nil	15000mm^2	24000 mm^2
Cost	$100	$3k/wafer	$6k/wafer
Mast costs	Nil	$200k	$400k

For the quality of 2000 ICs of 50k gates, which design is most cost-efficient? Here assuming that there is a chip area overhead for standard cell and custom design which is 30% of the required chip area for the gates.

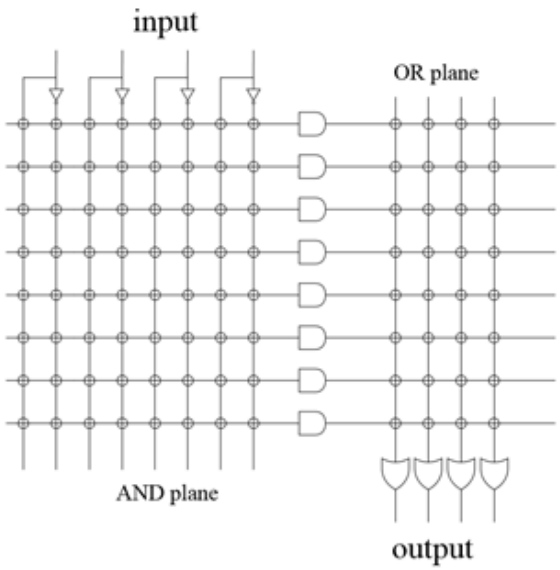
2) HDL programming (50 marks)

Implement the following design using HDL (VHDL or Verilog). Use Xilinx ISE simulator ISIM as in the lab, select the Virtex-5 device (V5-LX110T or V5-LX50T) and verify the functionality. Attach the corresponding code, pre-simulation and post-simulation output waveform showing all your input signals and corresponding output transitions.

a) Implement a 4-bit gray up counter with an input reset pin ‘rst’, an input clock pin ‘clk’ and an output gray code output ‘grayout’.
b) Implement a 4 bit ripple-carry adder with input A[0:3] and B[0:3]. Implement a module first for a full adder and then design the 4-bit adder based on the full-adder module.

3) Logic mapping in PLAs and FPGA (25 marks)

a) Suppose a PLA as shown in the following figure. How many programmable elements are needed in the PLA? Implement the following functions in the PLA using minimum resources: F1 = abc + c'd +abd; F2 = abcd + a'c; F3 = a'c + b'cd + abd



b) Map the Function F = abc + ade + b'd + a'bce to some number of 2-input LUTs, 3-input LUTs and 4-input LUTs. Draw the implementation. How many memory cells are needed for each implementation?