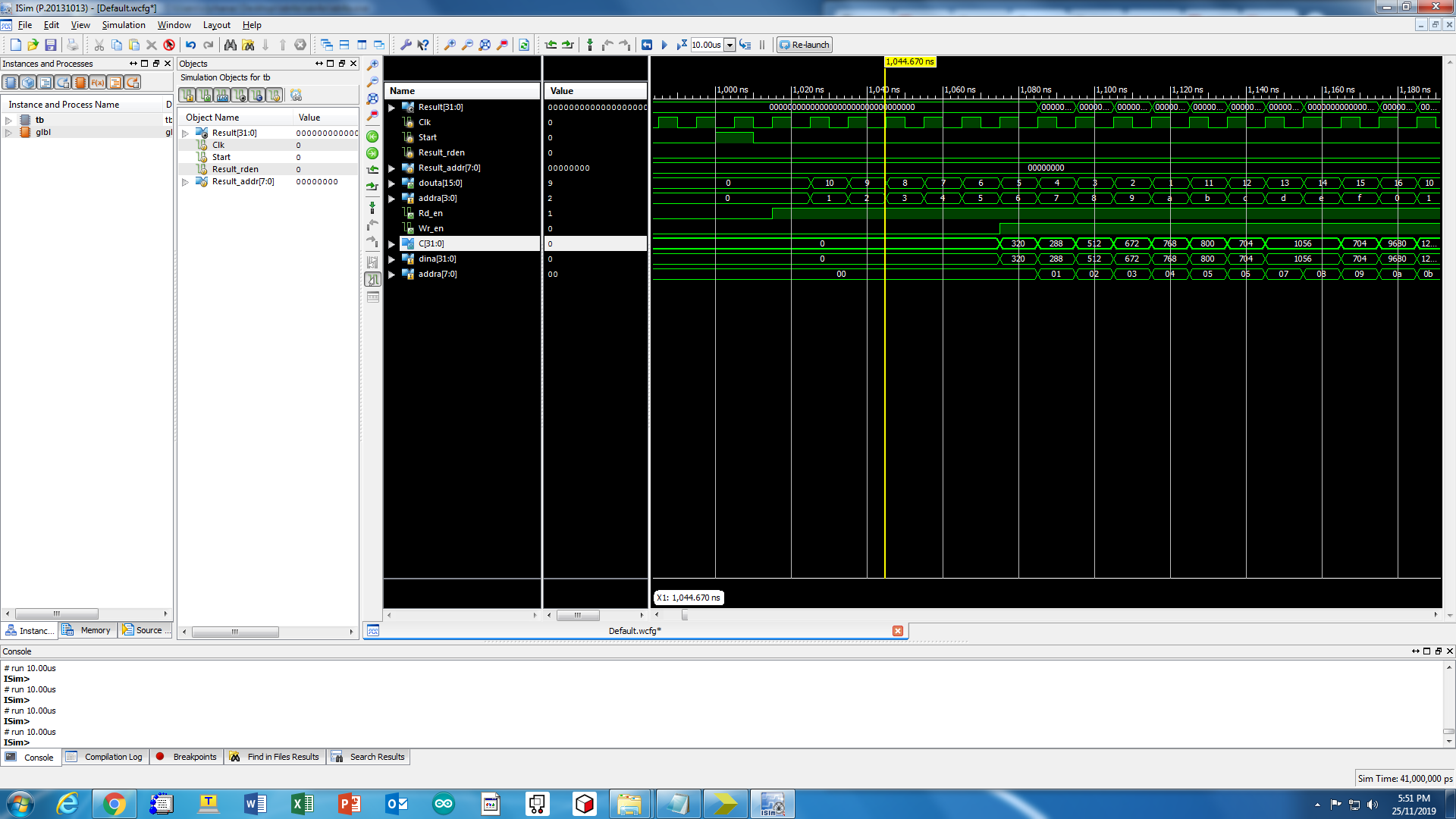
Lab4 – Submission

Chan Chak Lam Jonathan

Lee Lok Yin

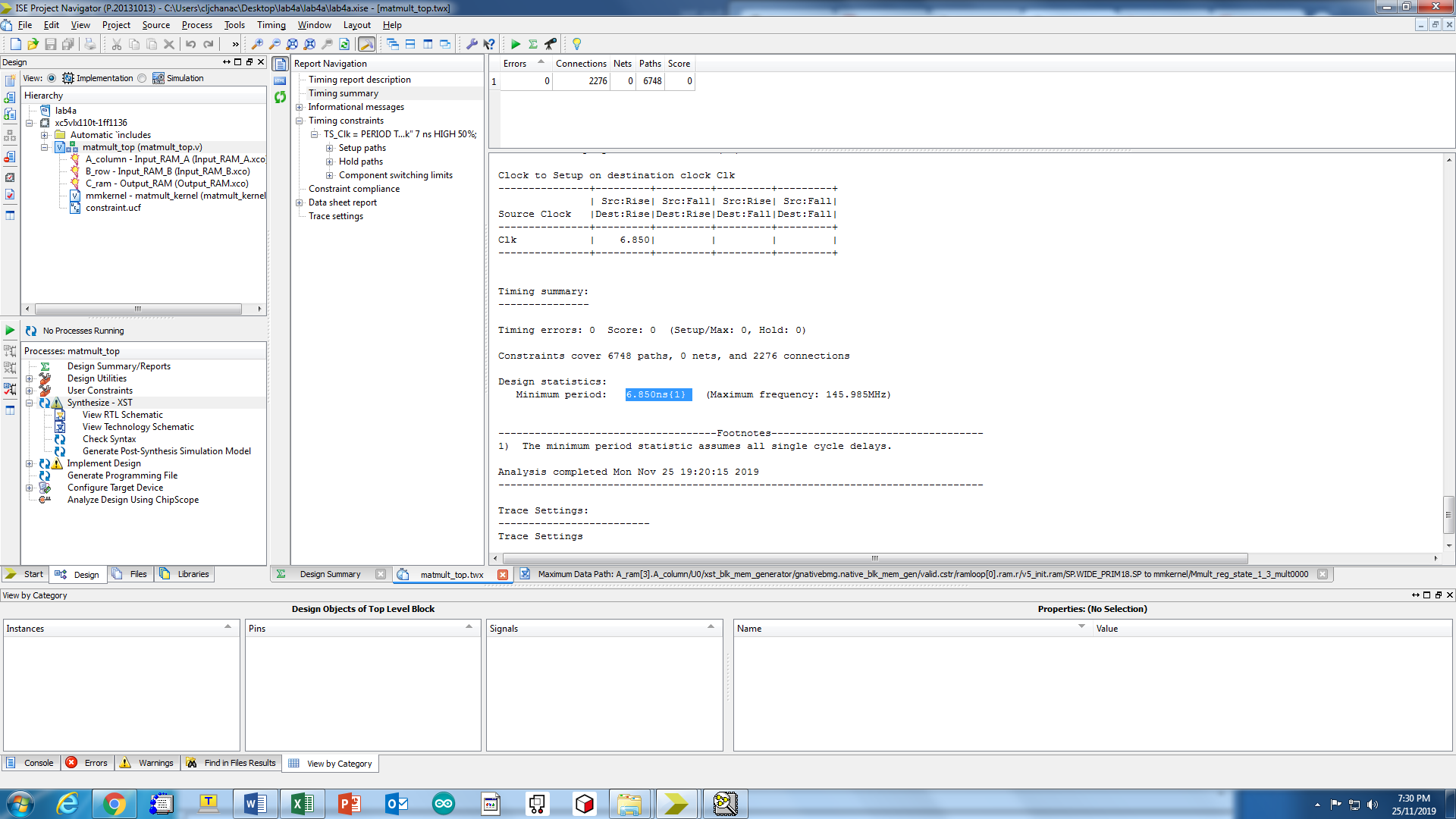
(a)



Task 1 simulation result

Cin is in matmult\_kernel.

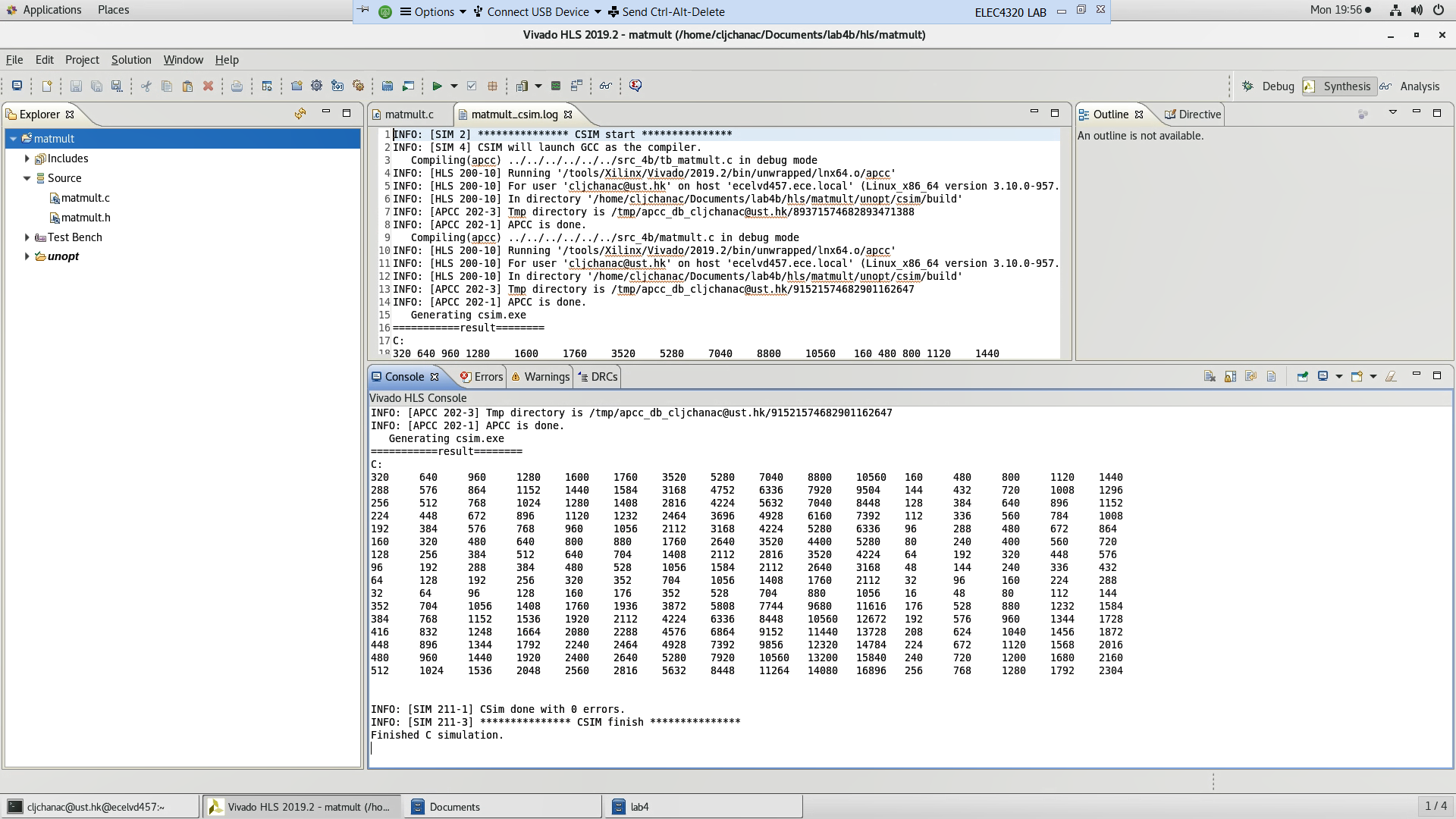
dina is the data input port of C\_ram.



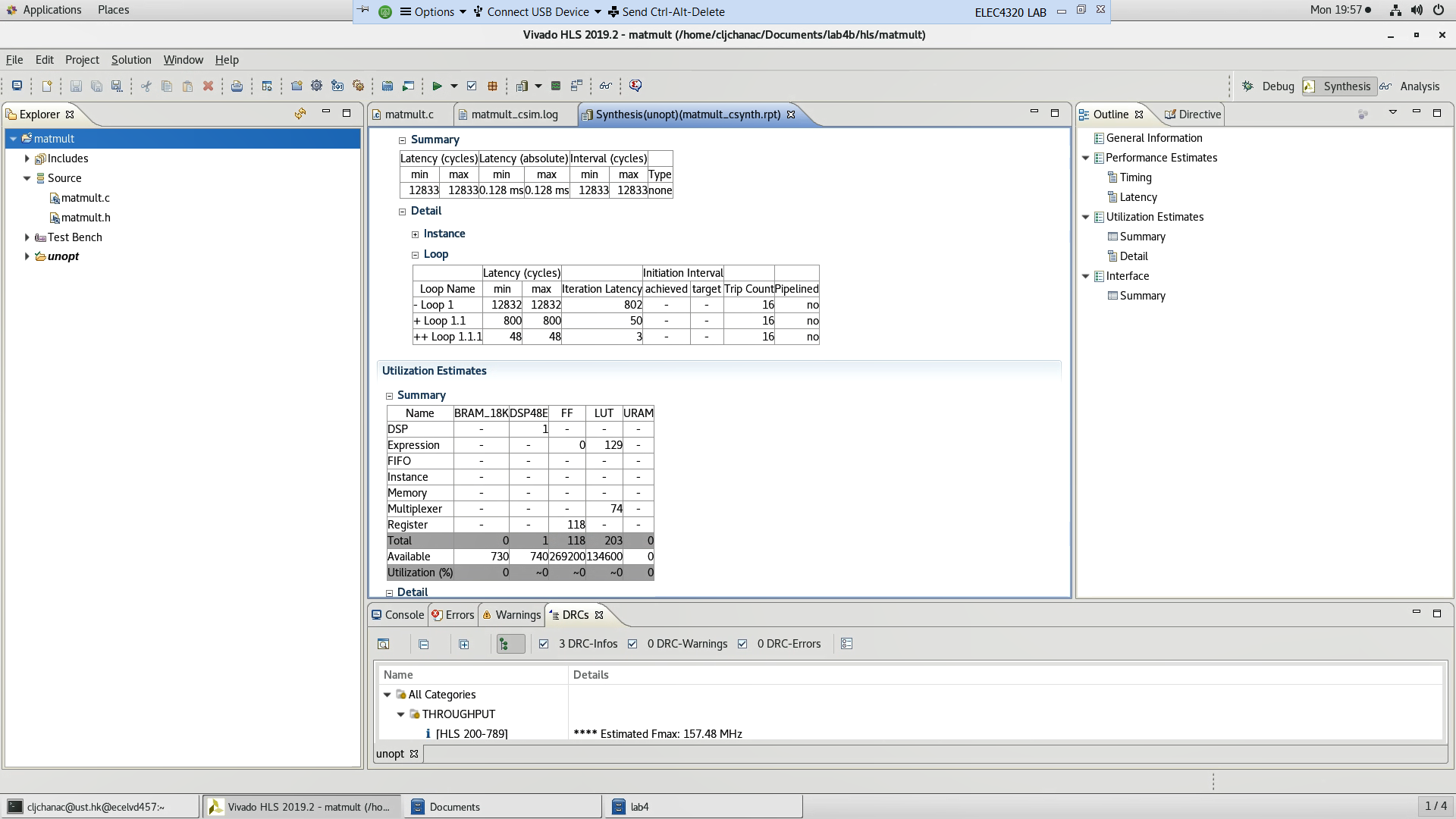
Required >6.85ns, say 7ns at least

Hence, Max frequency is 1/7ns = 143GHz

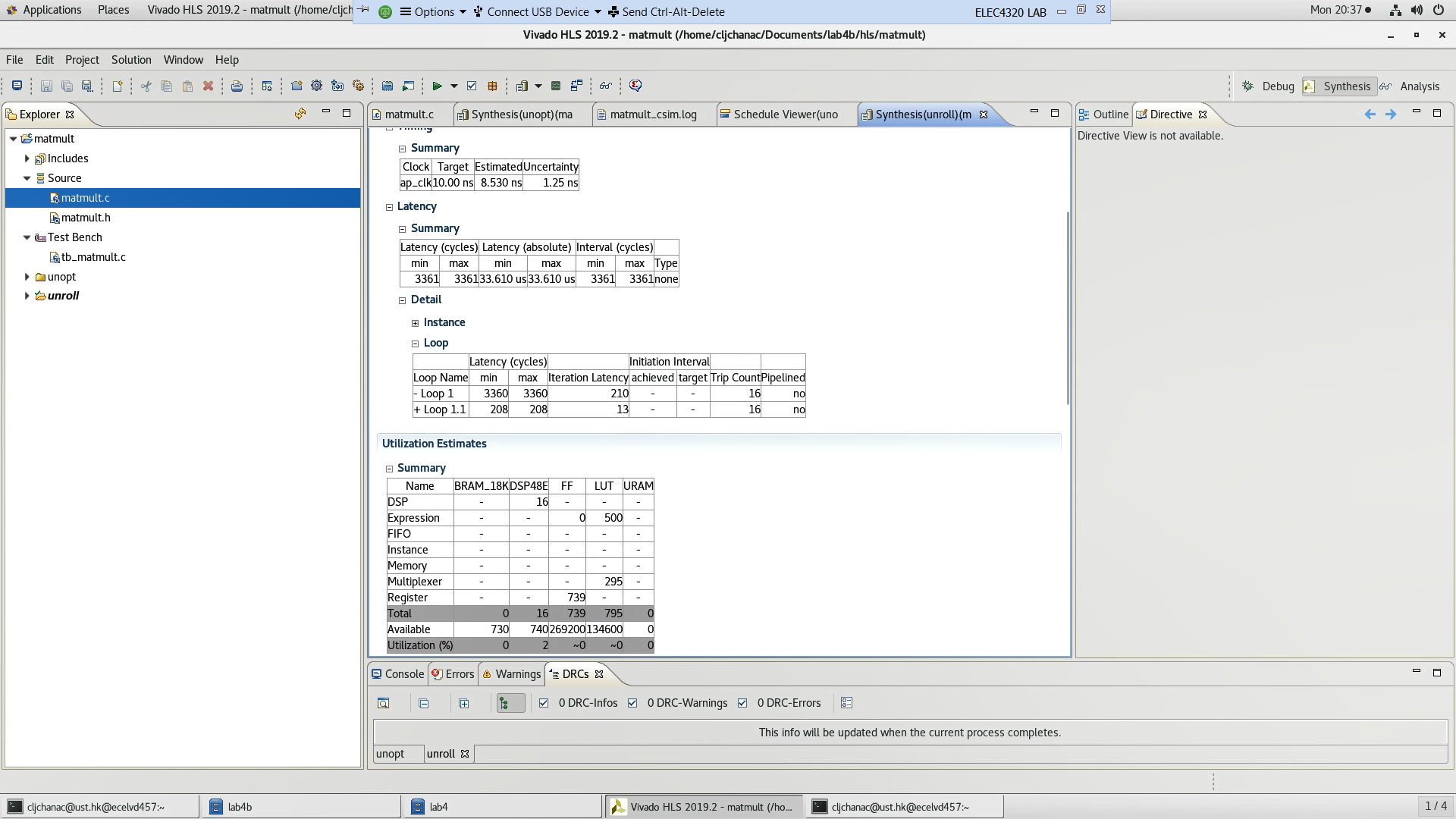
(b)



Normal:



Optimized



IO optimization - faster data exchange, decrease the trace length and better pin assignments

Pipeline – keep every part of the processor executing instruction. In same clock cycle, the unit is executing a sequence of instruction.

Q1. the optimized circuit occupies more resources, including LUT. LUT precomputes some of the output. In general, precomputing more instructions means decrease the need of real-time execution.