SONY

A multi-GNSS receiver

CXD5605GF

Description

The CXD5605GF is a multi-GNSS receiver with a high sensitivity and fast acquisition engine.
The CXD5605GF can operate from a single supply rail from 0.7 V to 1.8 V. Higher supply voltages up to 5.5 V are also possible using a companion PMIC (CXA3846GF). The CXA3846GF has two high efficiency DC-DC converters and very low power RTC (Real Time Clock) and Xtal oscillator.
The CXD5605GF also has integrated digital noise filters and spectrum analyzer, enabling developers to measure against noise and observe the received spectrum in the final product.

Features

- A multi-GNSS receiver for GPS, GLONASS, SBAS, QZSS, BeiDou and Galileo
- Ultra-low power consumption
- Embedded noise filters and spectrum analyzer for development
- Embedded NVM (8 Mbit)

Contents

Package

XFBGA-49Pin (WLCSP)

Structure

Silicon-Gate CMOS IC

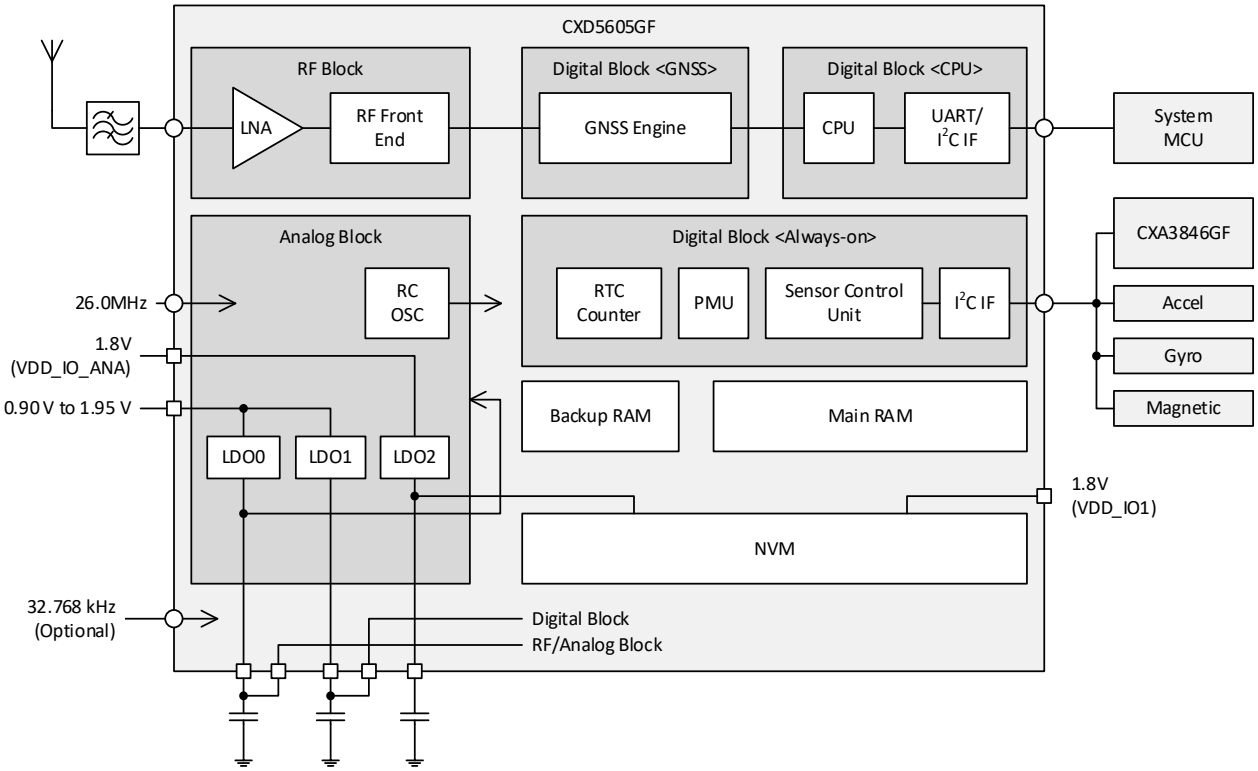
Absolute Maximum Ratings

Item	Min.	Max.	Unit
I/O supply voltage	-0.3	2.5	V
Supply voltage	-0.3	1.4	V
Digital input voltage (except Failsafe Mode)	-0.3	IO supply voltage + 0.3	V
Digital input voltage (Failsafe Mode)	-0.3	2.2	V
RF_IN input power	—	0	dBm
Analog input voltage	-0.3	IO supply voltage + 0.3	V
Storage temperature	-65	150	˚C
Magnetic field strength	—	1400	mT

Recommended Operating Conditions

Item		Min.	Typ.	Max.	Unit	Remarks
I/O supply voltage(VDD_IO0, VDD_IO1, VDD_IO_ANA)		1.71	1.80	1.89	V	
Supply voltage	VDD_CORE, VDDA_LNA, VDDA_LO, VDDA_ANA and LDO0_OUT (as analog blocks input)	0.65	0.70	0.75	V	in a range from -25 ˚C to 85 ˚C
		0.68	0.70	0.75	V	in a range from -40 ˚C to 85 ˚C
	LDO_IN	0.90	—	1.95	V	
Noise level	VDD_IO_ANA, VDDA_LNA, VDDA_LO, VDDA_ANA and LDO0_OUT, LDO_IN	—	—	—	mVpp	Since noise on these power supplies could deteriorate receiver sensitivity, it is preferable to lesser noise level. Please see reference circuits and recommended parts on “CXD5605GF Application Note for Hardware Implementation” for better performance.
Magnetic field strength		—	—	45	mT	In 25 ˚C / 10-year
		—	—	20	mT	In 105 ˚C / 10-year
Operating temperature		-40	25	85	˚C	

Block Diagram



Pin Description

List

Pin#	Pin Name	Type	I/O	IO Power Supply	Reset State	Description
A1	RF_IN	Analog	Input	VDD_IO_ANA	—	GNSS RF signal input
A2	VDDA_LNA	Power	—	—	—	Analog block (LNA) power
A3	VSSA_ANA	GND	—	—	—	Analog blocks GND
A4	VDD_IO_ANA	Power	—	—	—	Analog IO power
A5	P02 / UART0_CTS	Digital	In/Out	VDD_IO0	Hi-Z	UART CTS (Host IF)
A6	P03 / UART0_RTS	Digital	In/Out	VDD_IO0	Hi-Z	UART RTS (Host IF) / RF Mute
A7	VDD_IO0	Power	—	—	—	VDD_IO0 domain IO power
B1	VSSA_LNA	GND	—	—	—	Analog block (LNA) GND
B2	VSSA_LO	GND	—	—	—	Analog block (Local OSC) GND
B3	VDDA_LO	Power	—	—	—	Analog block (Local OSC) Power
B4	VSSA_AIN	GND	—	—	—	Analog IO GND
B5	TEST0	Digital	Input	VDD_IO1	Hi-Z	Tied to GND
B6	P00 / UART0_TXD / I2C0_SCL	Digital	In/Out	VDD_IO0	Hi-Z	UART TX (Host IF) / I2C SCL (Host IF / Slave)

Pin#	Pin Name	Type	I/O	IO Power Supply	Reset State	Description
B7	P01 / UART0_RXD / I2C0_SDA	Digital	In/Out	VDD_IO0	Hi-Z	UART RX (Host IF) / I^2C SDA (Host IF / Slave)
C1	DC_0	Analog	Output	VDD_IO1	—	For TEST Leave floating
C2	VSSA_XOSC	GND	—	—	—	Analog blocks GND
C3	VDDA_ANA	Power	—	—	—	Analog blocks power
C4	P07 / PMIC_INT_IN	Digital	In/Out	VDD_IO1	Hi-Z	TCXO enabler / Interrupt input from CXA3846GF
C5	P05 / EXTLD_IN	Digital	In/Out	VDD_IO0	Hi-Z	Timing signal input (from LTE Modem) / 1PPS out
C6	VSS	GND	—	—	—	Digital block VSS
C7	P04 / INT_OUT	Digital	In/Out	VDD_IO0	Hi-Z	Interrupt output / 1PPS out
D1	V_WL	Analog	In/Out	VDD_IO1	—	For TEST Leave floating
D2	XOSC_IN	Analog	In/Out	VDD_IO_ANA	—	Crystal OSC / Clock input from TCXO
D3	LDO0_OUT	Power	—	—	—	LDO output for analog blocks
D4	P17 / RTC_IRQ_OUT	Digital	In/Out	VDD_IO1	Hi-Z	External LNA enabler / Interrupt output to CXA3846GF
D5	SYSTEM0	Digital	Input	VDD_IO1	Hi-Z	BOOT MODE
D6	SYSTEM1	Digital	Input	VDD_IO1	Hi-Z	BOOT MODE
D7	VDD_IO1	Power	—	—	—	VDD_IO1 domain IO power
E1	LDO2_OUT	Analog	Out	VDD_IO_ANA	—	LDO output for memory core blocks
E2	VSSA_RCOSC	GND	—	—	—	Analog blocks GND
E3	P15 / I2C1_SDA	Digital	In/Out	VDD_IO1	Hi-Z	I^2C SDA (CXA3846GF IF / Master)
E4	P14 / I2C1_SCL	Digital	In/Out	VDD_IO1	Hi-Z	I^2C SCL (CXA3846GF IF / Master)
E5	VSS	GND	—	—	—	Digital block VSS
E6	P06 / BOOT_REC	Digital	In/Out	VDD_IO1	Pull-down	BOOT Recovery (Normally tied to GND) / 1PPS out
E7	VSS	GND	—	—	—	Digital block VSS
F1	LDO_IN	Analog	Input	VDD_IO_ANA	—	LDO0 / LDO1 input
F2	LDO_EN	Analog	Input	VDD_IO_ANA	—	LDO0 / LDO1 enabler
F3	P11 / SPI1_IO1	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO1 / Master)
F4	P12 / SPI1_IO2	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO2 / Master)
F5	P16 / SEN_IRQ_IN	Digital	In/Out	VDD_IO1	Hi-Z	Interrupt input
F6	RST_X	Digital	Input	VDD_IO1	Hi-Z	Reset input
F7	RTC_CLK_IN	Digital	Input	VDD_IO1	Hi-Z	RTC clock input
G1	P13 / SPI1_IO3	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO3 / Master)
G2	P10 / SPI1_IO0	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO0 / Master)

Pin#	Pin Name	Type	I/O	IO Power Supply	Reset State	Description
G3	P09 / SPI1_SCK	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI CLK / Master)
G4	P08 / SPI1_CS_X	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI CS / Master)
G5	LDO1_OUT	Analog	Output	VDD_IO_ANA	—	LDO output for digital block
G6	VDD_CORE	Power	—	—	—	Digital block power
G7	VDD_CORE	Power	—	—	—	Digital block power

Failsafe Mode

Digital pins are in failsafe mode when the interface (VDD_IO0 and VDD_IO1) power is not supplied (VDD_IO1 power must be less than 50 mV. Hi-Z is NOT acceptable), while the core supply (VDD_CORE) may or may not be available. If the pins are in failsafe mode and connected to 1.95 V, protection circuits prevent any unwanted leak current from the pins.

Unused Pin Terminations

LDO1_OUT

The LDO1_OUT should be open if the LDO1 is not used. However, LDO0_OUT should be tied to analog 0.7 V even if the LDO0 is not used.

RTC_CLK_IN

The RTC_CLK_IN should be tied with GND if an external RTC clock isn’t used.

Description of Functions

Support Satellite Systems

- GPS (L1 C/A)
- GLONASS (L1OF)
- QZSS (L1 C/A)
- SBAS (L1 C/A)
- BeiDou (B1)[1]
- Galileo (E1 CBOC)[1]

Position Accuracy

Item	GPS	GPS & GLONASS	Unit	Remarks
2DRMS	1.0	1.0	m	Signal strength is -130 dBm Test circuit is shown at p.19.

Time-To-First-Fix (TTFF)

Item	GPS	GPS & GLONASS	Unit	Remarks
Cold Start[2]	35	35	s	Signal strength is -130 dBm Test circuit is shown at p.19.
Hot Start[3]	2	2	s	

Sensitivity

Item	GPS	GPS & GLONASS	Unit	Remarks
Cold Start	-147	-147	dBm	Test circuit is shown at p.19.
Hot Start	-160	-160	dBm	
Tracking	-161	-161	dBm	

Noise Filter

An embedded noise filter for GNSS signals. It is automatically enabled at the optimum settings for the input noise.

RF Performance

Item	Min.	Typ.	Max.	Unit	Remarks
Total NF	—	3	—	dB	

[1] Planned for the future. Please contact your local sales representative for details.
[2] Positioning start without TCXO bias, GPS time, current location, ephemeris or almanac.
[3] Positioning start with 1) |CXD5605GF internal time – GPS time| < 500 µs, 2) |CXD5605GF internal location - true positioning location| < 50 km, 3) TCXO bias is known, 4) ephemeris is known and 5) any satellite broadcast codes have been decoded.

Internal LDO

Embedded LDOs are provided for each internal power supply block. They should be used if supply voltage is provided by some source other than the CXA3846GF to reduce noise on the supply lines.

LDO0 and LDO1 have same spec as follows.

Item	Min.	Typ.	Max.	Unit	Remarks
Input voltage	0.90	—	1.95	V	Even if the LDOs are not used, LDO_IN must be this input voltage level.
Output voltage	0.68	0.70	0.72	V	

The LDO0 is for analog powers and the LDO1 is for digital block powers.

If the LDOs are not used, the LDO_EN pin must be tied to GND and LDO_IN pin must be tied to VDD_IO_ANA.

LDO2 has spec as follows.

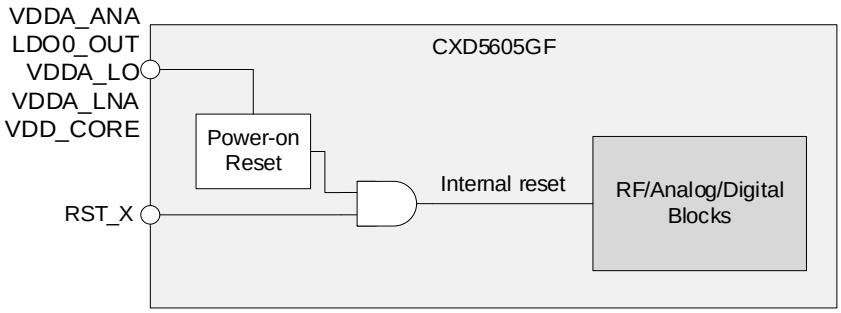
Item	Min.	Typ.	Max.	Unit	Remarks
Input voltage	1.20	—	1.95	V	
Output voltage	0.95	1.00	1.05	V	

The LDO2 is for memory core. This LDO is always ON even if the LDO_EN pin tied to GND.

Power-on reset

An internal power-on reset circuit enables autonomous startup without external reset control by the system. To avoid malfunction in boot-up, power-off state must be more than 100 ms.

The internal reset is generated from the power-on reset & the externa reset (the RST_X pin).



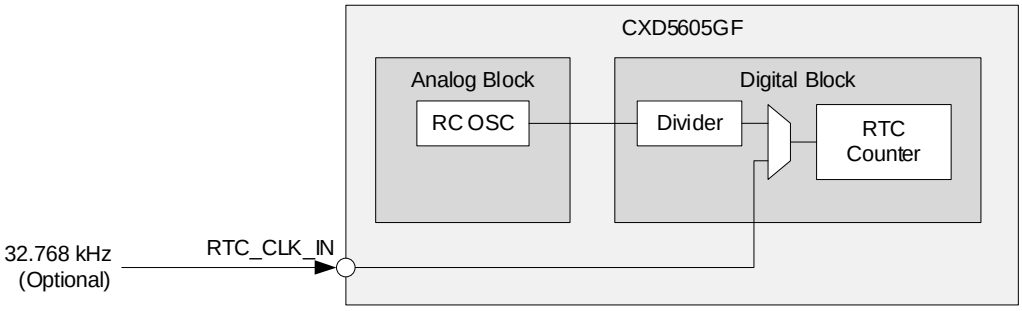
Internal clock oscillators

RC oscillator

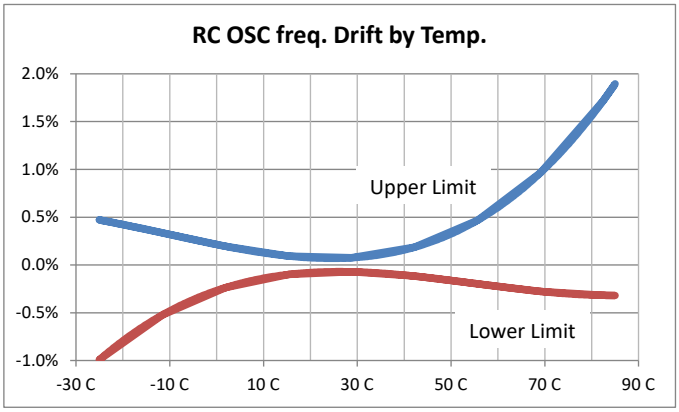
A clock from this oscillator is used for the power management unit and RTC counter (if there is no external RTC clock).

RTC clock

RTC counter maintains GNSS time and is used for the system wakeup/sleep timer function. Its clock sources are the RC oscillator or the RTC_CLK_IN pin with 32.768 kHz.



Because the clock from the RC oscillator is calibrated for the RTC counter but it may have frequency drift by temperature during sleep states (the calibration is done at S0: Exec[4] and S1: Idle states[4]), the sleep time also may be drifted. Below figure shows the frequency drifts by temperature around 25 °C at stabled input voltage.



Interfaces

Host MCU interface

The following are provided as interfaces to the host MCU.

- UART: up to 1.00 Mbps (8-N-1), up to 2.00 Mbps (8-N-2),
- I^2C[5]: Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)

The interface selection is set by the SYSTEM0 and SYSTEM1 pins.

SYSTEM1	SYSTEM0	Selected interface
0	0	I^2C
0	1	UART
1	0	Reserved
1	1	Reserved

CXA3846GF interface

This is an I^2C interface with normal mode and fast mode. It is provided as an interface for the CXA3846GF.

[4] Please see “Description of Operation” at p.10
[5] Planned for the future. Please contact your local sales representative for details.

FLASH memory interface

SPI1 is for an external FLASH memory. The max clock frequency is 39 MHz

1PPS output

A 1PPS (pulse per second) signal is synchronized in the GPS time. P04 / INT_OUT can be used for the 1PPS output.

Recovery pin

When P06/BOOT_REC pin is high at power-on sequence[6], the CXD5605GF doesn't read a firmware on the FLASH memory to over-write it. Please refer to the "CXD5605GF User's Manual" for details.

FLASH memory size

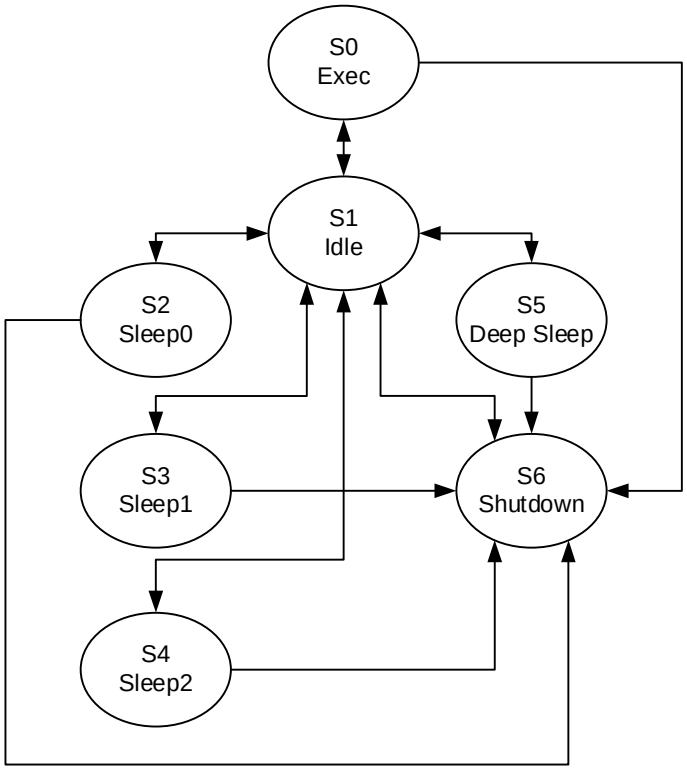
Item	Min.	Typ.	Max.	Unit	Remarks
FLASH memory size	0	—	64	Mb	

[6] See AC characteristics - Power-on / Power-off, p.17

Description of Operation

State Transition

There are some states in the CXD5605GF and the CXA3846GF operations as shown in the following diagram. If the CXA3846GF is not used, the system doesn't go to "S5" or "S6".



State	CXD5605GF					CXA3846GF		
	GNSS	CPU	Always-on block	Backup RAM	Main RAM	CE Pin	RTC Counter	Registers
S0: Exec	Operation	Operation	Operation	Hold	Hold	H	Operation	Hold
S1: Idle	Standby	Operation	Operation	Hold	Hold	H	Operation	Hold
S2: Sleep0	Power-off	Power-off	Operation	Hold	Hold	H	Operation	Hold
S3: Sleep1	Power-off	Power-off	Operation	Hold	Power-off	H	Operation	Hold
S4: Sleep2	Power-off	Power-off	Operation	Power-off	Power-off	H	Operation	Hold
S5: Deep Sleep	Power-off	Power-off	Power-off	Power-off	Power-off	H	Operation	Hold
S6: Shutdown	Power-off	Power-off	Power-off	Power-off	Power-off	L	Off	Off

State Description

S0: Exec

GNSS positioning can be performed.

S1: Idle

This is a command waiting state. The system can accept commands, but power consumption is managed to be low.

S2: Sleep0

The CXD5605GF holds program code, data and satellite date but other logic circuit is powered off. The CXD5605GF can wake up from this state without loading the data from an embedded NVRAM or an external FLASH memory or the system MCU.

S3: Sleep1

Because the CXD5605GF holds satellite data only in this state, it must load program data from an embedded NVRAM or an external FLASH memory or the system MCU for wake-up but it can get a position with hot start.

S4: Sleep2

In this state, the CXD5605GF is powered off except an internal PMU and always-on block.

S5: Deep Sleep

In this state, the CXD5605GF is powered off but the CXA3846GF holds its RTC counter and backup registers.

S6: Shutdown

The CE pin of the CXA3846GF is low in this state. All functions are off but the leakage current is very low.

Please refer to the “CXD5605GF User’s Manual” for details.

Electrical Characteristics

DC Characteristics

Digital IO

Item		Symbol	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH}	0.7 × IO supply voltage	—	IO supply voltage + 0.3	V
	L level	V_{IL}	-0.3	—	0.3 × IO supply voltage	V
Output voltage	H level	V_{OH}	0.8 × IO supply voltage	—	—	V
	L level	V_{OL}	—	—	0.2 × IO supply voltage	V
Drivability (VDD_IO0)	H level @V_{OH}(Min.)	I_{OH}	1.2	—	—	mA
	L level @V_{OL} (Max.)	I_{OL}	1.2	—	—	mA
Drivability (VDD_IO1)	H level @V_{OH}(Min.)	I_{OH}	2	—	—	mA
	L level @V_{OL} (Max.)	I_{OL}	2	—	—	mA
Pull-up/down resistance (VDD_IO0)		R_{PUD}	20	—	50	kΩ
Pull-up/down resistance (VDD_IO1)		R_{PUD}	30	—	70	kΩ
Capacitance		C_{BL}	—	—	5	pF

Analog IO

- LDO_EN

Item		Symbol	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH}	0.8 × IO supply voltage	—	IO supply voltage + 0.3	V
	L level	V_{IL}	-0.3	—	0.3	V

- Except above

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage	V_I	—	—	Recommended operating supply voltage	V
Output voltage	V_O	—	—	Recommended operating supply voltage	V

Current consumption

- Core[7]

Item	State	Symbol	Min.	Typ.	Max.	Unit	Remarks
Max load	—	MAX	—	—	50	mA	
Satellite acquisition	S0: Exec	GNS_{ACQ}	—	15	—	mA	
Satellite tracking		GNS_{TRK}	—	7	—	mA	GPS 8-ch tracking
Idle	S1: Idle	IDLE	—	2	—	mA	Waiting for command

[7] Sum of VDD_CORE, VDDA_LNA, VDDA_LO, VDDA_ANA and LDO0_OUT current

Item	State	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sleep0	S2: Sleep0	SLP_0	—	0.3	3	mA	Temp. in Max. is 25 ˚C
Sleep1, Sleep2 w/ ext. RTC clock	S3: Sleep1, S4: Sleep2	SLP_1, SLP_2	—	40	500	µA	Temp. in Max. is 25 ˚C
Sleep1, Sleep2 w/o ext. RTC clock			—	70			
Deep Sleep[8]	S5: Deep Sleep	DSLP	—	—	0	µA	CXA3846GF cuts all power of CXD5605GF's core
Shut down[8]	S6: Shutdown	SD	—	—	0	µA	

- VDD_IO0 + VDD_IO1

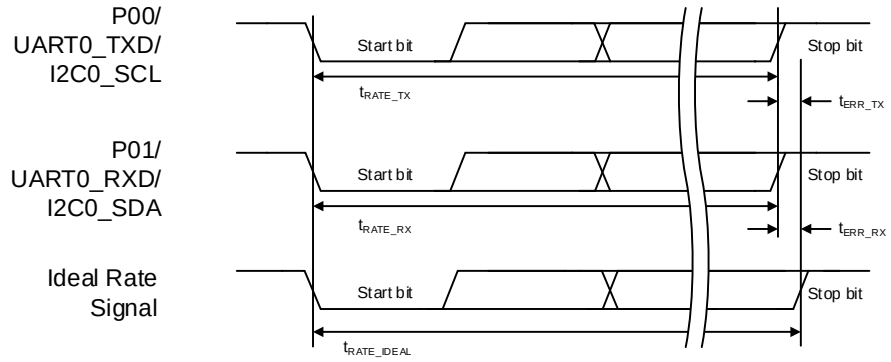
State	Min.	Typ.	Max.	Unit	Remarks
All states except S5, S6	—	30	—	µA	Depends on IO toggling

- VDD_IO_ANA

State	Min.	Typ.	Max.	Unit	Remarks
S0: Exec, S1: Idle	—	170	—	µA	
S2: Sleep0	—	150	—	µA	
S3: Sleep1, S4: Sleep2	—	60	—	µA	

AC characteristics

UART (Host interface)

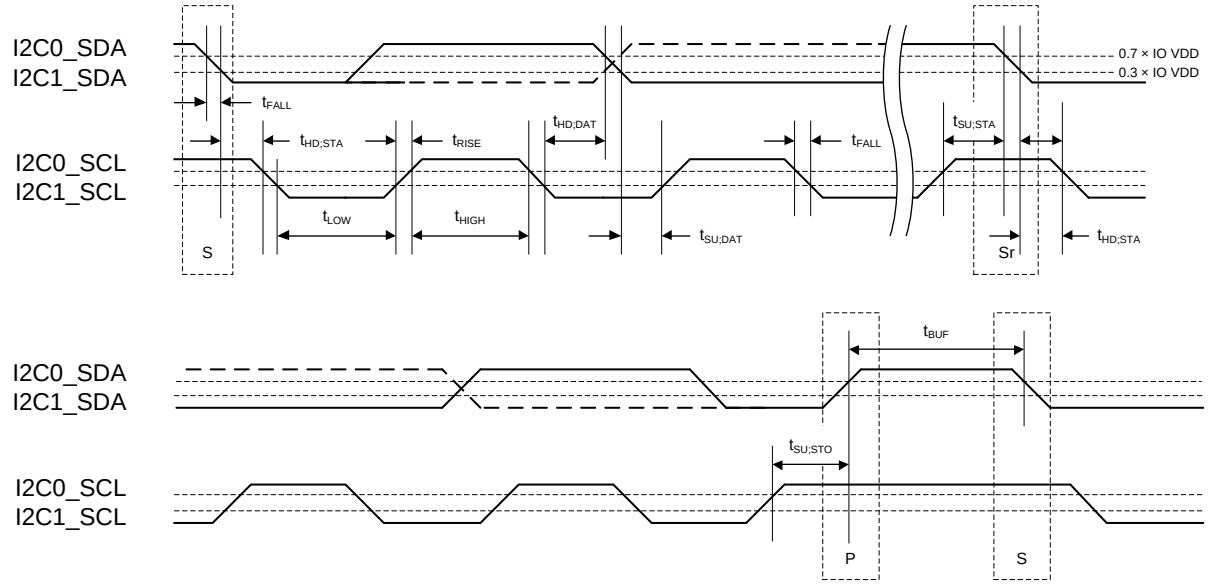


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
UART Error Rate (except TX @ 115.2 kbps)	R_{BRT_ERR}	-1	—	1	%	t_{ERR_TX} / t_{RATE_IDEAL} t_{ERR_RX} / t_{RATE_IDEAL}
UART Error Rate (TX @ 115.2kbps)	$R_{BRT\_ERR\_FD\_TX}$	-4	—	4	%	t_{ERR_TX} / t_{RATE_IDEAL}

These timing budgets are changed by PCB (Printed Circuit Board) design. Please evaluate UART function on your PCB carefully.

[8] Please refer to the CXA3846GF data sheet for the its core current

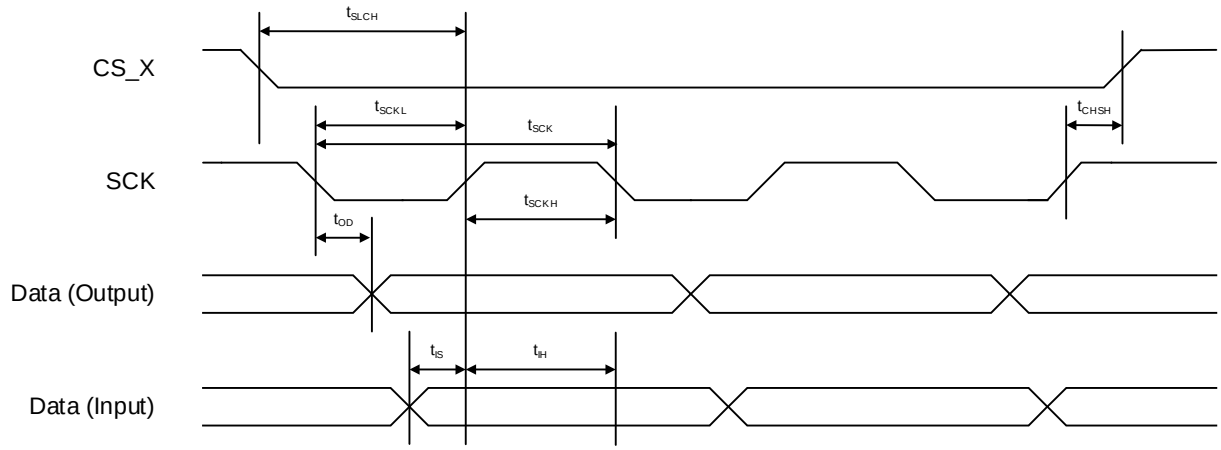
I²C (Host interface and CXA3846GF interface)



Item	Symbol	Standard-Mode		Fast-Mode		Fast-Mode Plus[9]		Unit	Remarks
		Min.	Max.	Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz	—
HOLD time (repeated) START condition	$t_{HD;STA}$	4	—	0.6	—	0.26	—	us	—
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	0.5	—	us	—
LOW period of the SCL clock	t_{HIGH}	4	—	0.6	—	0.26	—	us	—
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	0.26	—	us	—
Data hold time	$t_{HD;DAT}$	0	—	0	—	-	—	us	—
Data setup time	$t_{SU;DAT}$	250	—	100	—	50	—	ns	—
Rise time of both SDA and SCL signals	t_{RISE}	—	1000	20	300	—	120	ns	—
Fall time of both SDA and SCL signals	t_{FALL}	—	300	—	300	—	120	ns	—
Setup time for STOP condition	$t_{SU;STO}$	4	—	0.6	—	0.26	—	us	—
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	0.5	—	us	—
Capacitive load for each bus line	C_L	—	73	—	73	—	29	pF	4.7 kΩ Pull-up

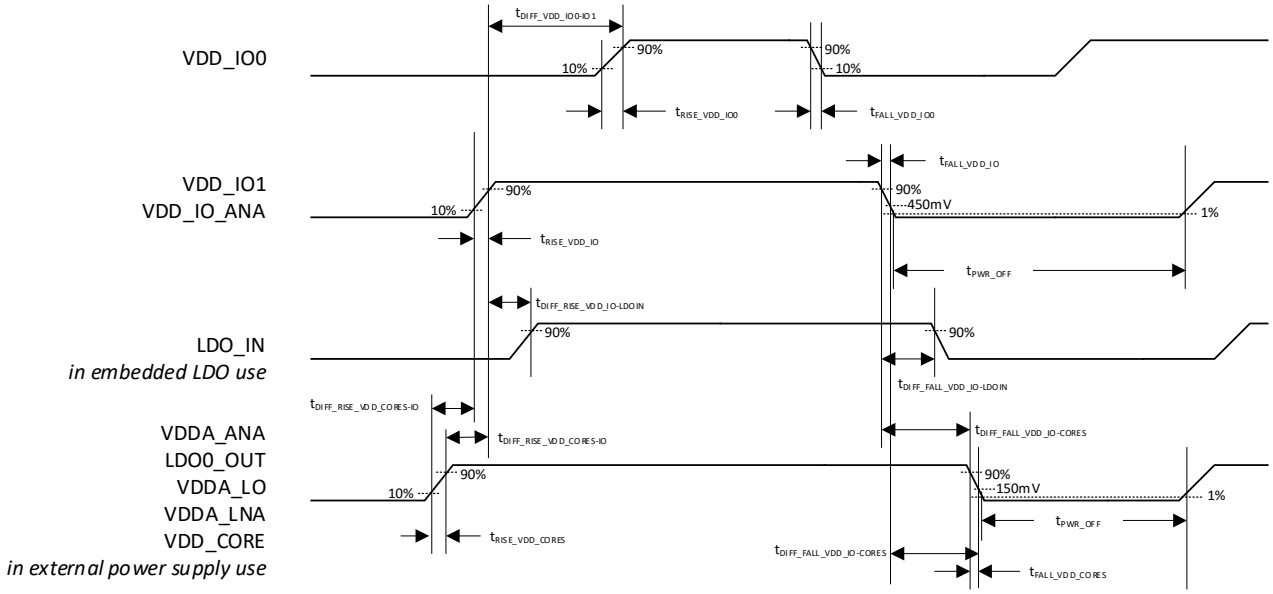
[9] Host Interface only

External FLASH memory interfaces



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK Period	t_{SCK}	—	30.5	—	ns	33 MHz
SCK Duty Ratio	t_{SCKH} / t_{SCK} (t_{SCKL}/t_{SCK})	40	50	60	%	—
CS_X active setup time	t_{SLCH}	7	—	—	ns	—
CS_X active hold time	t_{CHSH}	5	—	—	ns	—
IO Output Delay Time	t_{OD}	-10.36	—	12.86	ns	—
IO Input Setup Time	t_{IS}	0	—	—	ns	—
IO Input Hold Time	t_{IH}	15.36	—	—	ns	—

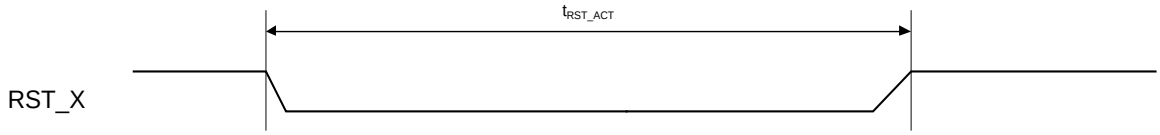
Power-on / Power-off



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Time difference from VDD_IO1 and VDD_IO_ANA rise to VDD_IO0	$t_{DIFF\_VDD\_IO0-IO1}$	—	—	—	ms	—

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
VDD_IO0 rise time	$t_{RISE\_VDD\_IO0}$	—	—	—	ms	—
VDD_IO0 fall time	$t_{FALL\_VDD\_IO0}$	—	—	—	ms	—
Power off period	t_{PWR_OFF}	100	—	—	ms	—
VDD_IO1 and VDD_IO_ANA rise time	$t_{RISE\_VDD\_IO}$	—	—	—	ms	—
VDD_IO1 and VDD_IO_ANA fall time	$t_{FALL\_VDD\_IO}$	—	—	500	ms	—
Time difference from VDD_IO1 and VDD_IO_ANA rise to LDO_IN rise	$t_{DIFF\_RISE\_VDD\_IO-LDOIN}$	-5	—	1	ms	VDD_IO1 and VDD_IO_ANA can rise earlier than LDO_IN by 1ms
Time difference from VDD_IO1 and VDD_IO_ANA fall to LDO_IN	$t_{DIFF\_FALL\_VDD\_IO-LDOIN}$	0	—	10	ms	LDO_IN should fall later than VDD_IO1 and VDD_IO_ANA
Time difference from VDD Cores[10] rise to VDD_IO1 and VDD_IO_ANA rise	$t_{DIFF\_RISE\_VDD\_CORES-IO}$	0	—	10	ms	VDD Cores should rise earlier than VDD_IO1 and VDD_IO_ANA
Time difference from VDD_IO1 and VDD_IO_ANA fall to VDD Cores fall	$t_{DIFF\_FALL\_VDD\_IO-CORES}$	0	—	10	ms	VDD Cores should fall later than VDD_IO1 and VDD_IO_ANA
VDD Cores rise time	$t_{RISE\_VDD\_CORES}$	0.08	—	4.00	ms	Keep monotonically increasing
VDD Cores fall time	$t_{FALL\_VDD\_CORES}$	—	—	—	ms	Keep monotonically decreasing
POR activating voltage	V_{POR_ACT}	—	—	500	mV	

Reset



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
RST assert period	t_{RST_ACT}	100	—	—	ms	—

Clocks

- XOSC_IN

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}	0.8	—	1.4	Vpp

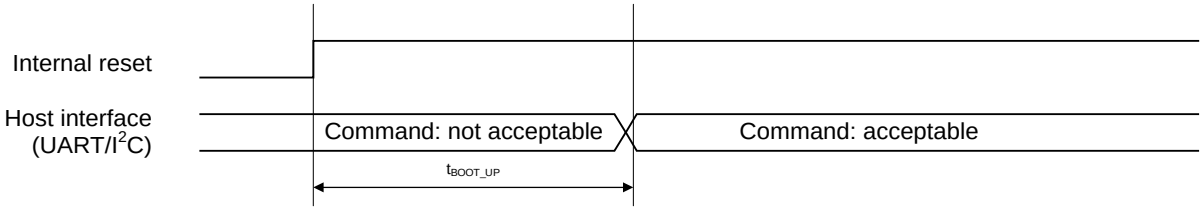
[10] VDDA_LNA, VDDA_LO, VDDA_ANA, LDO_OUT0 and VDD_CORE

Input Frequency	F_{IN}	—	26.0	—	MHz
Input frequency characteristics	F_{IN_C}	-0.5	—	0.5	ppm
Duty Cycle	D_C	40	—	60	%

- RTC_CLK_IN

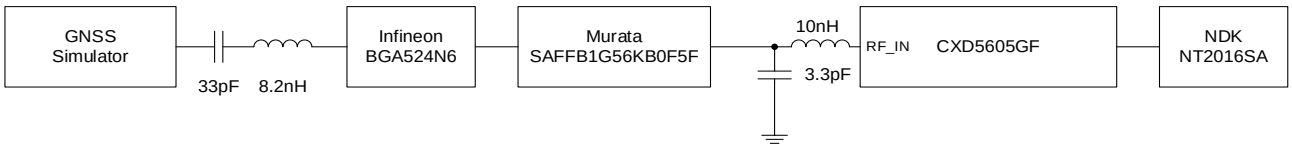
Item	Symbol	Min.	Typ.	Max.	Unit
Input Frequency	F_{IN}	—	32.768	—	kHz
Frequency Tolerance	F_{IN_T}	-300	—	300	ppm
Duty Cycle	D_C	5	—	95	%

Boot-up



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Time to accept commands from the system reset asserting	t_{BOOT_UP}	—	—	1000	ms	

Test Circuit



Reliability Qualification

ESD Strength

- CDM: ±250 V (JEDEC)
- HBM: ±2000 V (JEDEC)

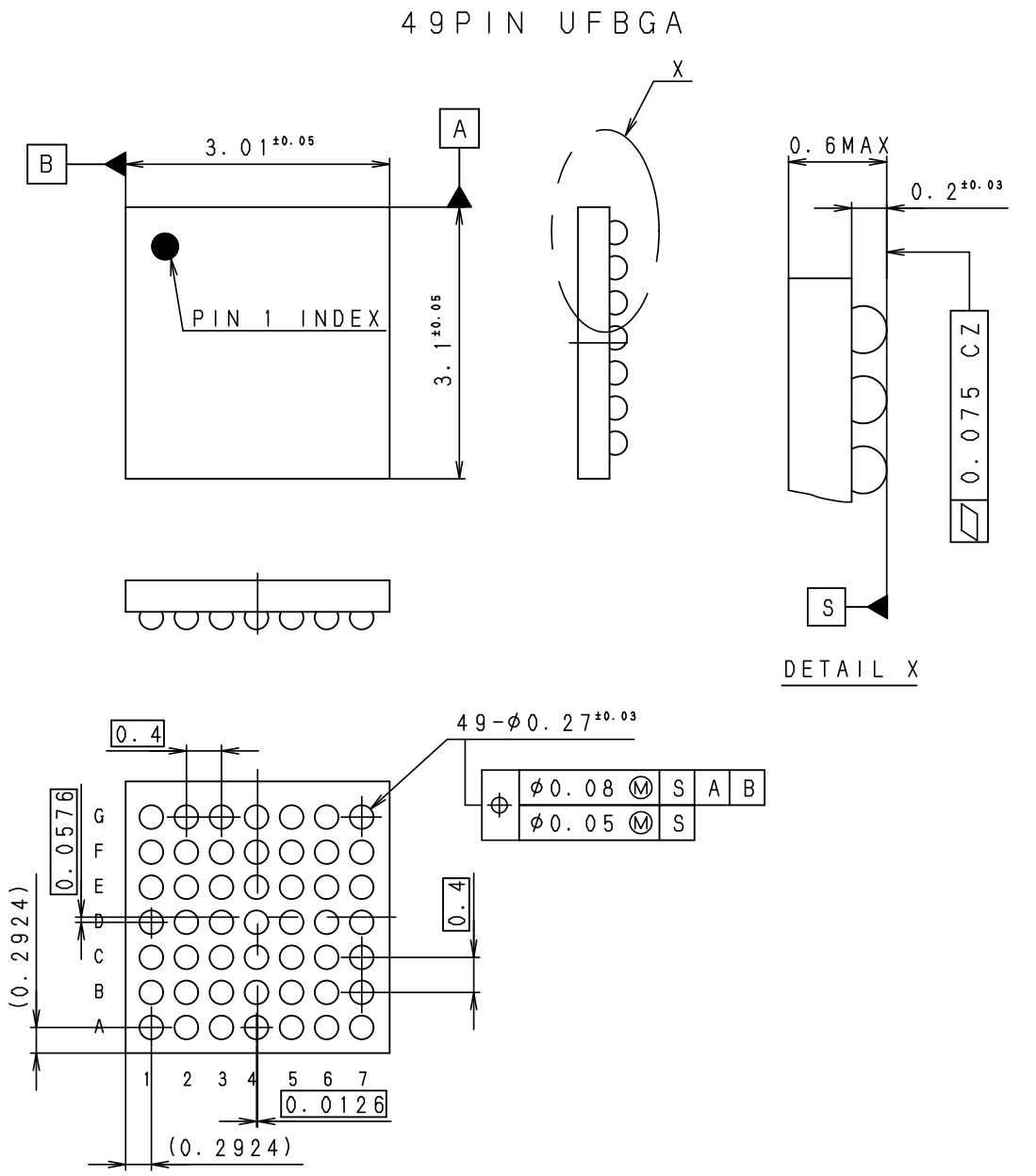
Moisture Sensitivity Level

MSL1 (JEDEC)

Reflow Profile

IPC/JEDEC J-STD-020

Package Outline



PACKAGE STRUCTURE

SONY CODE	UFBGA-49S-312
JEITA CODE	S-UFBGA49-3.01x3.1-0.4
JEDEC CODE	————

PACKAGE MATERIAL	Si SUBSTRATE
TERMINAL MATERIAL	Sn-4.0Ag-0.5Cu-3.0Bi
PACKAGE MASS	0.011g

PART No. AP-2000-49BGAF2	Rev. 0
ISSUED '19.03.07	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR MANUFACTURING.
REMARKS PKG CODE:GM-49-WAF	

Purpose of Use of the Products:

Customer shall use the Products with the utmost concern for safety, and shall not use the Products for any purpose that may endanger life or physical wellbeing, or cause serious damage to property or the environment, either through normal use or malfunction.
Use of the Products for purposes other than those stipulated in this specification is strictly prohibited.
Furthermore, usage of the Products for military purposes is strictly prohibited at all times.

Safe Design:

- Customer is responsible for taking due care to ensure the product safety design of its products in which the Products are incorporated, such as by incorporating redundancy, anti-conflagration features, and features to prevent mis-operation, in order to prevent accidents resulting in injury, death, fire, or other social damage as a result of failure.

Product Information:

- The product specifications, circuit examples, and any and all other technical information and content contained in this specification, as well as any other information and materials provided to Customer in connection with the Products (collectively, “Product Information”) have been provided to Customer for reference purpose only, and the availability and disclosure of such Product Information and its usage by Customer shall not be construed as giving any indication that Sony, its subsidiaries and/or its licensors will license any right, including intellectual property rights in such Product Information by any implication or otherwise.
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- Customer shall comply with all applicable laws, ordinances, rules and regulations in connection with the usage of the Products, including the export control laws or regulations of various countries and shall be fully responsible for obtaining approvals in connection with the export of the Products in accordance with such said laws, ordinances, rules and/or regulations.

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- This specification and the terms and conditions contained herein shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this specification and the terms and conditions contained herein shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

Notes:

- The product specifications, circuit examples, technical information and any and all other information and content relating to the Products contained in this specification may be revised or updated by Sony at Sony's sole discretion without prior notice to the Customer and Customer shall abide by their latest versions. Such revisions or updates will be made available to Customer in a way as Sony deems appropriate.
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