FPGA implementation of an optimal IGBT gate driver based on Posicast control

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***Abstract*—In this paper, we propose an IGBT gate driver that provides an optimal gate signal to manage the IGBT switching mechanism, without the need of a feedback current measurement across the parasitic inductance of the circuit. Our approach is based on the Posicast method, which allows determining an optimal gate signal shape from pulses whose characteristics are determined from the IGBT model. Experimental results demonstrate the effectiveness of the proposed method to minimize electrical switching constraints.**

***Index Terms*—Power semiconductor switches, Driver circuits, Field programmable gate arrays, Optimization methods, Power conversion**

I. NOMENCLATURE

L_p	Total Parasitic inductance of the IGBT module
R_p	Total Parasitic resistance of the IGBT module
V_{cc}	Gate voltage supply
v_{ge}	Gate voltage applied to the IGBT
v_{ge}^{i}	Internal gate voltage of the IGBT
$V_{ce,\,m}$	Turn-off V_{ce} voltage of the IGBT
$V_{ce,\,\delta}$	Peak voltage of V_{ce} when turning off
$V_{ge,\,th}$	Internal gate threshold voltage
i_c	Collector current of the IGBT
$t_{ge,\,off}$	Instant of controlled turn-off
$t_{ge,\,th}$	Instant of effective turn-off when $v_{ge} < V_{ge,\,th}$

II. INTRODUCTION

The main purpose of an IGBT gate driver is to optimize the switching performances of power electronics components. Several factors are important to consider when designing an IGBT driver [1], including wiring inductance, protection against short circuit and faults [2] and overvoltage due to turn-off. The effect of the temperature on the switching conditions has been also studied [3]. Classical gate drivers generally use the principle of a resistor gate network [4] controlled by complex sequential algorithms that detect critical voltage changes in the switching process. Recent work reported in [5] [6] describes a driver with a control loop, which uses high speed operational amplifiers. To the best of the authors' knowledge, published techniques, which mainly focus on the minimization of $\mathrm{d}v_{ce}/\mathrm{d}t$ (or $\mathrm{d}i_c/\mathrm{d}t$) [7], need collector current sensing with a very high bandwidth [8], which results in high sensitivity to electromagnetic field due to the driver itself, parasitic inductances [9] and the switching current. An advanced IGBT driver that provides a solution to the previous limitations has been proposed in [10] [11]. It uses a ramp generator to drive the IGBT, whose slope is calculated from data-sheet-based IGBT parameters. Although no direct feedback is needed, the slope has a constant value regardless of the switching current, which depends on the load.

In this paper, we introduce a new feedforward control of the IGBT turn-off dynamics based on the gate voltage shaping method [10] using a 100 MHz-FPGA device that overcomes some of the previous limitations. In particular, the oscillations created during the IGBT turn-off are known as a critical factor of the turn-off [7] and therefore parasitic inductances are an important parameter to consider when designing an IGBT driver [1]. Results obtained on a laboratory-scale 100 W buck converter are also presented at the end of the paper to demonstrate the validity of this new IGBT driver, hereafter called Posicast IGBT driver.

This paper is structured as follows. Section II reviews the Posicast method. Section III discusses the modeling of the IGBT and its electrical environment, and Section IV describes the Posicast method applied to the IGBT model. The experimental set-up and experimental results are described in Section V, and Section VI concludes the paper.

III. REVIEW OF THE POSICAST METHOD

Introduced in [12] and further developed in [13] [14] with applications in power electronics [15] [16], Posicast control, which is assimilated to a bang-bang control [17] composed of "control levels", constitutes an elegant solution to eliminate oscillations created in second order systems with step inputs. The "control level" refers to the set of discrete levels used in the bang-bang control. To illustrate the principle of the Posicast control, consider a lightly-damped second order system $\Sigma(u \mapsto y)$ with unit gain, whose unit step response is depicted in Fig. 1. The parameters δ and T_d, which are respectively the overshoot and the period of the damped oscillation, are required to design a Posicast controller.

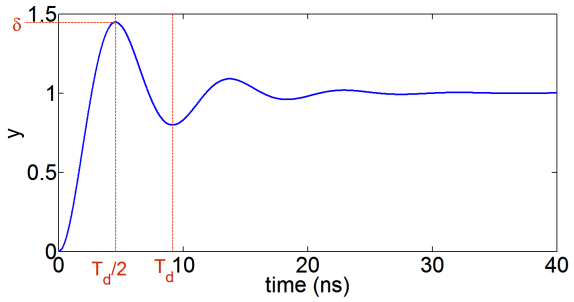


Figure 1. Unit step response of the system Σ.

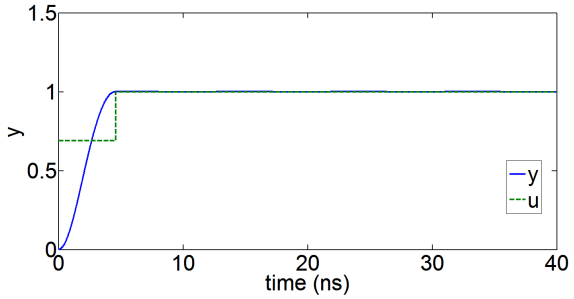


Figure 2. Unit step response of the system Σ with Posicast control.

Its purpose is to reshape the original reference in order to cancel the resonance during the transients of Σ. The reshaped signal is composed of two control levels. The first segment of the control signal $(0 \leq t < t_d/2)$ anticipates the system overshoot by decreasing the level of the reference such that the peak value of y coincides with the final desired asymptotical value. The second segment of the control signal $(t \geq t_d/2)$ is the level of the reference, which stabilizes the output at the desired value. Figure 2 presents the unit step response of Σ with Posicast control. This method defines a feedforward compensation [18] [19] and has been also used as a time-optimal control under constraints .

In [20] an IGBT gate driver is based on the original Posicast method is presented. In particular, during the turn-off, a specific control level is defined to minimize the $\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ (to damp resonances). This method requires an on-line detection of the switching conditions on v_{ce} in order to define precisely, using a specific digital circuit, the timing and the level of the pulse that will damp the oscillations. The pulse level is adjusted using a voltage divider. In [8], an integrated solution that requires an on-line detection of the Miller plateau and a dedicated digital circuit is presented.

IV. Behavior of the IGBT turn-off

Let's consider the turn-off of the IGBT under hard switching conditions. To realize the Posicast IGBT driver, we need to model the IGBT turn-off transients considering its electrical environment.

Figure 3 presents the electrical environment of the IGBT, which is modeled by a wiring resistor R_p and a wiring inductance L_p. According to [9], a single parasitic inductance can be used to represent the total parasitic inductances of the circuit. C_x is the equivalent output capacitor of the IGBT. Figure 4 presents the associated waveforms during the turn-off [20]. V_{ce} is the collector-emitter voltage across the IGBT. V_{ae} is defined as an "extension" of the V_{ce} voltage including the parasitic elements (R_p and L_p). $V_{ce,m} = \max|V_{ce}|$ is the maximum voltage seen by the IGBT in the blocking state.

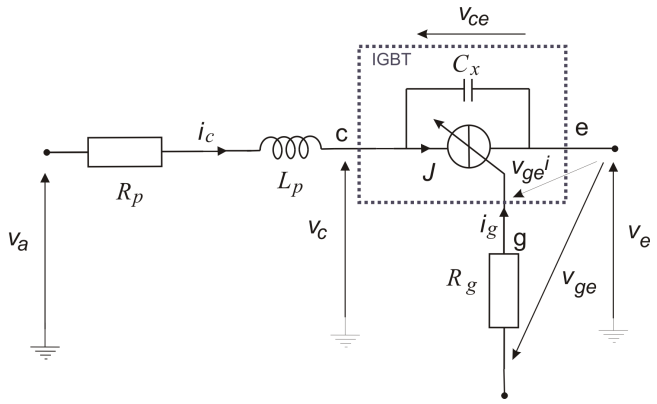


Figure 3. Modeling of the electrical environment of the IGBT.

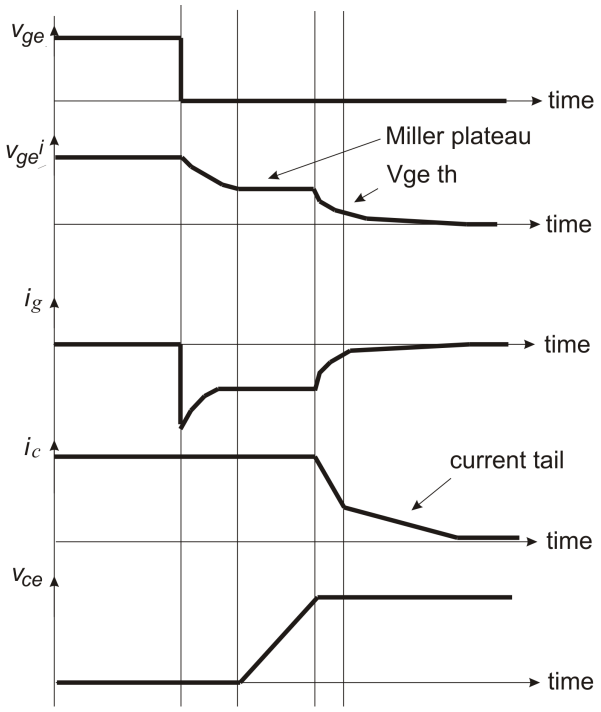


Figure 4. Waveforms of the IGBT turn-off.

When conducting, the IGBT is equivalent to a current source controlled by $v_{ge} \geq V_{ge,th}$. To turn off the IGBT and bring i_c down to zero, the necessary condition is that $v_{ge} < V_{ge,th}$.

When not considering R_p and L_p, it is possible to use the Hammerstein decomposition to model the turn-off behavior of the IGBT, which leads to the first order system in terms of i_c presented below. In particular, i_c is described as a first order system with input v_{ge}.

$$\begin{cases} v_{ge} \geq V_{ge,\,th}, & \frac{\mathrm{d}i_c(t)}{\mathrm{d}t} + q i_c(t) = f_{NL}(v_{ge}(t)) \\ v_{ge} < V_{ge,\,th}, & i_c(t) \to 0 \end{cases} \quad (1)$$

where $1/q$ is a time-constant that depends on the gate resistance and the inter-electrodes capacitors of the IGBT; this constant may be experimentally characterized [21] [22]. The function f_{NL} is a non-linear function that describes the static $i_c - v_{ce}$ characteristic. The function f_{NL} can be assimilated to the continuous equations proposed in [23]. To establish the Posicast IGBT model, we linearize f_{NL} around a particular v_{ce0} voltage to simplify the Hammerstein model. As a result, we can consider that $i_{cp} = g_p v_{ge0}$ for this particular operating point so that f_{NL} is represented by gain g_p.

When turning-off, v_{ge} decreases quickly to 0 V. v_{ge}^i decreases more slowly than v_{ge} due to the internal capacitors and i_c decreases according to (1). At time $t_{ge,\,th}$, $v_{ge}^i = V_{ge,\,th}$ and $i_c = i_{c,\,th}$; it means that when $v_{ge} \approx v_{ge}^i = V_{ge,\,th}$, then i_c is close to its conduction threshold, $i_c = i_{c,\,th}$. Finally, when $v_{ge} = V_{ge,\,th}$, the IGBT turns off and $i_c \to 0$ implies that $v_{ce} \to V_{ce,\,m}$:

$$v_{ae} - R_p C_x \frac{\mathrm{d}v_{ce}(t)}{\mathrm{d}t} - L_p C_x \frac{\mathrm{d}^2 v_{ce}(t)}{\mathrm{d}t^2} - v_{ce} = 0 \quad (2)$$

From (1) and (2), we can conclude that, during the turn-off, i_c decreases first with a certain delay according to v_{ge} (1), and then, as soon as $v_{ge} < V_{ge,\,th}$, the current decreases quickly and forms a current tail [24], whereas v_{ce} evolves to $V_{ce,\,m}$ as the second order system described by (2).

V. Posicast method applied to IGBT turn-off control

The purpose of the Posicast method applied to the IGBT turn-off is therefore to damp the resulting oscillations on v_{ce} that occur when $v_{ge} < V_{ge,\,th}$. However, because of the IGBTs' turn-off process, the classical Posicast control presented in section I must be adapted to avoid usage of v_{ge} level adjustment with IGBTs.

In this section, we propose a modification of the Posicast control such that the adjustment of the control levels is in time rather than in amplitude. The original Posicast method is composed of two discrete control levels (see Section II) and our proposed Posicast method is composed of two binary levels 0 or $+V_{cc}$, for which a specific adjustment in time is required. As a result, we minimize the $\mathrm{d}i_c/\mathrm{d}t$ rate using defined pulses on v_{ge}. Thus, when $v_{ge} < V_{ge,\,th}$, the current i_c decreases quickly but induces a resonance on v_{ce}. Finally, turning on again the IGBT for a very short time can damp the resonance on v_{ce}. The timing for the v_{ge} signal is as follows:

- for $t_{ge,\,th} < t < t_{q1}$, $v_{ge}(t) = 0$;
- for $t_{q1} < t < t_{q2}$, $v_{ge}(t) = V_{cc}$;
- for $t_{q2} < t$, $v_{ge}(t) = 0$,

t_{q1} and t_{q2} define the Posicast pulse, and for a given t_{q1}, t_{q2} values, it verifies:

$$\left.\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}\right|_{t=t_{q2}} = 0, \qquad v_{ce}(t_{q2}) = V_{ce,\,m} \quad (3)$$

To illustrate the proposed concept, consider a second order "generic" system $\Sigma(v_{ge}^* \mapsto v_{ce})$. This system reproduces mathematically the response of the resonant v_{ce} according to (2) as a function of the control input v_{ge}^*.

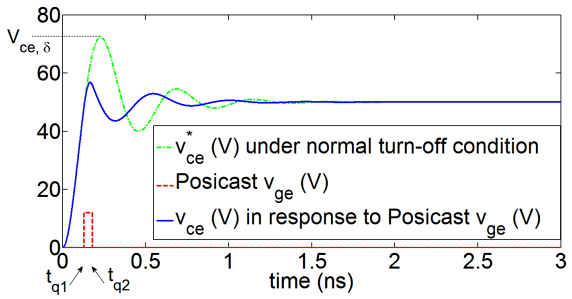


Figure 5. Example of oscillations cancellation on v_{ce} using Posicast.

Voltage v_{ce} corresponds to the response to the illustrated Posicast v_{ge} (Fig. 5) and the voltage v_{ce}^* is obtained under a typical turn-off condition (down-step of v_{ge}^* during the turn-off), also called standard turn-off. In case of a straight turn-off, the gate capacitor C_{ge} is discharged through a short-circuit to maximize the $\mathrm{d}i/\mathrm{d}t$, at the expense of a large overshoot.

In standard conditions, when $v_{ge} < v_{ge,\,th}$, the i_c current goes down to 0 and v_{ce}^* increases and stabilizes to $V_{ce,\,m}$; this corresponds to the effective turn-off phase. In the Posicast condition, when v_{ce} is close to $V_{ce,\,m}$, we turn on again the IGBT for a brief period to cancel the overshoot.

The voltage v_{ge} that corresponds to a Posicast sequence is called v_{ge} P-optimal. The term "optimal" is referred to as the minimization of $V_{ce,\delta}$.

VI. Experimental evaluation of the Posicast IGBT driver

The purpose of the Posicast IGBT driver is to minimize the voltage overshoot on the v_{ce} voltage during the IGBT turn-off. In order to validate the ability of the Posicast gate driver to reduce voltage overshoots upon turn-off, a small-scale power converter (buck-type) was assembled according to Fig. 6.

We used an International Rectifier IRG4IBC20W IGBT. A FPGA development board (Xilinx® / Virtex™-II Pro) running at 100 MHz was used to generate the Posicast digital sequence. To adapt the low voltage signals delivered by the FPGA to the voltage requirement of the gate, we used the circuit illustrated in Fig. 7. Although no voltage or current feedback is required in order to apply the Posicast sequence, v_{ce} and i_c are measured to assess the improvement on the commutation waveforms. These measurements were performed with a 17 pF oscilloscope voltage probe and a 200 MHz-hall-effect current probe, respectively.

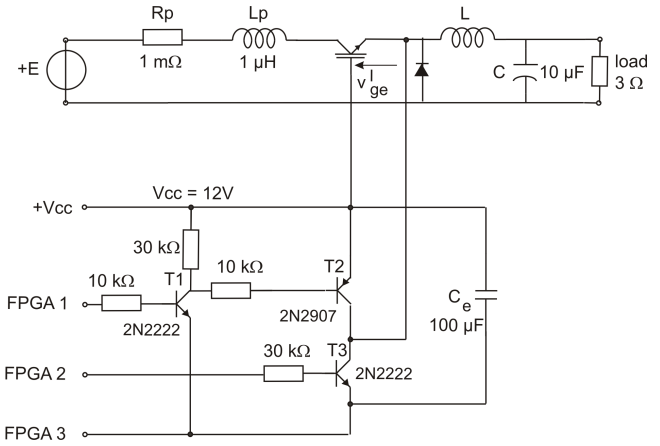


Figure 6. Scheme of a buck converter supplying a resistive load.

V_{ge} is imposed by the state of T2 and T3, which are controlled by the signalS provided by the FPGA (FPGA 1 and FPGA 2 respectively) (Fig. 10). The waveform of the signal that is effectively seen at the IGBT gate is determined by the gate circuitry and the parasitic capacitors present in the circuit. The circuit manages the discharge rate of the gate capacitor C_{ge} according to the states of the transistors T2 and T3. No explicit gate resistor is used in our proposed implementation.

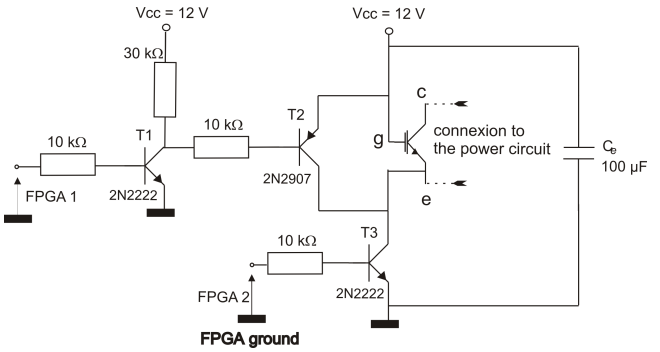


Figure 7. Circuit used to interface the FPGA with the IGBT gate.

The control signals from the FPGA work as follows: the two FPGA binary outputs, denoted FPGA 1 and FPGA 2 provides three electrical states on v_{ge}. The driver supplies the IGBT gate when FPGA 1 = ”0” and FPGA 2 = ”1” and it short-circuits the gate-emittor junction of the IGBT when FPGA 1 = ”1” and FPGA 2 = ”0”. A high-impedance state on the gate is possible when FPGA 1 = ”0” and FPGA 2 = ”0”. This state means that the transistor T2 is equivalent to a high resistance, connected in parallel to the gate. The transistor resistances are generally given in data-sheets. The working digital sequence is summarized in Table I. The evolution of V_{ge}^{i} is represented in Fig. 10.

The various states of the driver allows consequently adjusting the $\mathrm{d}v_{ge}/\mathrm{d}t$ and thus, the $\mathrm{d}i_c/\mathrm{d}t$. The resistors are chosen such that the consumption of the circuit remains low ($<$ 1 mW). The voltage reference of the IGBT emitter corresponds to the FPGA ground, which is not connected to the power circuit ground.

The use of a gate resistor R_g may add a small delay when turning on the IGBT because of the parasitic input capacitor. From the point of view of the Posicast method, R_g can be seen as a parasitic element and the method used to adjust the Posicast control parameters could be used without any change.

Table I
SIGNIFICATION OF FPGA DRIVER CONTROL BITS.

FPGA 1	FPGA 2	v_{ge} state
”0”	”0”	high-impedance
”0”	”1”	on (Fig. 8)
”1”	”0”	off (Fig. 9)
”1”	”1”	forbidden

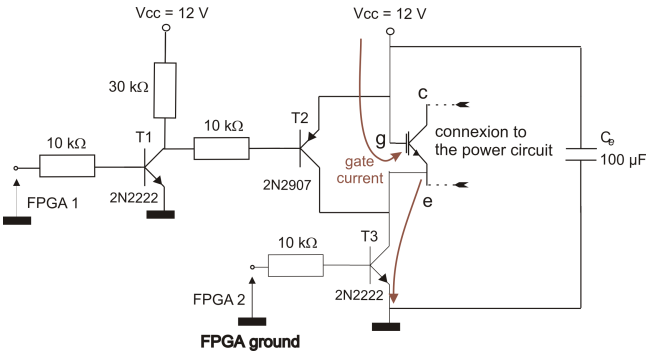


Figure 8. Supply of the IGBT gate.

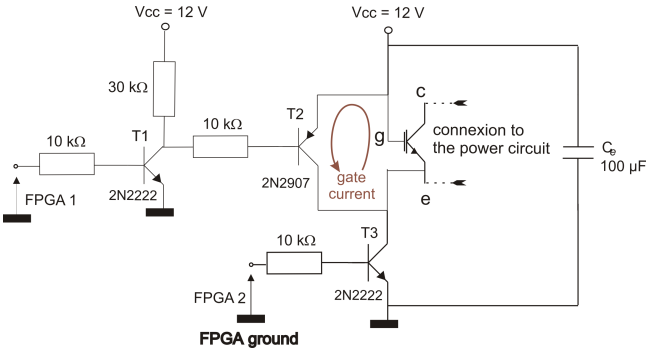


Figure 9. Short-circuit of the IGBT gate.

Figure 10 presents the corresponding sequence for the buck converter. For $t > t_{ge,off}$, which corresponds to the turn-off of T3, v_{ge} is forced to 0 until the voltage v_{ge}^{i} is close to $V_{ge,th}$. Let's denote t_m this instant. For $t_m < t < t_{ge,th}$, T2 and T3 are turned off, and the gate is connected to a high-impedance that allows v_{ge}^{i} and i_c to decrease slowly. Depending on the choice of t_m, it is therefore possible to control the $\mathrm{d}i_c/\mathrm{d}t$.

We call Posicast sequence of the IGBT, the sequence that drives the transistors T2 and T3 such that v_{ge} is P-optimal;

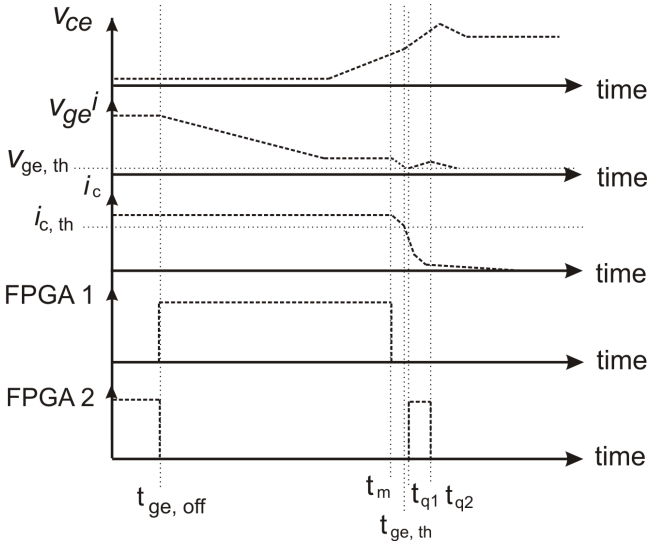


Figure 10. Description of the Posicast sequence in the case of a buck converter.

the set of parameters $\{t_m, t_{q1}, t_{q2}\}$ is called the Posicast parameters.

We distinguish the pre-P-optimal case, which corresponds to the minimization of the v_{ce} overshoot considering only the adjustment of the $\mathrm{d}i_c/\mathrm{d}t$ (using only the time t_m as our degree of freedom). The P-optimal case corresponds to the pre-P-optimal case plus the Posicast pulse. In this case, the whole set $\{t_m, t_{q1}, t_{q2}\}$ is used to control both $\mathrm{d}i_c/\mathrm{d}t$ (before effective the turn off) and $\mathrm{d}v_{ce}/\mathrm{d}t$ (after the effective turn off).

When $v_{ge}^i \geq v_{ge,\,th}$, the $\mathrm{d}i_c/\mathrm{d}t$ rate is modified by the high impedance state on the IGBT gate. Thus, v_{ge}^i, in the high impedance state, remains quasi-constant. At $t_{ge,\,th}$, the current i_c decreases quickly and can not be controlled. Finally, when the Posicast pulse occurs (i.e. at the instant t_{q1}), the fact that v_{ge}^i is constant and close to $v_{ge,\,th}$ helps to turn on quickly the IGBT again. v_{ge}^i does not have the time to reach $+V_{cc}$ during the Posicast pulse.

The selection of the parameters is based on an initial visual manual adjustment of the control parameters using external inputs on the FPGA development board. It means that one has to probe the v_{ce} voltage during the turn-off resonant transients and apply the procedure described below (Fig. 10).

- First, we adjust the t_m time, which controls the period of the short-circuit on the v_{ge} gate (recall that the v_{ge} short-circuit, operated by turning on T2, allows increasing $\mathrm{d}v_{ge}/\mathrm{d}t$ (or equivalently $\mathrm{d}i_c/\mathrm{d}t$) when the IGBT conducts). By controlling the discharge of the input capacitor C_{ge}, we control the $\mathrm{d}i_c/\mathrm{d}t$ rate at the time t_m, when the IGBT is blocking. Therefore, since the $\mathrm{d}i_c/\mathrm{d}t$ is minimized at the effective IGBT turn-off (when the i_c current is effectively turned-off), the resulting v_{ce} overshoot is also minimized since it is equal to $L_p \mathrm{d}i_c/\mathrm{d}t$.
- Then, we adjust the "Posicast pulse", whose purpose is to turn on the IGBT during a short time in order to cancel or minimize the resulting oscillation on v_{ce}. The principle of the "Posicast pulse" is the same as the short-circuit of the gate : whereas the short-circuit allows controlling the rate $\mathrm{d}i_c/\mathrm{d}t$, the "Posicast pulse" allows controlling the rate $\mathrm{d}v_{ce}/\mathrm{d}t$. The instant t_{q1} is defined when v_{ce} begins to increase and t_{q2} is defined when v_{ce} is close to its asymptotic value. Turning on the IGBT during the time interval $[t_{q1}, t_{q2}]$ allows managing the rate $\mathrm{d}v_{ce}/\mathrm{d}t$. At this time, the IGBT is turned off again and $v_{ce} \approx V_{ce,\,m}$. The result is a significant reduction of the original v_{ce} overshoot.

Although the $\mathrm{d}i_c/\mathrm{d}t$ is significantly reduced by the high-impedance state on the gate, there still exists an overshoot that can be reduced by the IGBT turn-on pulse when FPGA 1 = "0" and FPGA 2 = "1"(as described Fig. 5). Figure 11 presents the P-optimal and P-pre-optimal v_{ce} voltages for $L = 15$ mH as well as the collector current i_c and the control signals FPGA 1 and FPGA 2.

In the case of the buck converter, oscillations on v_{ce} induce oscillations on i_c due to the free-wheeling diode. Both oscillations are reduced by the proposed IGBT driver. However, this reduction of the oscillations comes at the expense of increased switching losses, as shown in Table II.

Table II
SWITCHING ENERGY FOR THE DIFFERENT OPTIMIZATION CASES IN THE CASE OF THE BUCK CONVERTER.

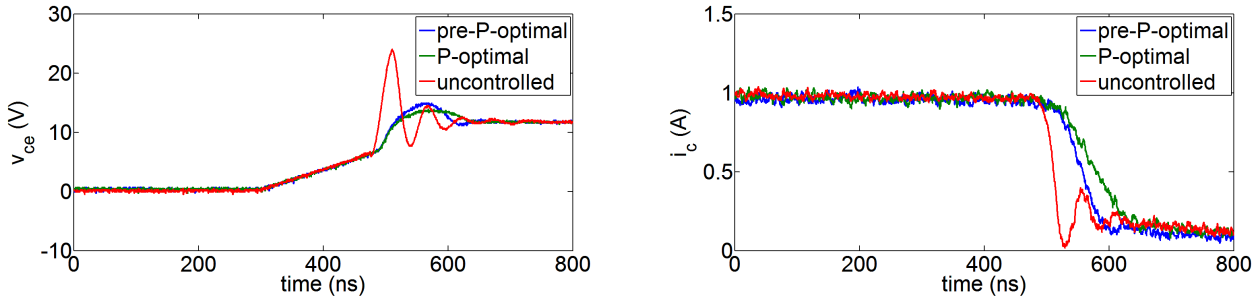
case	switching energy (mJ)
non optimal	1.26
P-pre-optimality	1.33
P-optimality	1.64

Figure 12 presents the optimized v_{ce} voltage and i_c current for $L = 10$ mH.

For a given buck topology, i.e. fixed load impedance and parasitic elements R_p and L_p, we observed that the optimal set of control parameters was independent of the output voltage and current. In other words, there is no need to adjust again the control parameters if the switching current changes through the source. If the load impedance changes, the topology changes and therefore, the response of the current changes (via time constants) when beginning upon turn-off (in particular the rate $\mathrm{d}i_c/\mathrm{d}t$). A reconfiguration of the control parameters is thus necessary in the case of varying loads. Moreover, the parasitic inductance influences both the amplitude of the overshoot $V_{ce,\,\delta}$ and the pseudo- resonance period ($2\pi\sqrt{L_p C_x}$). Each change of the power circuit configuration, in terms of cable length, or the IGBT device requires a readjustment of the control parameters.

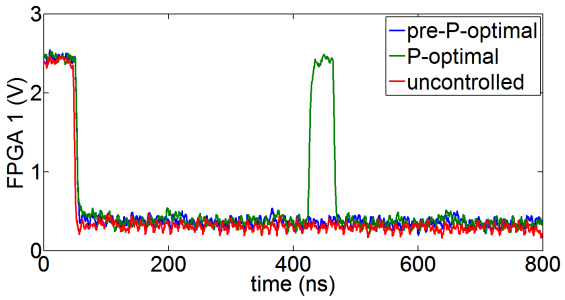
VI. CONCLUSION

In this paper, we introduced a new Posicast control for IGBT turn-off. We showed that it is possible to realize an optimal control of the v_{ce} voltage in order to minimize the switching overvoltage $V_{ce,\,\delta}$ and thus to decrease the resonant effects. The Posicast IGBT driver provides, in a general way, some

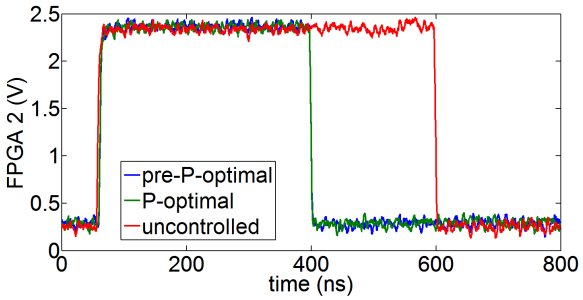


(a) v_{ce} voltage

(b) i_c current (cancelled at 0.7 μs)

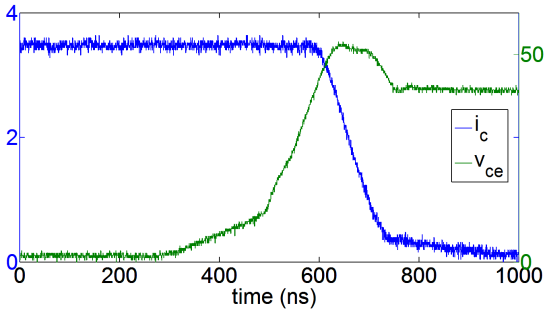


(c) signal FPGA 1

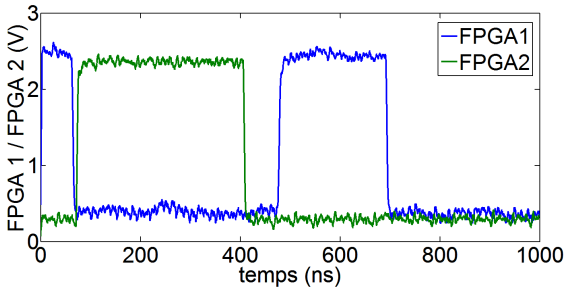


(d) signal FPGA 2

Figure 11. Evolution of v_{ce} and i_c for different turn-off sequences in the case of a buck converter ($L = 15$ mH) (switched current : 1 A - switched voltage 12 V).



(a) v_{ce} voltage and i_c current



(b) FPGA signals

Figure 12. Evolution of v_{ce} and i_c in the case of a P-optimal sequence ($L = 10$ mH) (switched current : 3.5 A - switched voltage 42 V.).

answers to the problem of the switching effectiveness. A FPGA device is used to generate a Posicast pulse sequences. This sequence allows minimizing the overshoot voltage and the resonant effects that occur during the turn-off. We demonstrated the effectiveness of the proposed method considering a small-scale buck converter. The main features are summarized as follow :

- simple Posicast control sequence, easy to adjust according to the parasitic inductance and the IGBT;
- any FPGA device can be used provided that its internal frequency is sufficient (typically around 100 MHz);
- the multiple outputs of an FPGA can be used to drive simultaneously multiple IGBTs, which are included for instance in a multi-level inverter topology.

Future work will address with the development of algorithms that could identify and adjust automatically the Posicast sequence when the load varies. An adaptative procedure could be implemented in order to preserve the resulting optimization according to load changes. In this case, one can sense the average current (with a relatively low bandwidth) in the load and build a table inside the FPGA that creates a correspondence between the optimal control parameters and the output current. The control parameters of the Posicast controller would be thus updated with the data provided by the table according to the output current. The application of the Posicast driver to the drive of power switches in high power converters is also of interest. Following this proof-of-concept, the next step of this research is to prepare a test setup at high power, in the range

of 200 A and 400 V.

REFERENCES

[1] R. Chokhawala, J. Catt, and B. Pelly, "Gate drive considerations for IGBT modules," in Conf. Rec. IEEE-IAS Annu. Meeting, pp. 1186-1195, Oct. 1992.

[2] D. W. Brown, M. Abbas, A. Ginart, I. Ali, P. W. Kalgren, and G. J. Vachtsevanos, "Turn-Off Time as an Early Indicator of Insulated Gate Bipolar Transistor Latch-up," IEEE Transactions on Power Electronics, vol.27, no.2, pp.479-489, Feb. 2012.

[3] A. Bryant, Y. Shaoyong, P. Mawby, X. Dawei, R. Li, P. Tavner, and P. Palmer, "Investigation Into IGBT dV/dt During Turn-Off and Its Temperature Dependence," IEEE Transactions on Power Electronics, vol.26, no.10, pp.3019-3031, Oct. 2011.

[4] R. Hemmer, "Intelligent IGBT drivers with exceptional driving and protection features," in Proc. of 13th European Conference on Power Electronics and Applications, pp. 1-4, Sept. 2009.

[5] L. Chen, and F.Z. Peng, "Closed-Loop Gate Drive for High Power IGBTs," in Proc. of Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, pp. 1331-1337, Feb. 2009.

[6] L. Chen, and F.Z. Peng, "Switching loss analysis of closed-loop gate drive," in Proc. of Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition, pp.1119-1123, Feb. 2010.

[7] S.K. Biswas, B. Basak, and K.S. Rajashekara, "Safe operation of IGBTs in switching converters," in Proceedings of 1995 International Conference on Power Electronics and Drive Systems 1995, pp.65-70, vol.1, Feb. 1995.

[8] L. Dulau, S. Pontarollo, A. Boimond, J.-F. Garnier, N. Giraudo, and O. Terrasse, "A new gate driver integrated circuit for IGBT devices with advanced protections," IEEE Trans. Power Electron., vol. 21, no. 1, pp. 38-44, Jan. 2006.

[9] S. Yanqun, J. Jiang, Y. Xiong, Y. Deng, X. He, and Z. Zeng, "Parasitic inductance effects on the switching loss measurement of power semiconductor devices," in IEEE International Symposium on Industrial Electronics, vol.2, pp.847-852, Jul. 2006.

[10] P.J. Grbovic, "An IGBT Gate Driver for Feed-Forward Control of Turn-on Losses and Reverse Recovery Current," IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 643-652, Mar. 2008.

[11] P.J. Grbovic, F. Gruson, N. Idir, and P. Le Moigne, "Turn-on Performance of Reverse Blocking IGBT (RB IGBT) and Optimization Using Advanced Gate Driver," IEEE Transactions on Power Electronics, vol.25, no.4, pp.970-980, Apr. 2010.

[12] O.J.M. Smith, "Posicast Control of Damped Oscillatory Systems," in Proceedings of the IRE, vol.45, no.9, pp.1249-1255, Sept. 1957.

[13] G. Cook, "An application of half-cycle Posicast," IEEE Transactions on Automatic Control, vol.11, no.3, pp. 556- 559, Jul. 1966.

[14] J.Y. Hung, "Feedback control with Posicast," IEEE Transactions on Industrial Electronics, vol.50, no.1, pp. 94- 99, Feb. 2003.

[15] M. Rasoulzadeh, and M.B. Ghaznavi-Ghoushchi, "Oscillation controlled electronic systems design using Posicast-based pulse pre-shaping," in 52nd IEEE International Midwest Symposium on Circuits and Systems, pp.24-28, Aug. 2009.

[16] F. Qi, R.M. Nelms, and J.Y. Hung, "Posicast-based digital control of the buck converter," IEEE Transactions on Industrial Electronics, vol.53, no.3, pp. 759-767, June 2006.

[17] O. M. Bashnyakov, "On optimal bang-bang control," Nonlinear Oscillations, Vol. 5, No. 2, 2002.

[18] N. C. Singer, and W. P. Seering, "Experimental Verification of Command Shaping Methods for Controlling Residual Vibration in Flexible Robots," American Control Conference, pp 1738-1744, 1990.

[19] T.D. Tuttle, and W.P. Seering, "Creating time-optimal commands for systems with denominator dynamics," in Proceedings of the 1996 IEEE International Conference on Control Applications, pp.385-390, Sep 1996.

[20] N. Idir, R. Bausiere, and J.J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," IEEE Transactions on Power Electronics, vol.21, no.4, pp. 849- 855, July 2006.

[21] J.-T. Hsu, and K.D.T.Ngo, "Behavioral modeling of the IGBT using the Hammerstein configuration," IEEE Transactions on Power Electronics, vol.11, no.6, pp.746-754, Nov 1996.

[22] K. Wanying, A. Hyungkeun, and M.A.E. Nokali, "A parameter extraction algorithm for an IGBT behavioral model," IEEE Transactions on Power Electronics, vol.19, no.6, pp. 1365-1371, Nov. 2004.

[23] S. Pittet, and A. Rufer, "The equivalent electron density concept for static and dynamic modeling of the IGBT base in soft- and hard-switching applications," IEEE Transactions on Power Electronics, vol.22, no.6, pp.2223-2233, Nov. 2007.

[24] V. K. Khanna, "IGBT Theory and Design", IEEE Press, Wiley-Interscience, 2003.