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Design of a Low Power and Delay 4-Bit CAM using 9T SRAM

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Abstract – Content Address Memory (CAM) is a type of memory that operates like hardware search engines which are widely used in a large number of applications that we use in our daily works or lives, such as networking when we send or communicate with each other, routers, and database management systems that require storing data, and fast searching when applying queries[15]. The use of the 9T SRAM (Static Random Access Memory) component to implement the CAM has been increased because of its advantages in terms of power consumption, stability, and area compared with other SRAM cells such as 6T, 7T, and 8T. By implementing CAM using 9T SRAM, we combine the searching functionalities of CAM and the optimization of power, area, and cost of 9T SRAM[21]. In this paper, we will design, and implement a low-power and delay 4-bit CAM by nine transistors of SRAM using a 22 nm process file. In addition, we will go through the steps of designing the schematics and the layout of each component used to build the final 4-bit CAM with its optimized area, and power without affecting the searching functionality of the Content Address Memory (CAM).

Keywords— CAM, SRAM, optimization, layout, schematic.

I. INTRODUCTION

RAM, or (Random Access Memory)is an important hardware component of a computer's main memory, allowing for direct access by the Central Processing Unit (CPU). It is used to read or write data in a targeted address on the memory. In addition, RAM serves as a temporary store for the running programs that are being used by the processor[1]. RAM is a volatile type of memory, meaning that when the power is turned off, the information will be lost. When searching in RAM, it takes the address of the data as an input, and returns the content word of that address; this operation is done by many cycles until getting the required data stored in RAM[6].

Content Addressable Memory (CAM), also referred Associative Memory, that performs similar operations of RAM that include the read and write on a given address[21], but it has additional searching functionalities; it takes the data as input, searches in its memory about that data by using a parallel comparison between the input word data and the whole memory, and returns the list of addresses where the data word was located[8]. As shown in the following figure (Figure 1), the data word(search word) is the input, and the search line for the parallel comparison; if the data stored in the memory cell matches the incoming data, the match line will be activated. The encoder outputs an encoded version of the match location using log2 w bits[6].As a functionality comparison between both RAM, and CAM; the CAM is an inverse operation of RAM in reading operation as shown in (Figure 2).

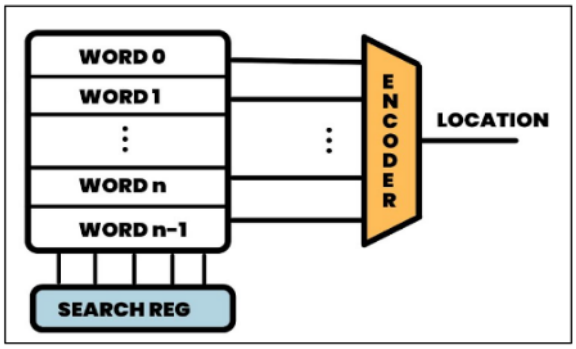

Figure 1 Conceptual view of a CAM[3].

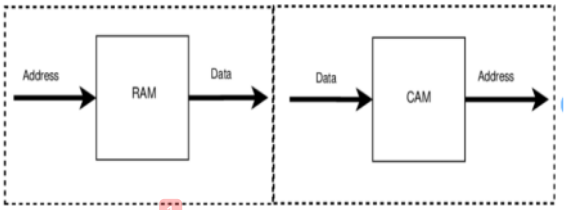

Figure 2 CAM is an inverse operation of RAM.

In terms of speed, when reading data words using the traditional RAM, multiple clock cycles are needed to find the address of the input data. While CAM can perform the search operation in parallel as mentioned in one single cycle, which makes CAMs have faster search times compared to RAMs, which makes the CAM widely used in database management systems and network switching that require fast searching functionalities which CAM offers[1]. However, the speed of a CAM comes at the cost of increased silicon area and power consumption compared with the normal RAM due to the additional circuit required to make comparisons and generate the search and match lines[6].

Implementing CAM can be done using the SRAM schematic since it performs the same operations as SRAM. In addition, the SRAM can be implemented using different numbers of transistors, such as 6T, 8T, 9T, and 10T all depending on the requirements and the specifications of the application or project[13]. In our project, the CAM will be designed and implemented using 9T SRAM. The following figure (Figure 3) shows the 9T SRAM schematic.

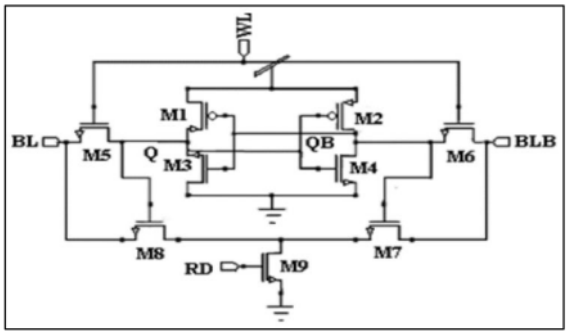

Figure 2 Schematic of 9T SRAM Circuit[14].

II. Design and Implementation

To implement 4-bit CAM using 9T SRAM, several components are required to be designed and built independently, and then used later in the 4-bit CAM schematic circuit as one block. These components are as the following:

A. 9T SRAM

As shown in the following figure, the 9T SRAM circuit has 4 inputs lines, which are the word line (WL), (RL), and other 2 bits line (BL and BLB). While the have two outputs (QB), and (Q).

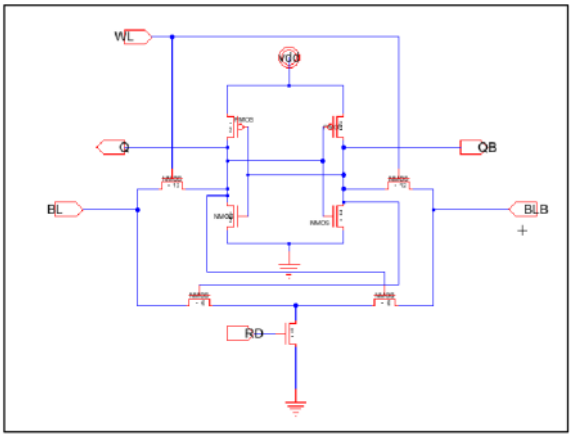

Figure 4 The schematic of 9T SRAM circuit.

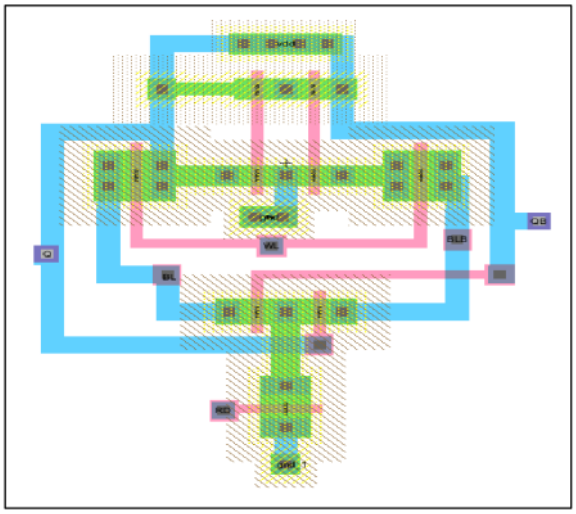

Figure 5 The layout of 9T SRAM.

B. 1-Bit CAM

Then, the circuit of the 1-bit CAM was implemented as shown in the following circuit; two additional invertors was added, and two pass gates for the comparison operation. And finally, the output of the circuit that represents the match signal.

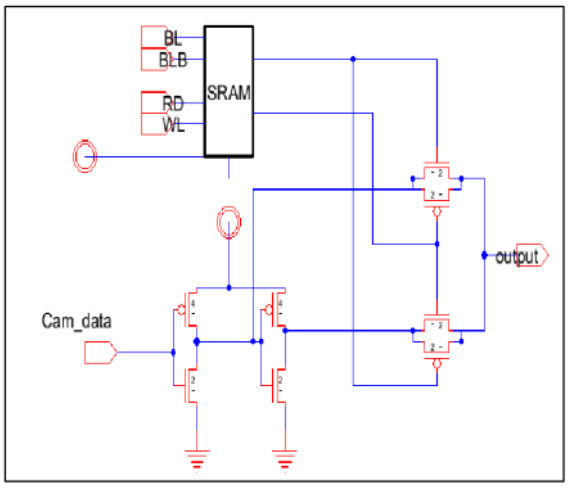

Figure 3 The schematic of 1-Bit CAM circuit.

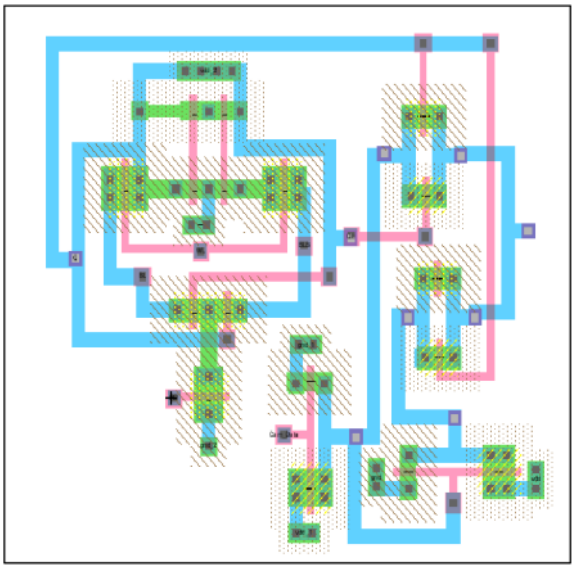

Figure 4 The layout of the 1-bit CAM.

C. 2x4 Decoder

In the 4-bit CAM implementation, the 2x4 decoder needed, because it helps in selecting the appropriate 1-Bit CAM cell from the 4-bits for the search operation. The following the figures represent the schematic and the layout of the decoder.

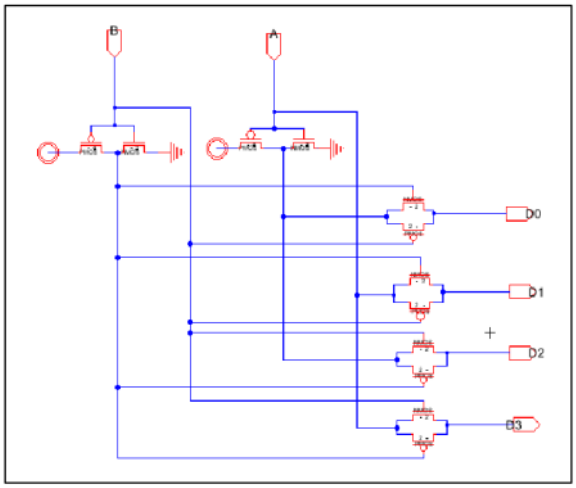

Figure 5 The schematic of the 2x4 Decoder.

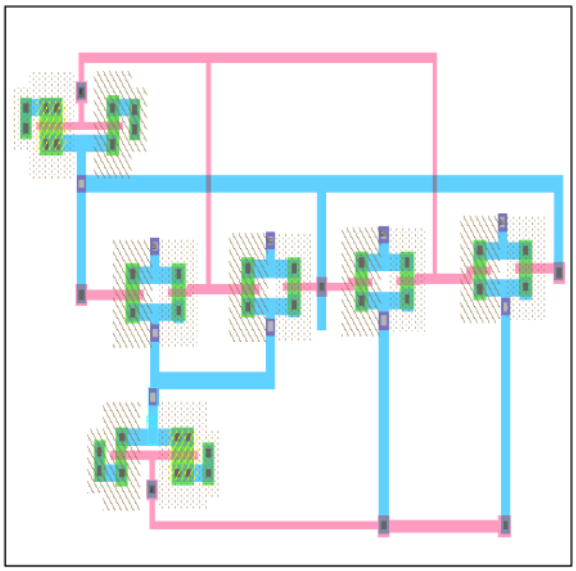

Figure 6 The layout of the 2x4 Decoder.

D. 4-inputs NAND gate

The 4-inputs NAND gate implementation will be used when implementing the 4-Bit CAM when connecting the 4 blocks of the 1-bit CAM to the final output.

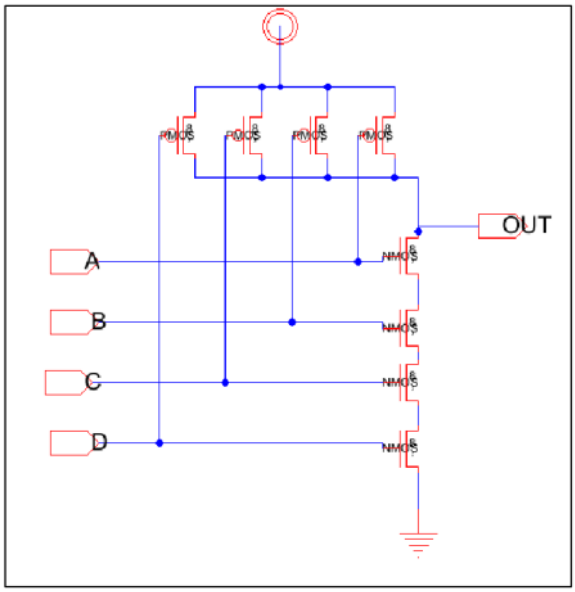

Figure 7 4-inputs NAND gate schematic.

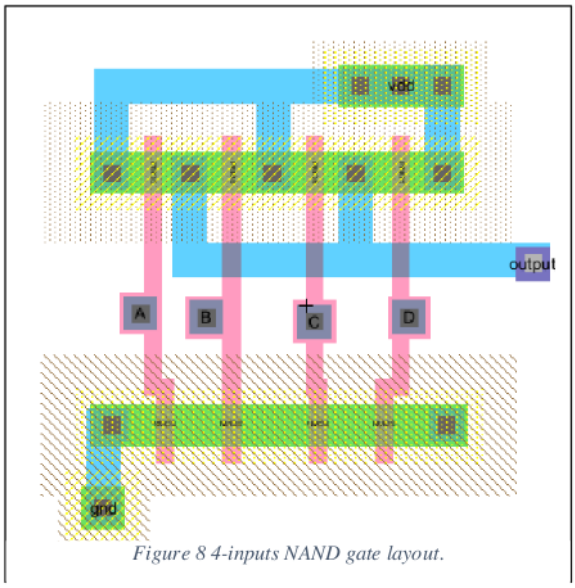

Figure 8 4-inputs NAND gate layout.

E. Invertor

Lastly, the last component needed for the 4-Bit CAM circuit is the invertor circuit, the following figures shows the used schematic and layout of the component.

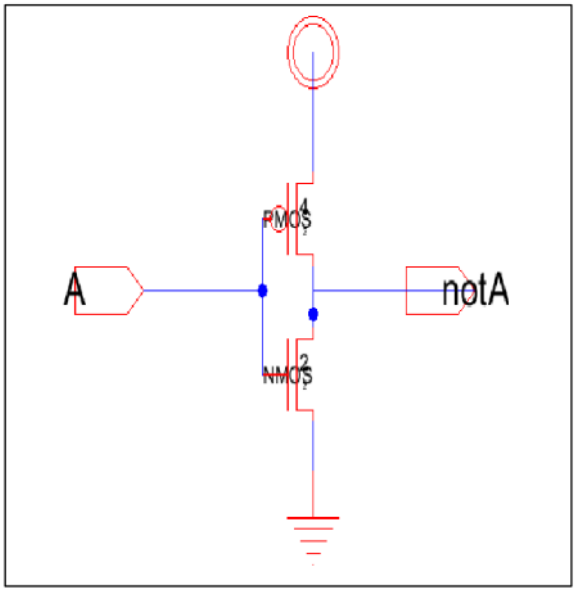

Figure 9 Invertor schematic.

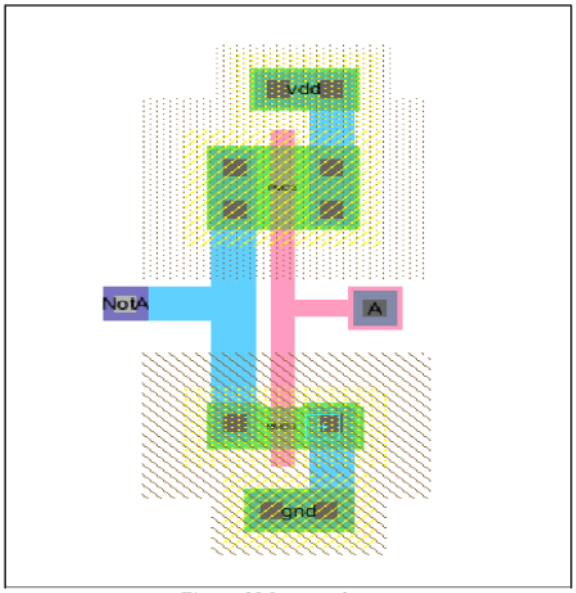

Figure 10 Invertor layout.

F. 4-Bit CAM

Finally, the circuit of the 4-Bit CAM using 9T SRAM was implemented as shown in the following figure, the decoder, and 1-bit CAM, NAND gates, and the invertor were used to design and implement to find the output of the 4-Bit CAM.

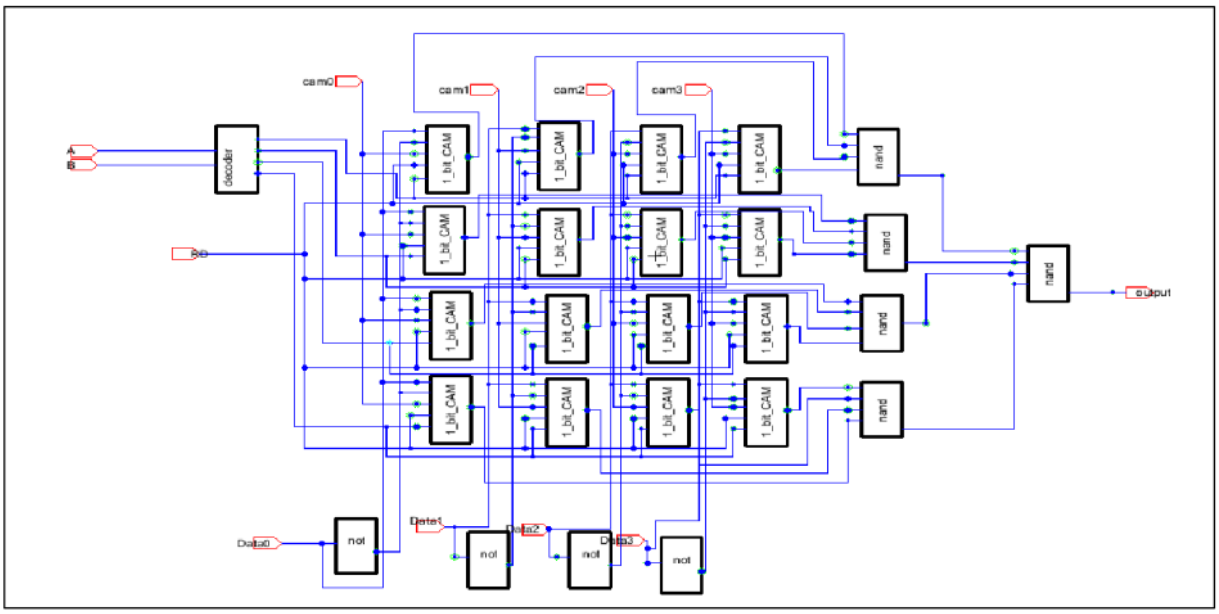

Figure 14 The schematic of the 4-Bit CAM using 9T SRAM.

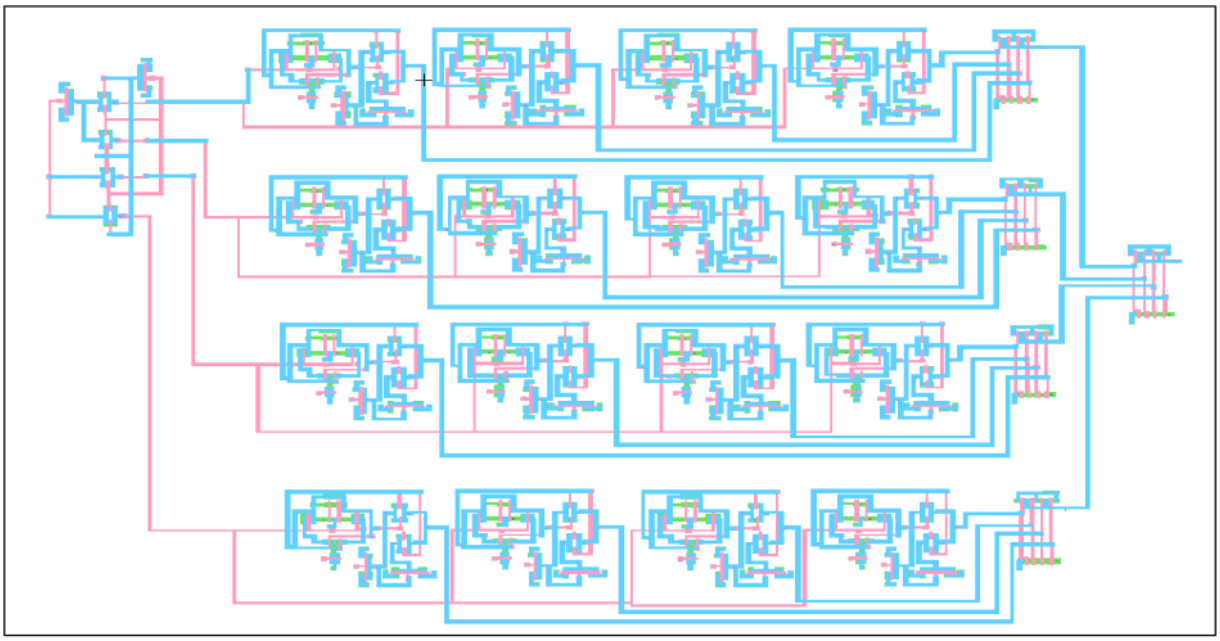

Figure 15 The layout of the 4-Bit CAM using 9T SRAM.

III. Area, Power, and Delay Optimization

In terms of power, and after extensive research and experimentation, it has been determined that an inverter size of 3λ provides optimal results for 9T SRAM design. In this configuration, the access transistors should quadruple the size of the inverter (12λ), while the two NMOS transistors should double the size of the inverter (2λ). Additionally, the NMOS transistor connected to the Read line should be sized between the access and the other two NMOS transistors. These findings serve as a helpful guideline for optimizing the design of 9T SRAM memory to achieve desired performance and efficiency.

Table 1 shows the output of changing the size of the CMOS.

Transistor Weight	Delay	Power Consumption
9	0.054ns	1.23uW
12	0.27ns	1.23uW
12	0.054ns	1.23uW
6	0.581ns	1.39uW
6	0.054ns	1.23uW
14	0.367ns	2.56 µW
2	0.533ns	0.12 µW

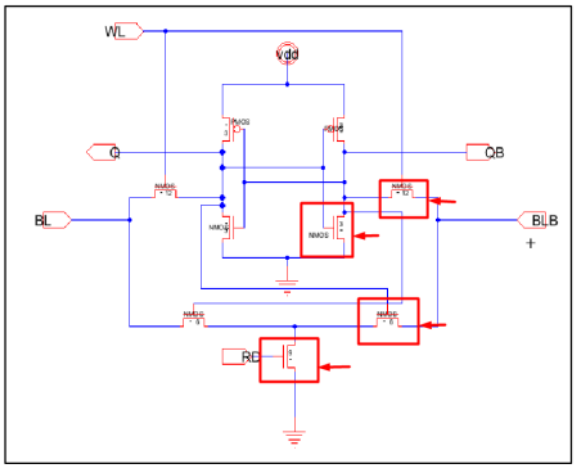

Figure 16 Sizing, and power optimization of SRAM.

While, in terms of area, and cost optimization, we have done several points that reduced the number of used transistors and silicon area, without affecting the efficiency of the output value, or performance of the circuit. Firstly, the following figure shows in the 2x4 decoder circuit. In particular, this decoder consists of 4 AND gates and 2 invertors which costs 28 gates.

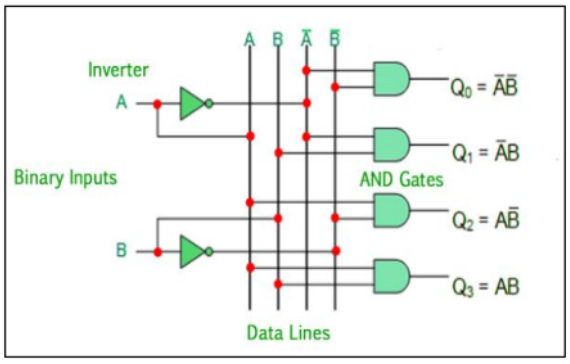

Figure 17 2x4 Decoder circuit.

However, the decoder that we used in 4-Bit CAM circuit was implemented using pass gates instead of AND gate, this minimized the number of used gates from 28 gates to 12 gates without affecting the power or delay.

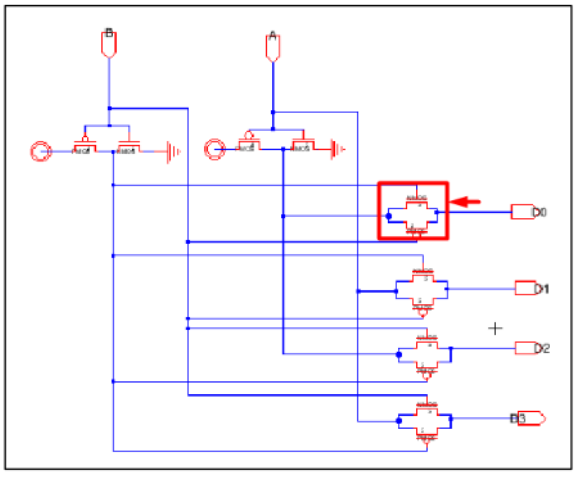

Figure 18 Area optimization for 2x4 Decoder.

In addition, the practical implementation of connecting the 4 blocks of the 1-Bit CAM in each line is by using AND – OR implementation, which requires adding 4 blocks of NAND gate blocks connected with an inverter to get the AND gate, and the same with the OR gate, it will be required to build the NOR gate first, and connect it with other inverter, this implementation requires 50 transistors. While in our design, we replaced this the AND – OR with its equivalent which is using NAND - NAND implementation, which optimize the number of used transistors from 50 to 40 transistors.

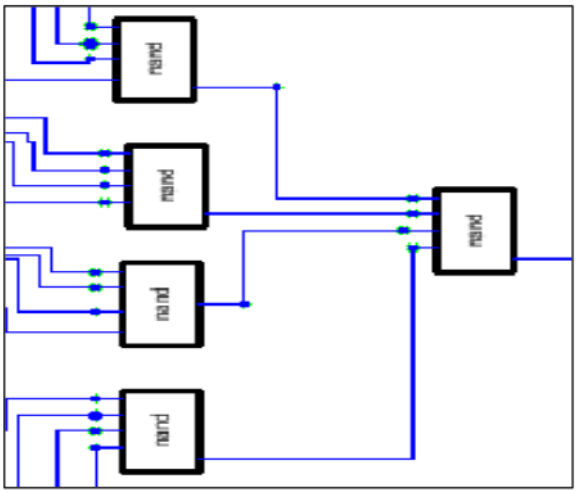

Figure 19 NAND gates area optimization.

IV. Simulation and Results

A. 9T SRAM Simulation

In SRAM memory, the write operation is performed when the write line, also known as the write, enable or WE line, is in a high state. This line acts as a control signal for the memory, determining whether the memory cells are in a read-only or write mode. When the write line is high, the memory cells can receive and store new data. Conversely, when the write line is low, the memory cells are in a "read-only" state, and any attempts to write to the memory will be ignored. This mechanism ensures the stability and integrity of the stored data while allowing for dynamic updates as needed.

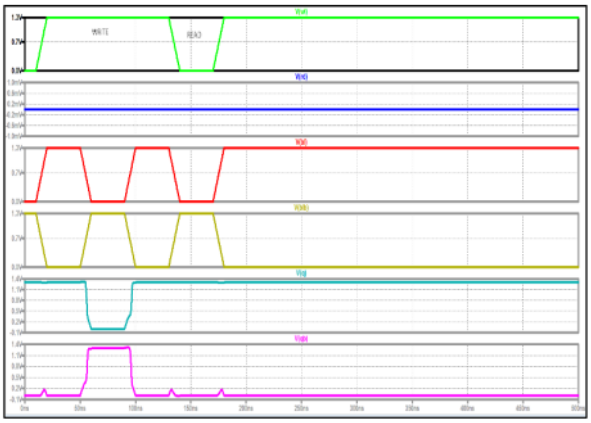

Figure 20 9T SRAM Simulation.

B. Decoder Simulation

In digital electronics, a 2x4 decoder is a combinational logic circuit that takes two binary inputs and produces four outputs corresponding to each possible combination of the input bits. When the input bits are "low, high", the decoder outputs a logical "high" signal at the first output, referred to as D1, while the remaining three outputs, namely D0, D2, and D3, are all set to logical "low". This specific behavior of the 2x4 decoder is due to its truth table, which defines the output of the decoder for each possible input combination.

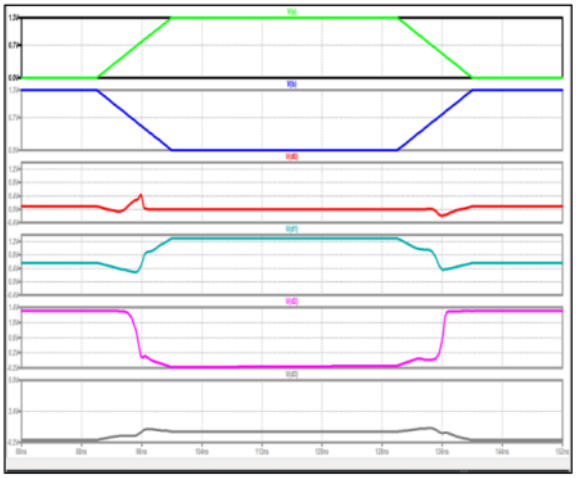

Figure 21 2x4 Decoder Simulation.

V. Possiple Improvements

Furthermore, we developed a possible improvement idea, which is combining each 1-Bit CAM in each row with 1 block; this solution can help to reduce and minimize the used area for each bit of the CAM circuit.

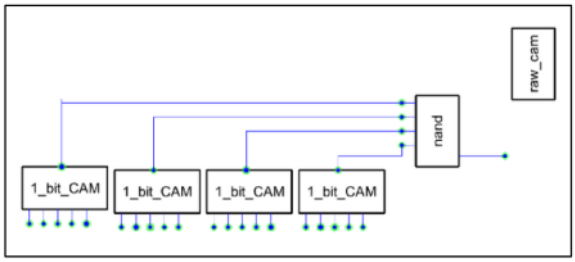

Figure 22 Possible Improvement for area optimization.

VI. Conclusion

Finally, the design and implementation steps of the 4-Bit CAM circuit were discussed and shown clearly; and the layout and the schematic circuit for each component used in the final circuit were illustrated. In addition, we represented some techniques that we followed to optimize the power consumption, area, and delay for the 4-Bit CAM without affecting the performance and the searching functionality of the Content Address Memory (CAM). Finally, the simulation results of some circuits were represented and discussed clearly.

VII. References

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