BIRZEIT UNIVERSITY

Faculty of Engineering and Technology

Electrical and Computer Engineering Department

ENEE4113

COMMUNICATION LABORATORY

Delta Modulation (Linear & DCDM)

Report No.3

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Abstract

This experiment aims to introduce the concepts and the two types of delta modulation and demodulation. Both linear delta modulation (LDM), and digital controlled delta modulation (DCDM) will be examined clearly by generating a sine wave signal practically and comparing it with the predicted signal. In addition, the experiment examines the pulse height characteristics in both linear and digitally controlled delta modulation. Furthermore, it discusses the output signals of the LDM modulator, comparing the return-to-zero (RZ) and non-return-to-zero (NRZ) modulation schemes. Also, to discuss the concepts of Granular noise, slope-overloaded distribution, and the dynamic of both linear (LDM) and digital controlled (DCDM) delta modulation as well as the demodulation processes for both techniques.

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Theory

1. Delta Modulation

Delta modulation is a process mainly used in the transmission of voice information. It is a technique where analog-to-digital and digital-to-analog signal conversion are seen. Delta modulation (DM) is an easy way of (DPCM). In this technique, the difference between consecutive signal samples is encoded into n-bit data streams. In DM, the data which is to be transmitted is minimized to a 1-bit data stream [2]. The following figure shows the block diagram of the delta modulation:

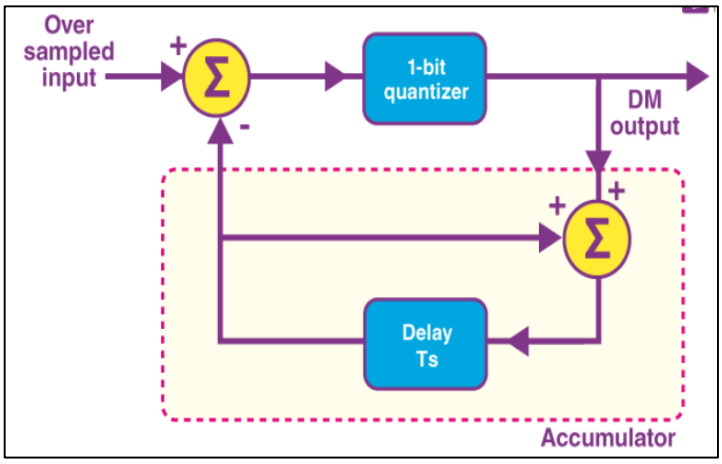


Figure 1 Delta Modulation (DM) block diagram.

The delta modulator block diagram includes a **1-bit quantizer** and a delay circuit along with two **summer circuits**. The output of the delta modulator will be a stair-case approximated waveform. The step size of this waveform is the delta (Δ) [1]. The output quality of the waveform is moderate.

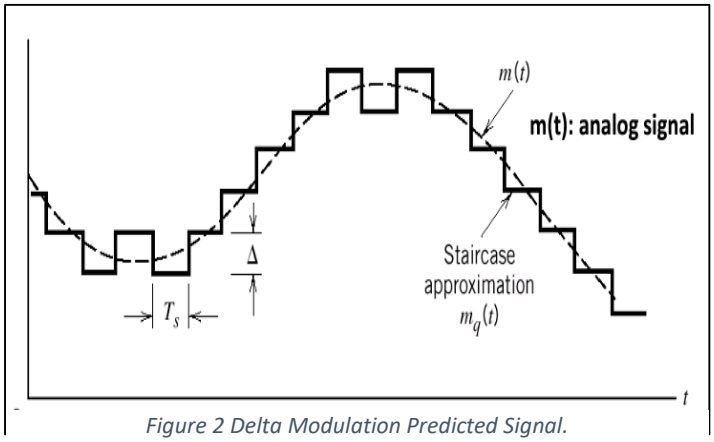


Figure 2 Delta Modulation Predicted Signal.

Delta modulation (DM) is divided into two main types, the linear delta modulation (LDM), and Digital Controlled Delta Modulation (DCDM).

1.1 Linear Delta Modulation (LDM)

Linear delta modulation is a simple and specific form of delta modulation, and it is considered a variant of delta modulation. In this kind of modulation, the step size or delta value remains constant throughout the modulation process. The input signal is compared to a linear approximation, and the difference or delta between the two is quantized and encoded. The constant step size used in LDM simplifies the implementation but can introduce certain issues, such as slope overload and granular noise [3].

1.2 Digital Controlled Delta Modulation (DCDM)

It also referred as Adaptive Delta Modulation. In the adaptive delta modulation, the step size of the staircase signal is not fixed and changes depending upon the input signal. Here first the difference between the present sample value and previous approximation is calculated. This error is quantized i.e. if the present sample is smaller than the previous approximation, quantized value is high or else it is low. The output of the one-bit quantizer is given to the Logic step size control circuit where the step size is decided.

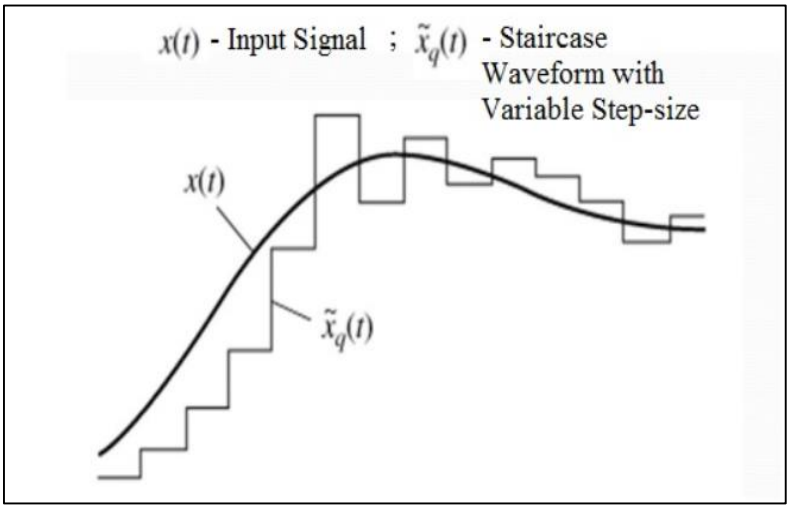


Figure 3 Adaptive Delta Modulation Waveform.

2. Granular noise and Slop-overload

The delta modulation has two major drawbacks, the granular noise and slop-overload.

2.1 Slop-overload distribution

This distortion arises because of large dynamic range of the input signal. The rate of rise of input signal x(t) is so high that the staircase signal can't approximate it, the step size 'Δ' becomes too small for staircase signal u(t) to follow the step segment of x(t) as figure 4 represents.

2.2 Granular noise

Granular or Idle noise occurs when the step size is too large compared to small variation in the input signal. This means that for very small variations in the input signal, the staircase signal is changed by large amount (Δ) because of large step size. Figure 4 shows that when the input signal is almost flat , the staircase signal u(t) keeps on oscillating by $\pm\Delta$ around the signal. The error between the input and approximated signal is called granular noise.

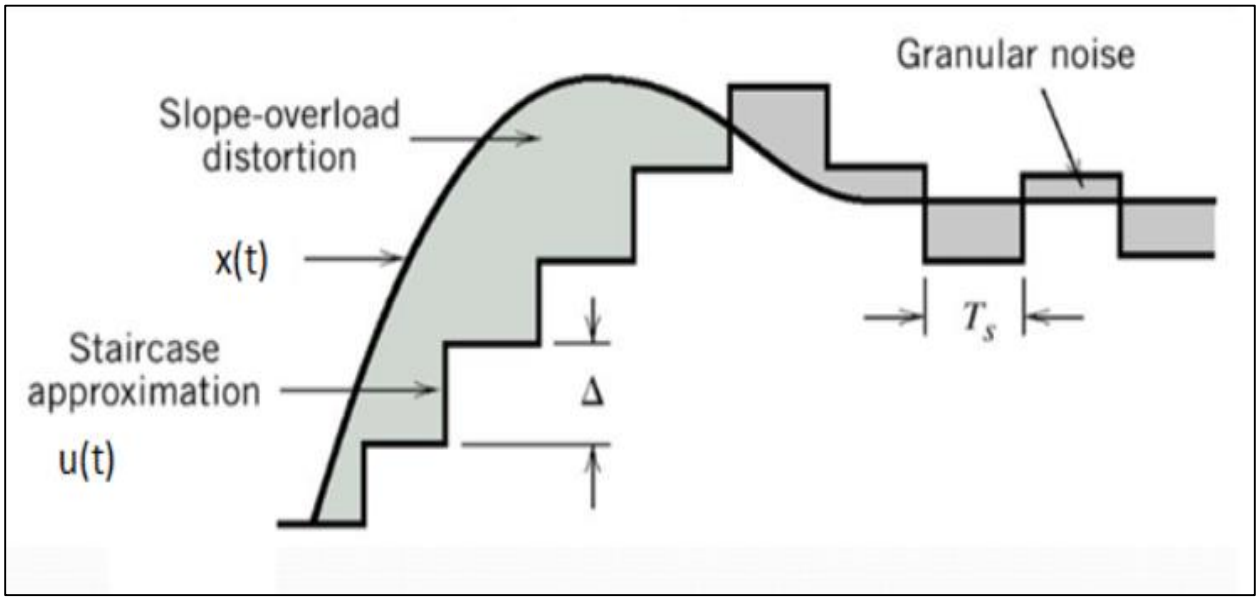


Figure 4 Quantization Errors in Delta Modulation.

3. Delta Demodulation

Delta demodulation is the process of converting a delta modulated signal back to its original form. The demodulation process involves using a one-bit quantizer to reconstruct the binary sequence from the delta modulated signal. This binary sequence is then integrated to approximate the original continuous-time waveform. The reconstructed signal is then passed through a low-pass filter to remove high-frequency components and noise. The output of the demodulation process is the demodulated signal, which ideally represents the original analog signal that was delta modulated [7].

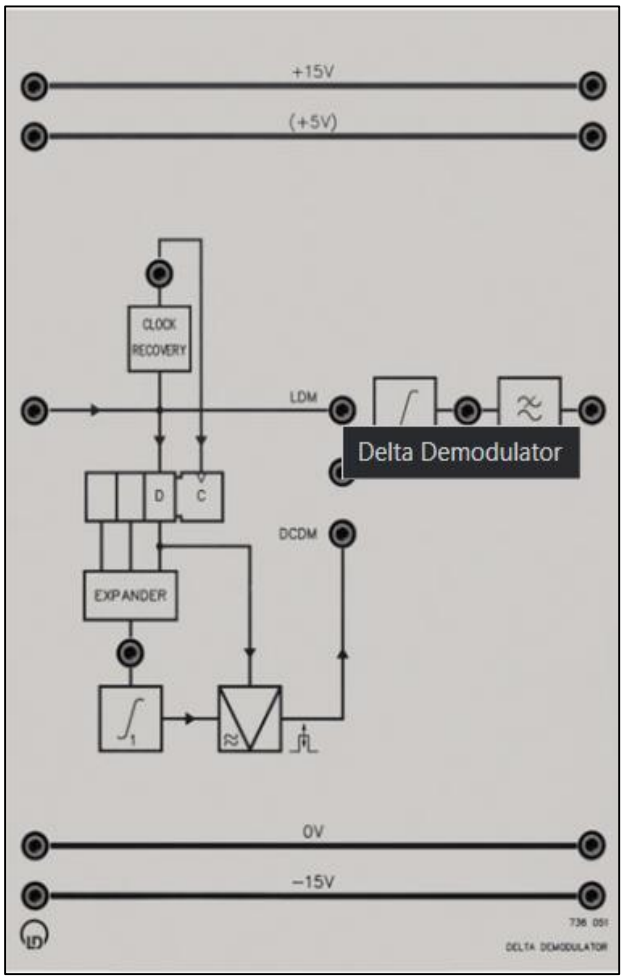


Figure 5 Delta Demodulation circuit components.

Procedure and Data Analysis

Part 1: Prediction Signals in Linear Delta Modulation (LDM)

The first part aims to compare the original message signal with the predicted signal for the Linear Delta Modulation. To carry out this objective, the delta modulator quantizes the difference between the signal and its prediction. The following circuit was connected, and a sine wave signal with message frequency 100 Hz, and amplitude equals to 1 Volts was generated using the function generator component. Also, the bridging plug to linear delta modulator was set. Finally, the CASSY Sensor UA1 was connected to the modulating signal Sm(t) while CASSY Sensor UB1 to the prediction signal, and clock frequency was set to its max value (f clock = 100 kHz).

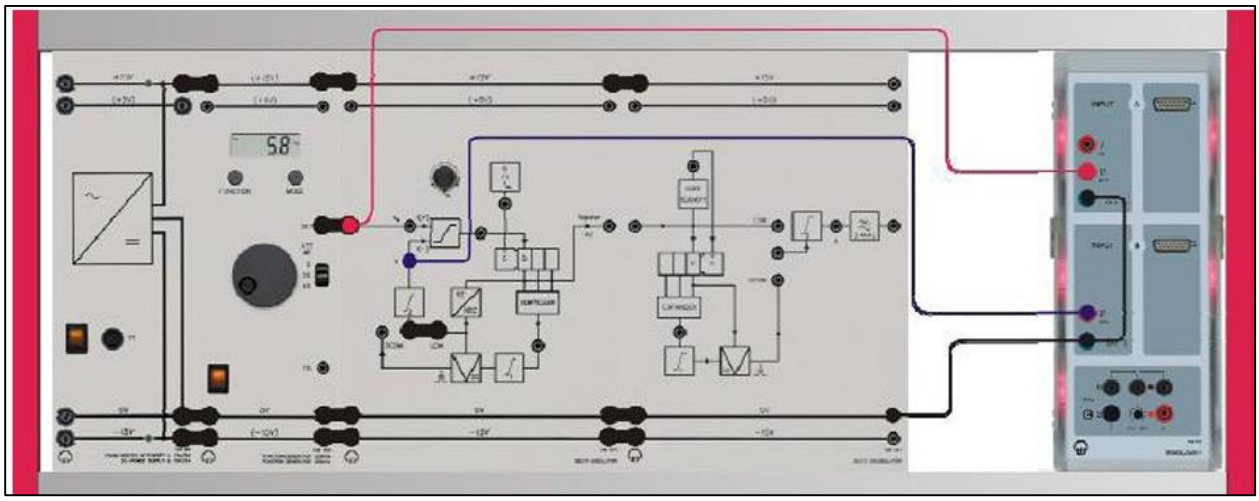


Figure 6 Predicted signal in linear delta modulation (LDM) circuit connection.

1.1 When clock frequency at its maximum value (f=100 kHz)

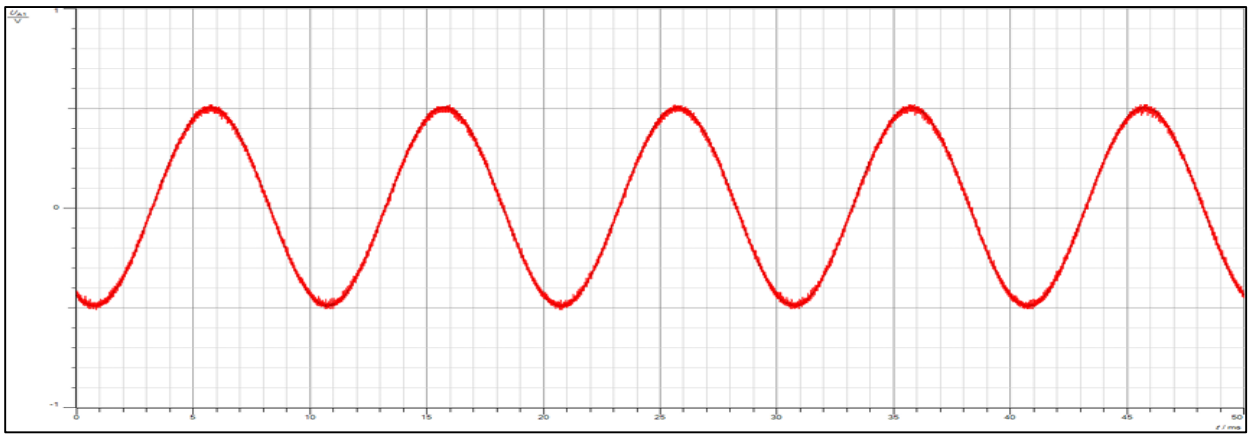


Figure 7 Predicted signal in linear delta modulation in time domain when clock freq = 100 kHz.

1.2 When clock frequency at its minimum value (f=10 kHz)

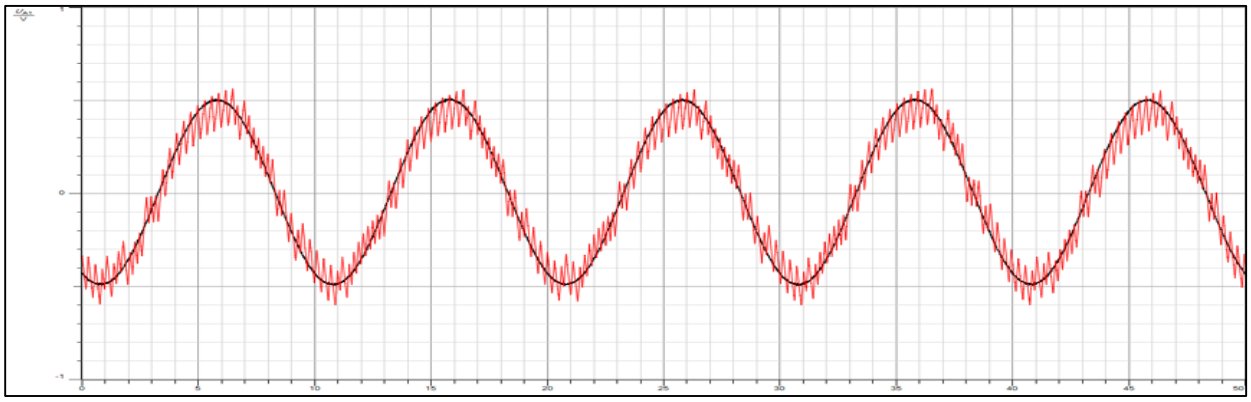


Figure 8 Predicted signal in linear delta modulation in time domain when clock freq = 10 kHz.

From the previous results, it is noticed that the clock frequency has a significant impact on the prediction signals. Increasing the clock frequency improves the predicted signal and leads to having e fewer error rate compared to the original input signal. However, when we decrease the value of the clock frequency to its min, it leads to reduce the predicted signal accuracy compared to when we increase it.

Part 2: Prediction Signals in Digital Controlled Delta Modulation (DCDM)

The objective of this part is to compare the predicted signal with the original input signal, and studying the effect of the clock frequency in digital controlled delta modulation (DCDM). The same circuit setup was used, but the bridging plug was connected to DCDM.

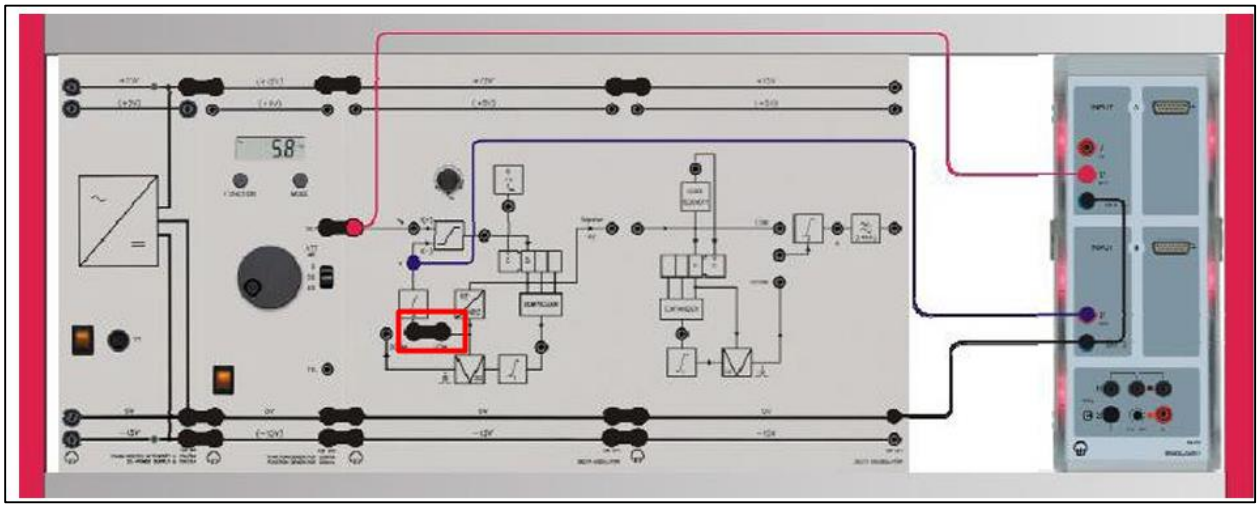


Figure 9 Predicted signal in digital controlled delta modulation (DCDM) circuit connection.

2.1 When clock frequency at its maximum value (f=100 kHz)

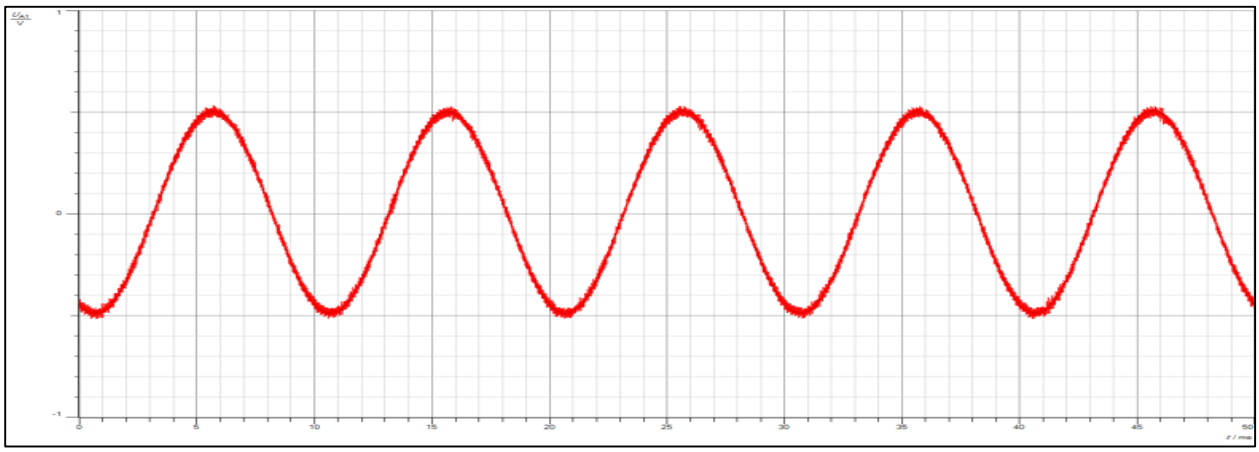


Figure 10 Predicted signal in digital controlled delta modulation in time domain when clock freq = 100 kHz.

2.2 When clock frequency at its maximum value (f=10 kHz)

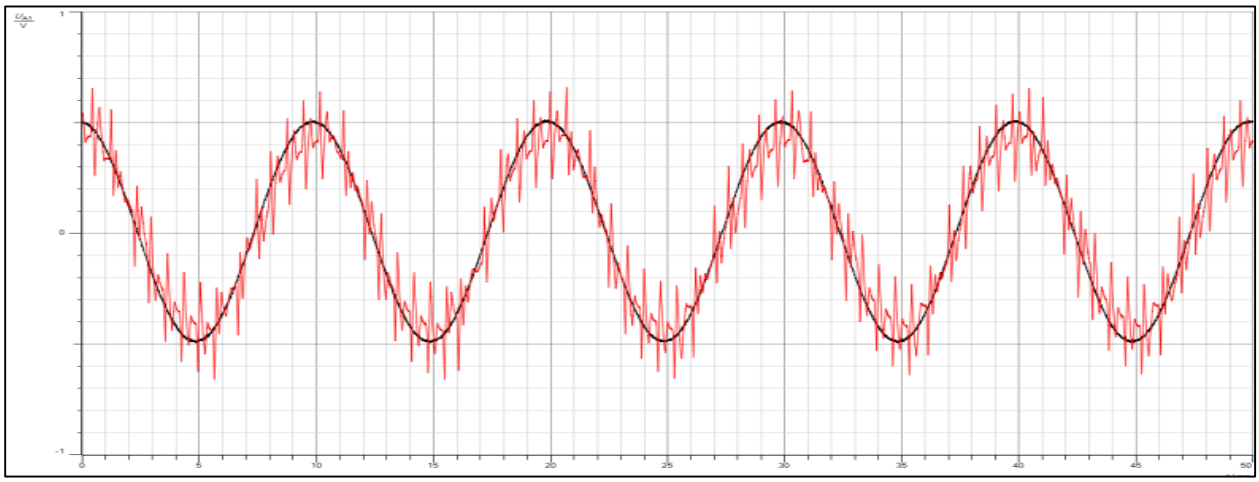


Figure 11 Predicted signal in digital controlled delta modulation in time domain when clock freq = 10 kHz.

Using the above results, and when comparing the predicted signal in each case, when increasing the value of the clock frequency, the predicted signal becomes more accurate and close to the original input message. Unlike the situation when decreasing the value of the clock frequency, the predicted signal has a higher error rate and less accuracy. When the clock frequency decreased in digitally controlled delta modulation (DCDM), the sampling frequency decreased, loading to have longer sampling periods and fewer samples taken per second, potentially leading to larger errors, while step size can be dynamic to optimize the encoding process.

Part 3: Pulse height in Linear Delta Modulation (LDM)

The following circuit was connected as shown in the following figure. The clock frequency was set to 50 kHz, and the sine signal with message frequency (fm=100 Hz), and amplitude (Vss = 1V), and the bridging plug was set to the linear delta modulation (at the input of the integration).

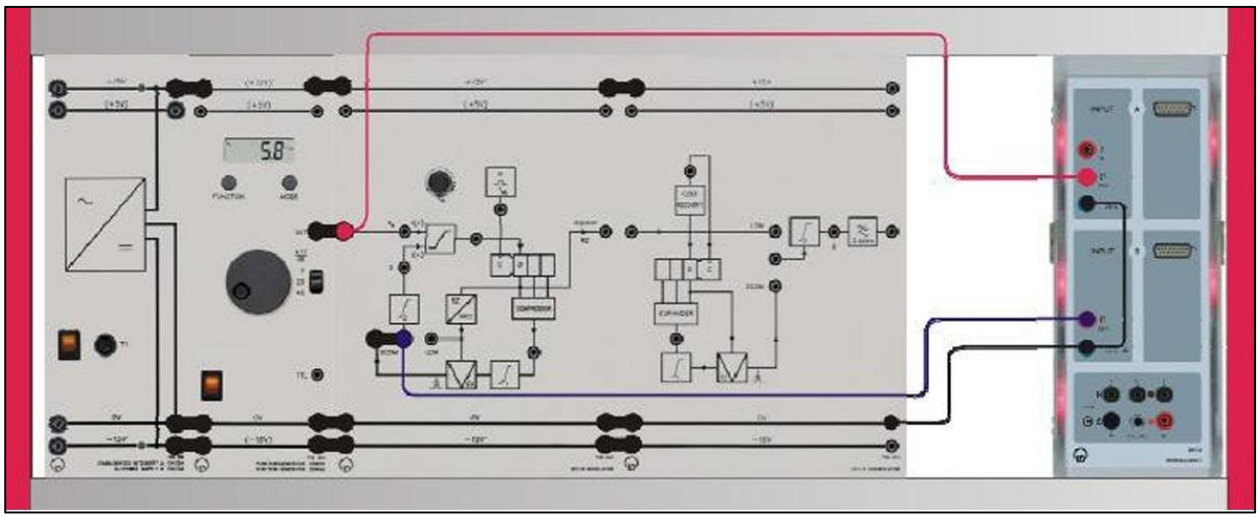


Figure 12 Pulse Height in LDM.

3.1 When the clock frequency is 50 kHz

3.1.1 Pulse height in linear delta modulation for the output signal

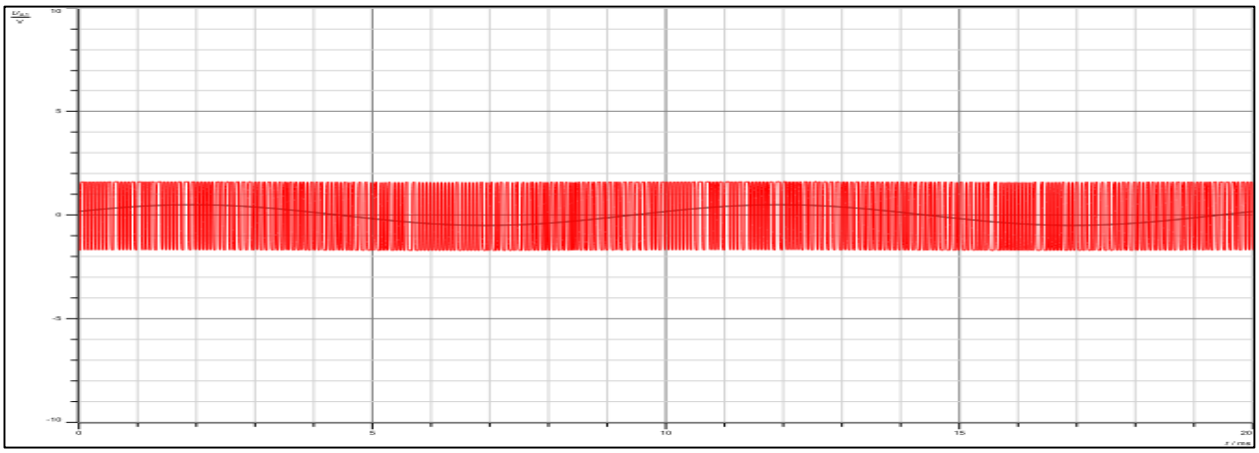


Figure 13 Pulse height in LDM when Vss=1 Volt for the output signal, freq = 50 kHz.

And when the input amplitude voltage was changed form **1 Volt** to **7 Volt,** the following figure shows the result:

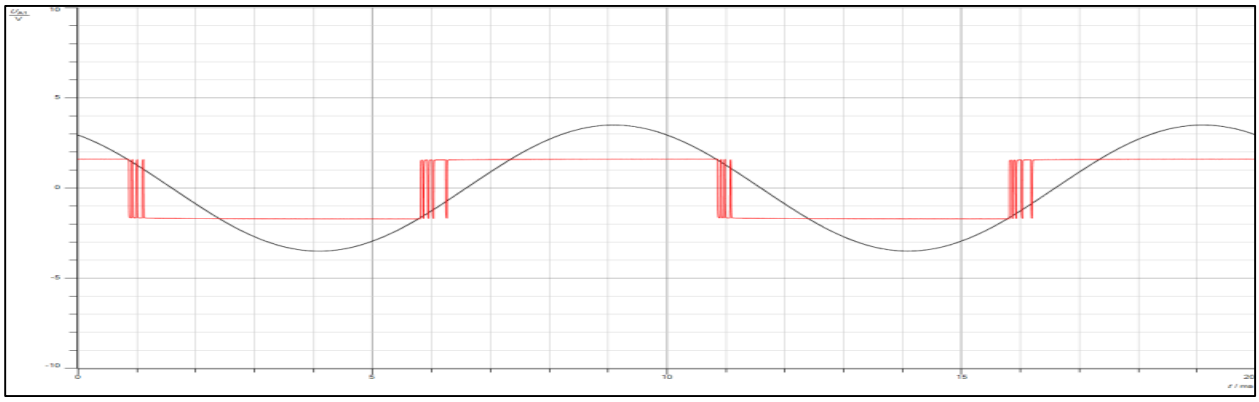


Figure 14 Pulse height in LDM when changing the Vss to 7 Volt for the output signal, freq = 50 kHz..

3.1.2 Pulse height in linear delta modulation for the predicted signal

Now, the same circuit connection was used again for the predicted signal of the linear delta modulation (LDM) which is the output of the integration $\int 2$. The following figures shows the pulse height of the predicted signal when input amplitude voltage equals 1 Volt, and 7 Volts.

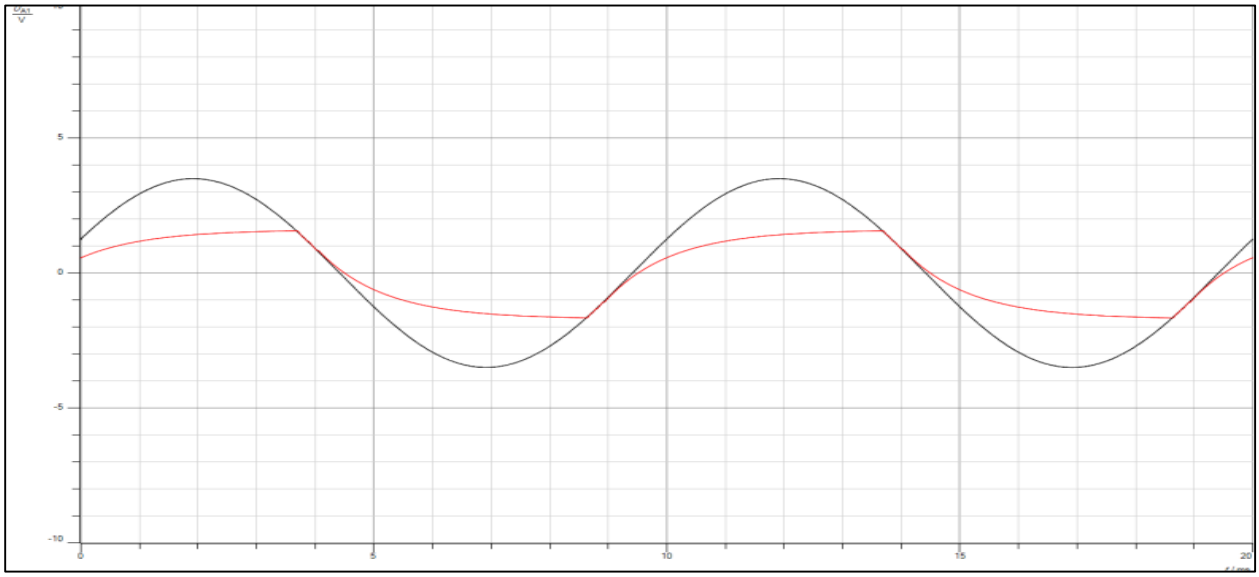


Figure 15 Pulse height in LDM when changing the Vss to 7 Volt for the predicted signal, freq = 50 kHz.

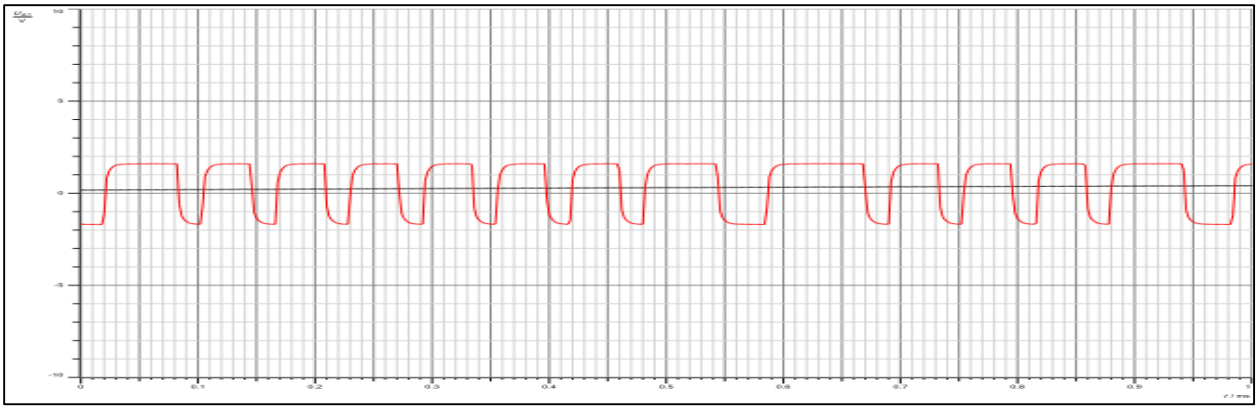


Figure 16 Pulse height in LDM when Vss = 1 Volt for the predicted signal, freq = 50 kHz.

3.2 When the clock frequency is 30 kHz

In this step, the connection was kept the same, but the clock frequency was changed to the 30 kHz.

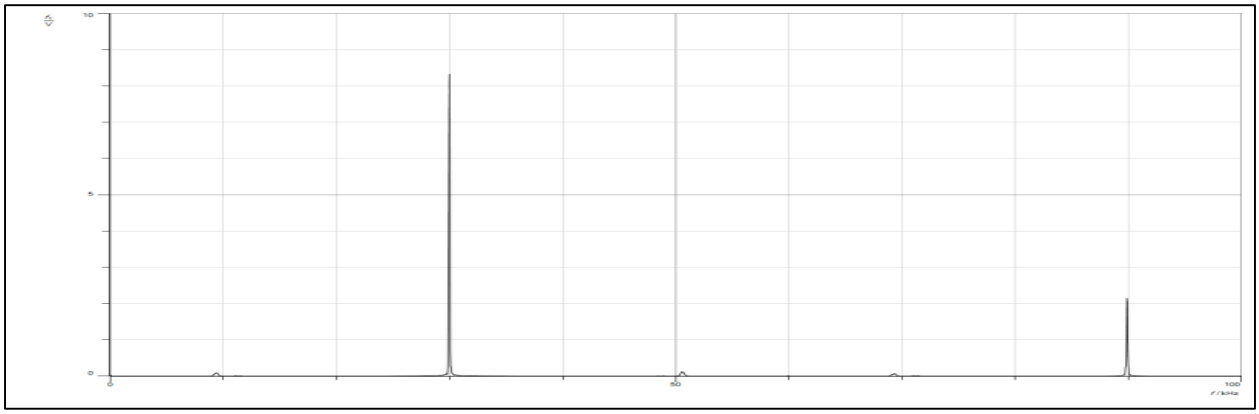


Figure 19 When changing the clock frequency to 30 kHz.

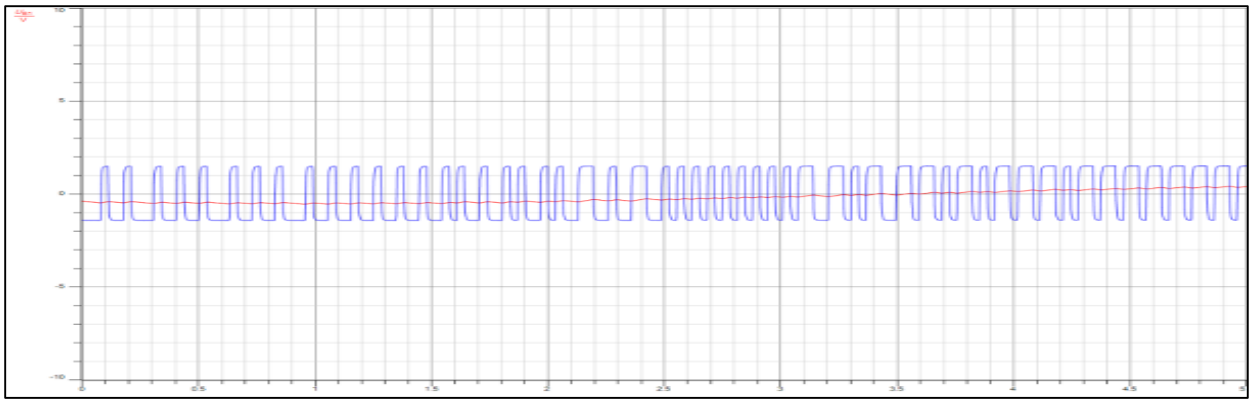


*Figure 18 Pulse height in LDM when the Vss =1 V for the predicted signal, freq = 30 kHz**.*

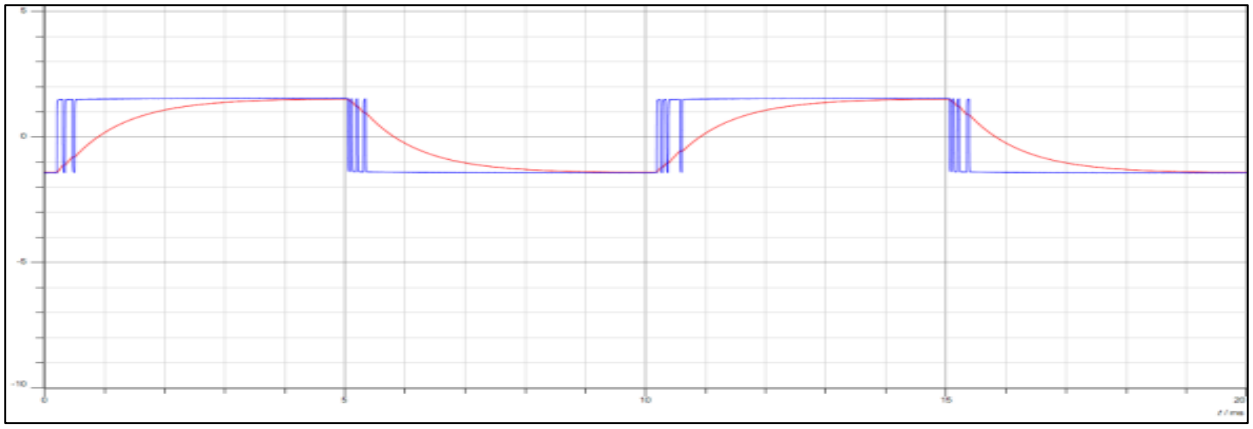


*Figure 20 Pulse height in LDM when the Vss =7 Volt for the predicted signal, freq = 30 kHz**.*

***Note: I have used the previous 2 figures from previous data and report since we forgot to take them unfortunately.*

From the previous results, it is noticed that there is a relation between the input amplitude value (Vss) and the pulse height for both the output signal and the predicted one. The relation between the input voltage and the pulse height is that as the amplitude of input signal increases the pulse height increases, which leads to have a higher accuracy and decrease the noise on the signal. The same thing for the predicted signal of the Linear Delta Modulation (LDM), when increasing the amplitude we get a higher pulse height. As a result, the pulse height is dependent on the input signal Sm(t).

Moreover, there is a relation between the pulse highest rate of activity of the Linear Delta Modulation (LDM) and the slope of the of Sm(t) which is a larger slope or faster rate of change results in a higher pulse rate of activity in the LDM output signal.

Part 4: Pulse height in Digital Controlled Delta Modulation (DCDM)

In this step, the objective is to study the effect of the amplitude input signal on the pulse height in digital controlled delta modulation (DCDM). The same previous circuit was kept, but the bridging plug was set to (DCDM).

4.1 When the clock frequency is 50 kHz

4.1.1 Pulse height in digital controlled delta modulation for the output signal

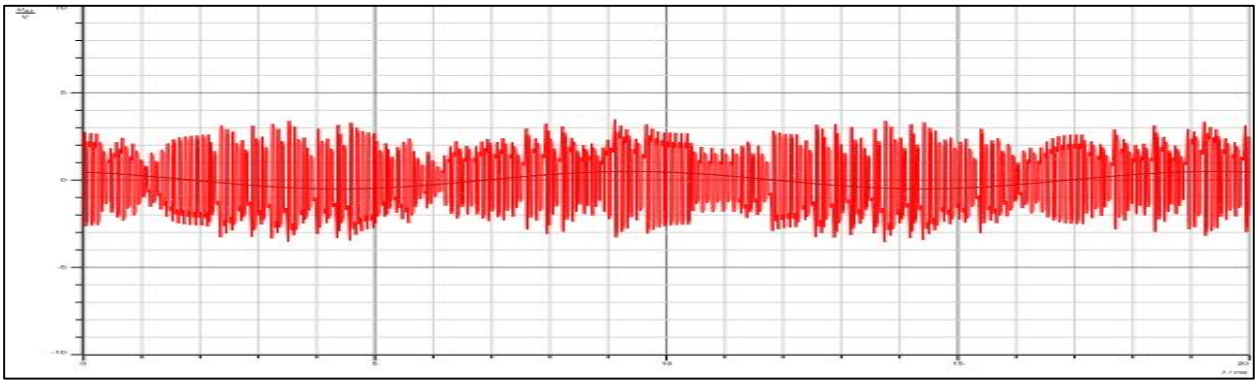


Figure 22 Pulse height in DCDM when Vss=1 Volt for the output signal, freq = 50 kHz.

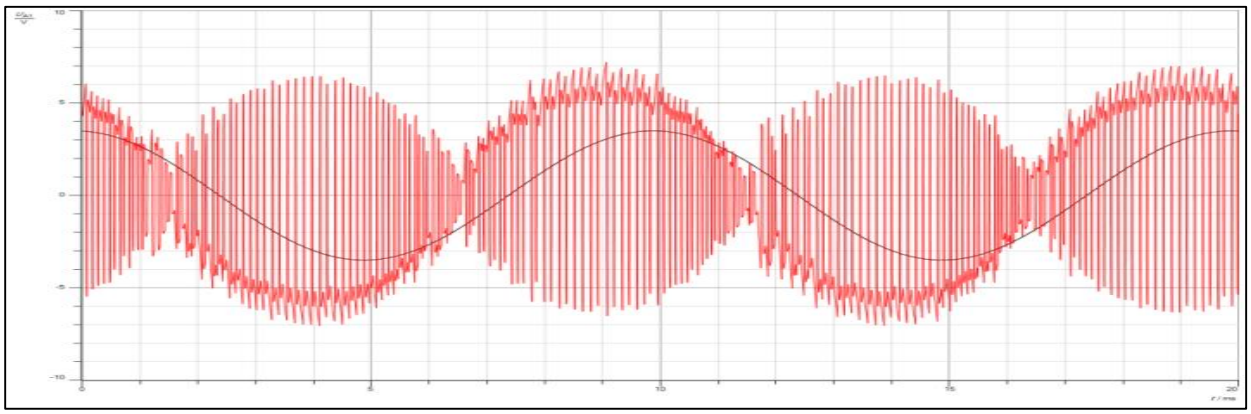


Figure 21 Pulse height in DCDM when Vss=7 Volt for the output signal, freq = 50 kHz.

4.1.2 Pulse height in digital controlled delta modulation for the predicted signal

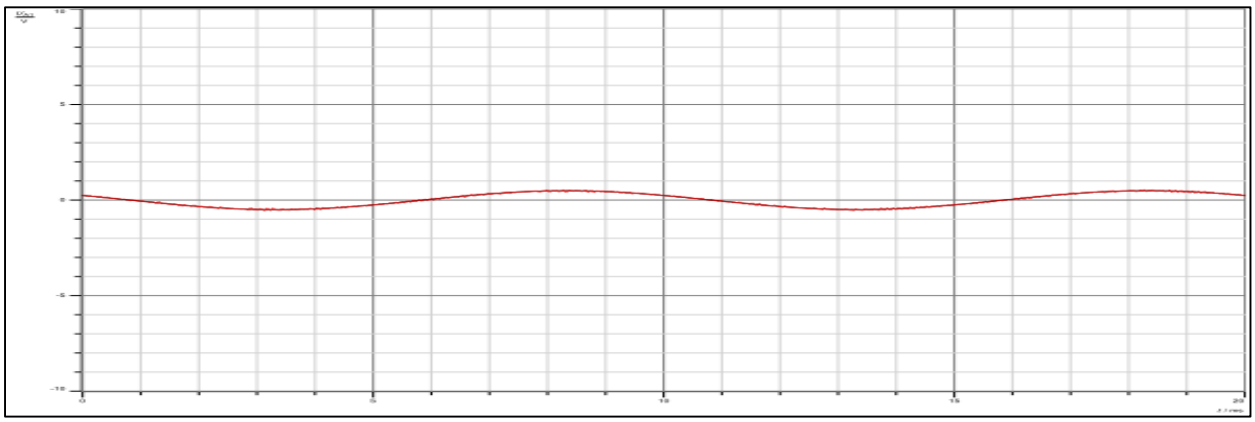


Figure 23 Pulse height in DCDM when Vss=1 Volt for the predicted signal, freq = 50 kHz.

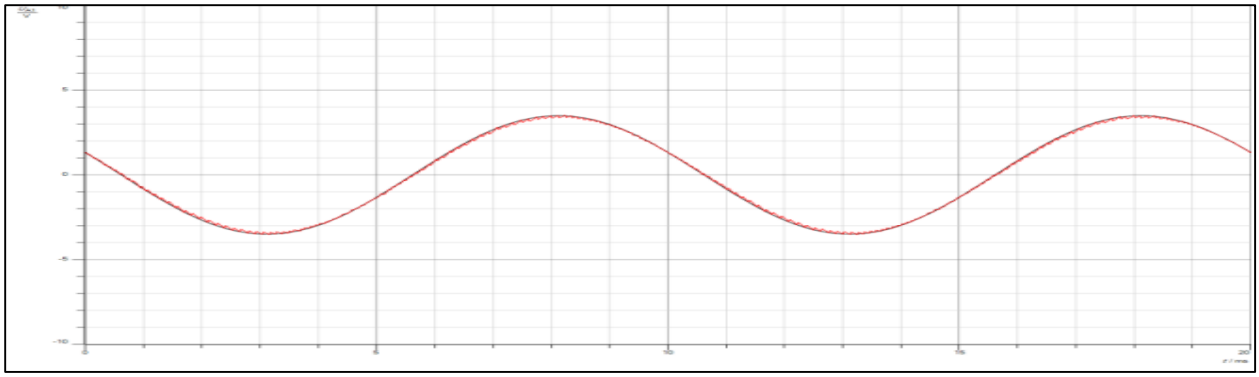


Figure 24 Pulse height in DCDM when Vss=7 Volt for the predicted signal, freq = 50 kHz.

4.2 When the clock frequency is 30 khz

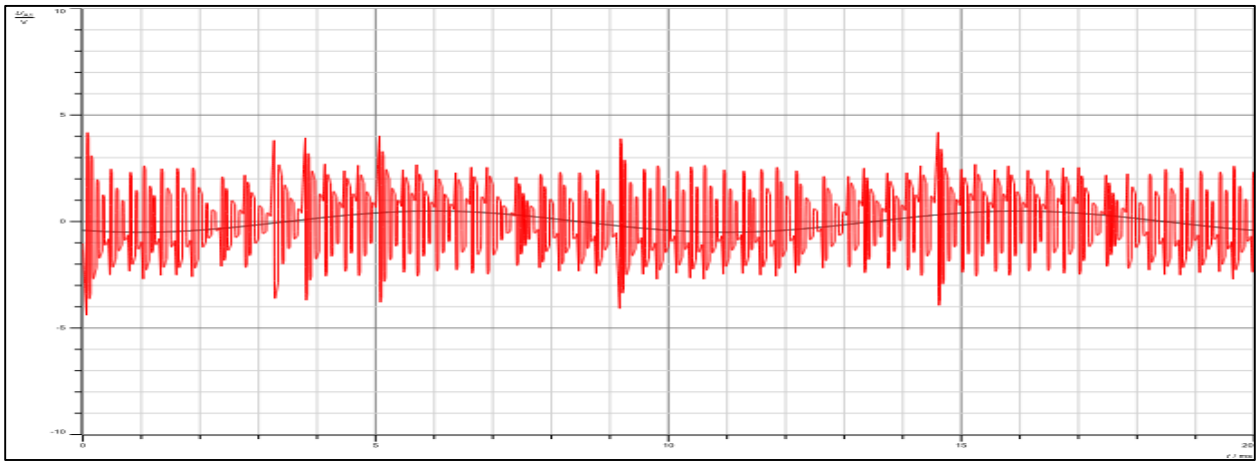


Figure 25 Pulse height in DCDM when the Vss =1 Volt for the predicted signal, freq = 30 kHz.

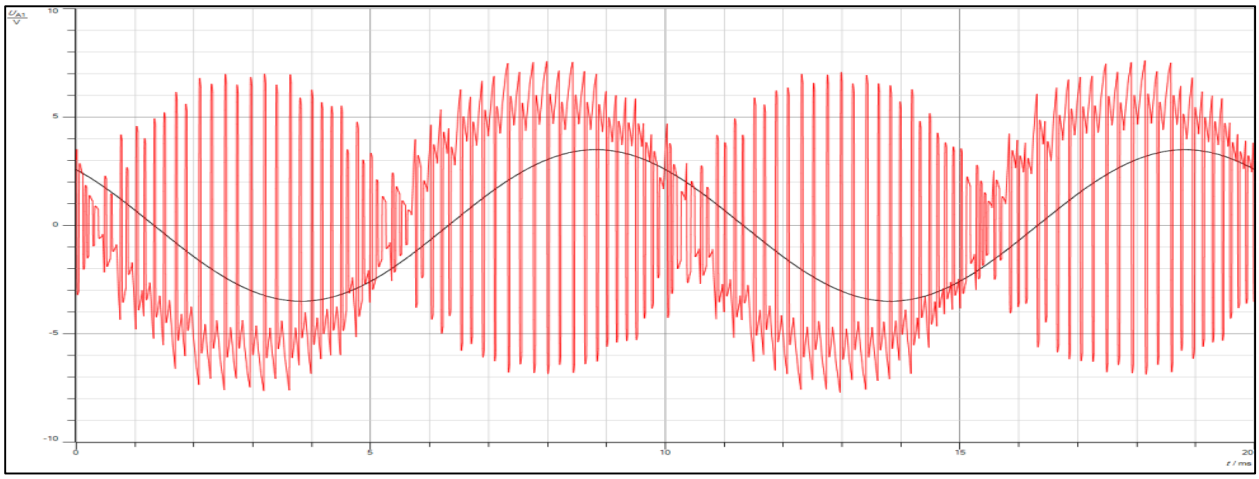


Figure 26 Pulse height in DCDM when the Vss =7 Volt for the predicted signal, freq = 30 kHz.

From the above figures, it is shown that the pulse height in digital controlled delta modulation (DCDM) depends on the amplitude of the input signal. When the input signal has a smaller value, the step size becomes smaller which leads to have a smaller pulse height. In contrast, when the signal has a higher value of the amplitude, the pulse height becomes larger.

Part 5: Output signals of the LDM modulator (RZ/NRZ)

The aim of this part is to find the type of signals used to represent the modulated delta signal and the signal used in the feedback path to generate the prediction. To achieve this goal, the following circuit was connected:

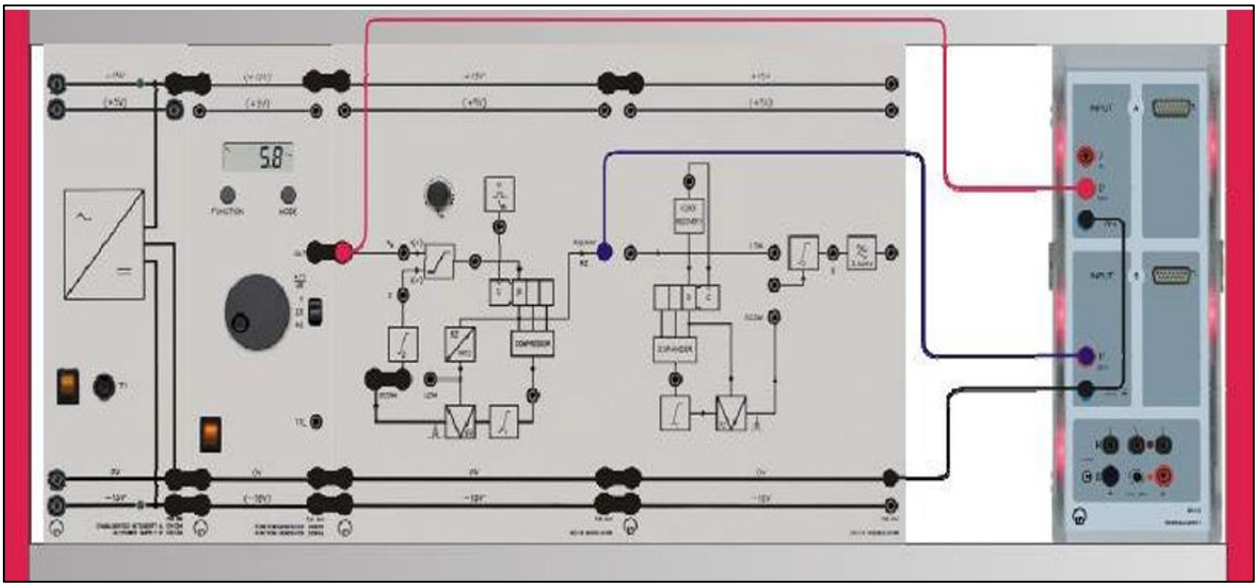


Figure 27 LDM modulator (RZ/ NRZ) circuit.

The clock frequency was set to its minimum value (f = 10 kHz). And the function generator was set to generate the sine wave with message frequency equals to 100 Hz, and amplitude 1 Volt. Finally, the bridging plug was connected to LDM, and the CASSY Sensor UB1 to the DM signal at the output of DM modulator (bipolar, RZ) while CASSY Sensor UA1 to the LDM signal (at the input of ∫2).

The previous connection, and settings was run into the Cassy Lab software, and the following signal represents the output of the delta modulator. It is shown that the output signal represents the "bipolar" encoding scheme used for representing the output signal. In bipolar LDM, the quantized samples are represented by pulses that can have both positive and negative polarities.

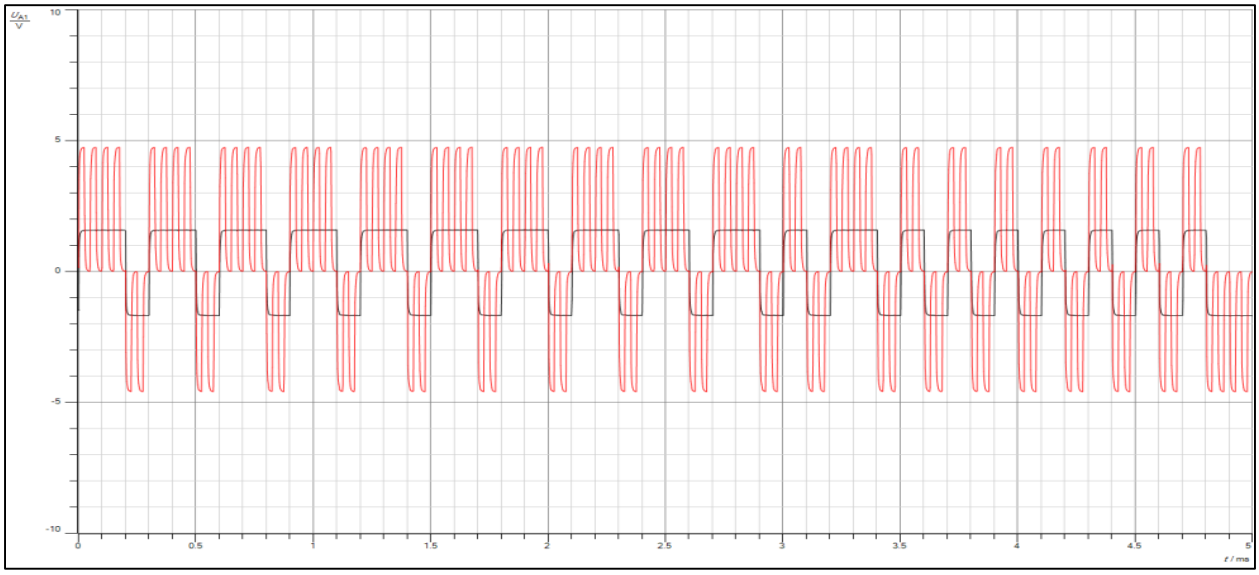


Figure 28 Output signal of the LDM modulator (RZ/NRZ).

Part 9: Granular noise in LDM

In this part, the concept of granular noise which is one of the Delta Modulation (DM) drawbacks will be studied for Linear type (LDM). To carry out this part, the following circuit was connected. The clock frequency (f clock) was set to its minimum value which is10 kHz and the function generator was set also to pulse train with message frequency equals 200 Hz, amplitude (Vss = 2 Volt), and duty cycle equals 50%.

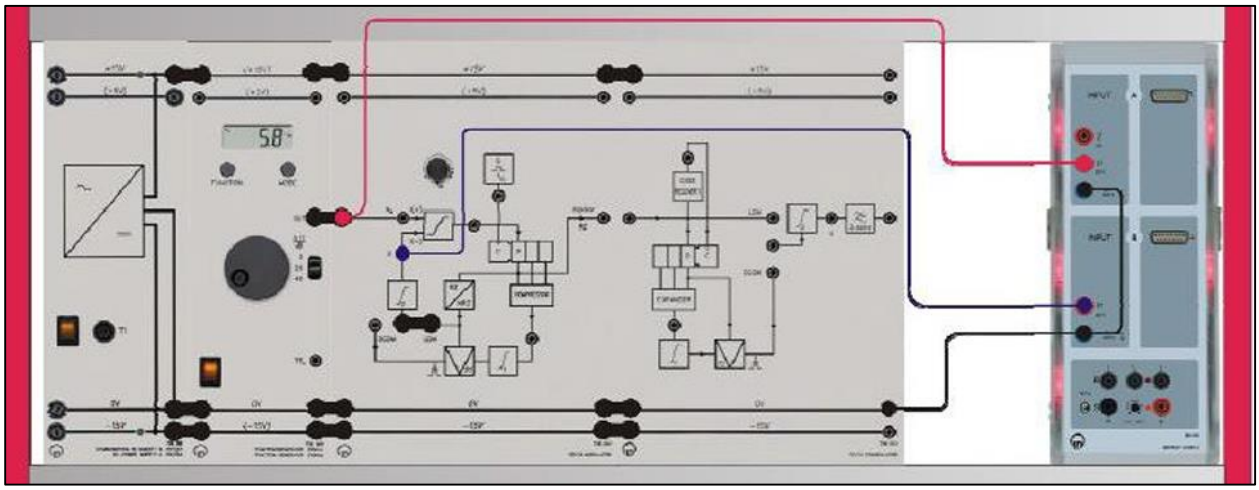


Figure 29 Granular Noise in LDM circuit.

Moreover, The bridging plug was connected with the LDM, the Cassy UA1 was connected to the modulating signal, and UB1 to the predicted signal (output of ∫2).The following figures represent the results.

9.1 When connecting the delta modulator to the LDM

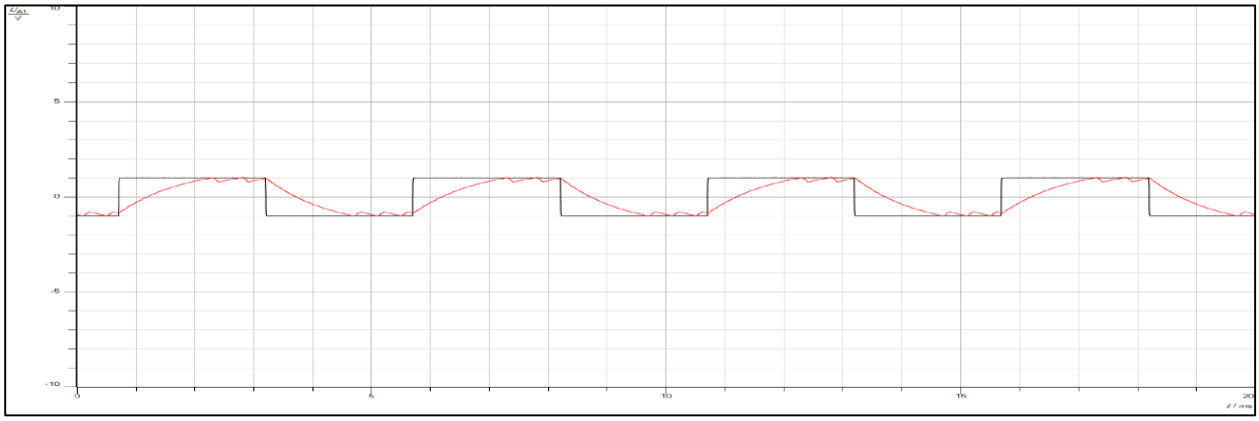


Figure 30 Granular noise in the predicted signal X(t) when f clock = 10 kHz (min).

After that, the clock frequency was changed to **30 kHz** and **100 kHz (max**), and the simulation started again,

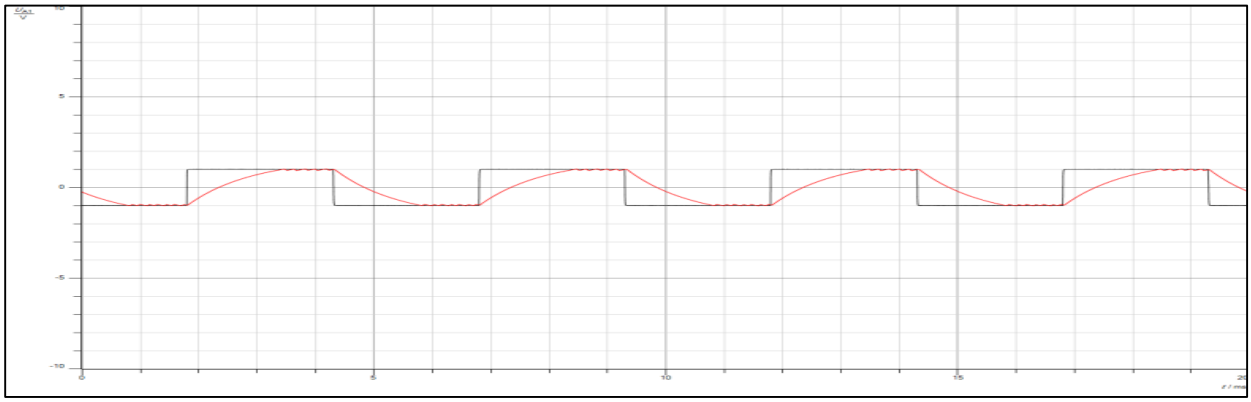


Figure 31 Granular noise in the predicted signal X(t) when f clock = 30 kHz.

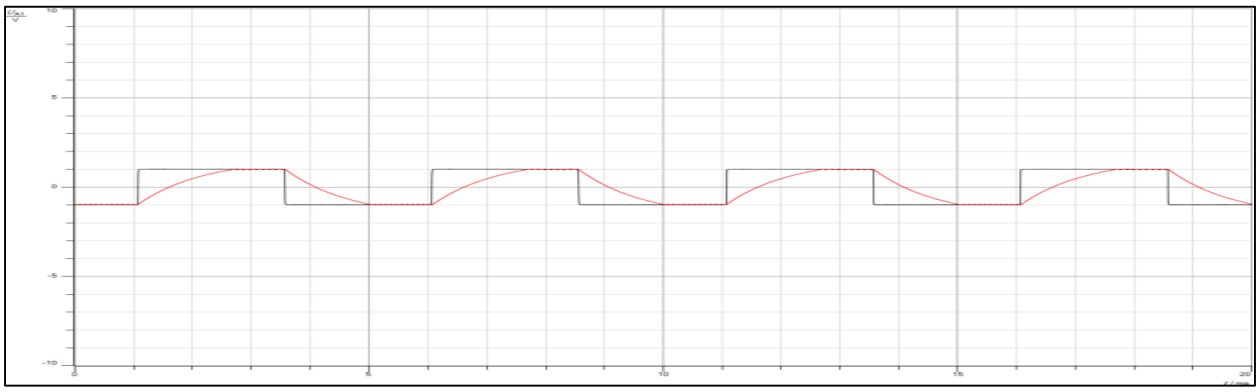


Figure 32 Granular noise in the predicted signal X(t) when f clock = 100 kHz(max).

9.2 When connecting the delta modulator to the ground

Now, the input of the delta modulator was connected to the ground and the frequency clock was set again to its minimum value (fclock = 10 kHz), then changed to its maximum value (fclock = 100 kHz), the recorded results are as the following:

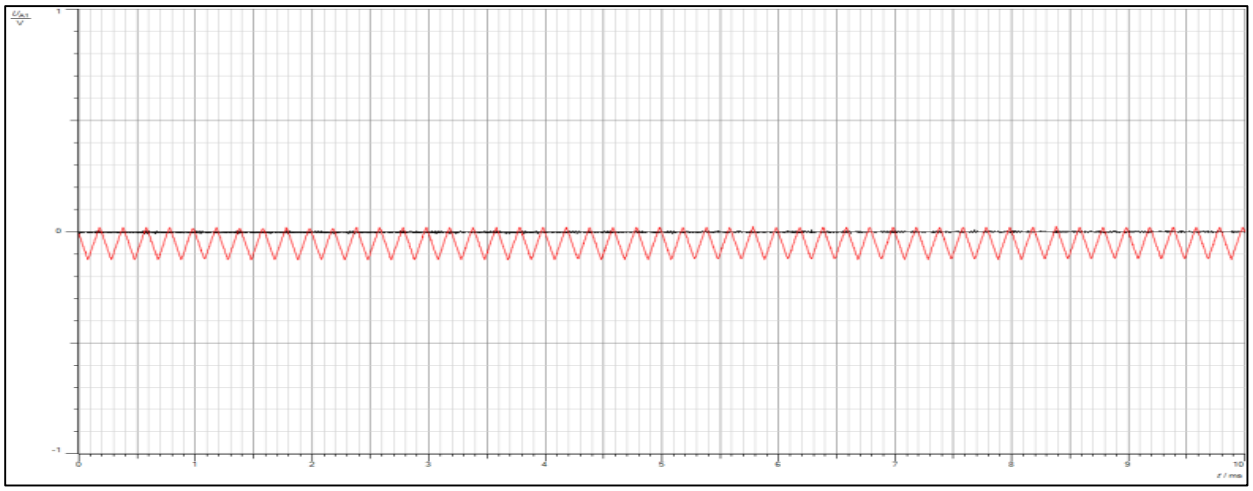


Figure 33 Granular noise in the predicted signal X(t) when f clock = 10 kHz (min).

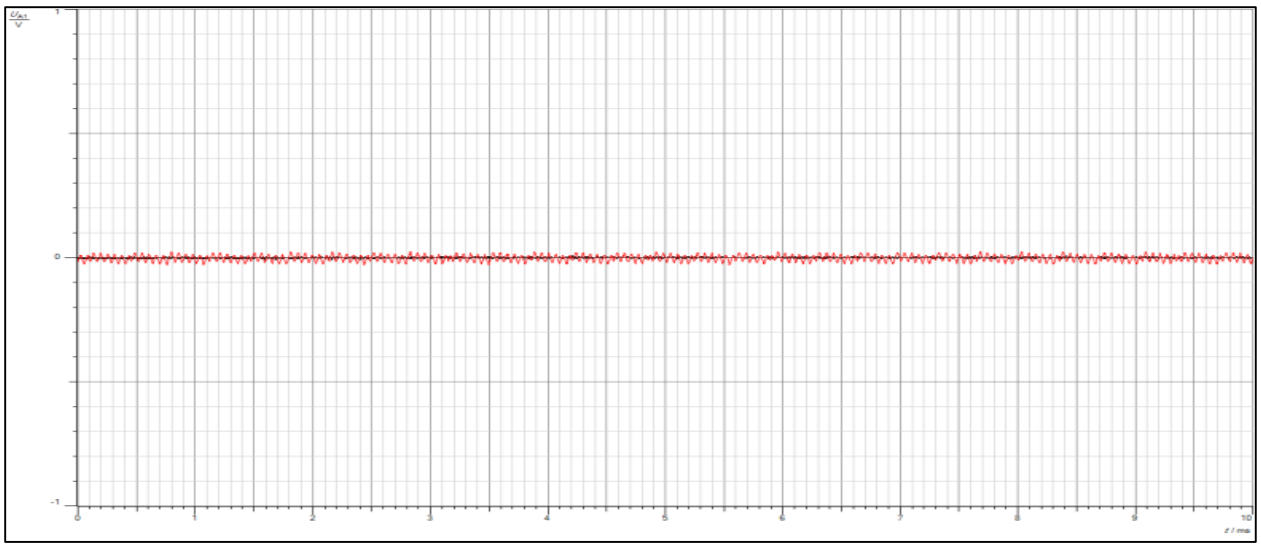


Figure 34 Granular noise in the predicted signal X(t) when f clock = 100 kHz(max).

Based on the previous results in (9.2 and 9.2), it is noticed that the granular noise (which represented in the red line) in the linear delta modulation (LDM) increase by decreasing the value of the clock frequency. In other words, they are **inversely** proportional.

Part 10: Granular noise in DCDM

In this part, the same previous circuit connections was used. The only difference is that the bridging plug was set to DCDM (input of ∫2). The same previous steps were applied again, the following figures represent the results in terms of digital controlled delta modulation (DCDM) when changing the value of the clock frequency to 10 kHz, 30 kHz, and 100 kHz.

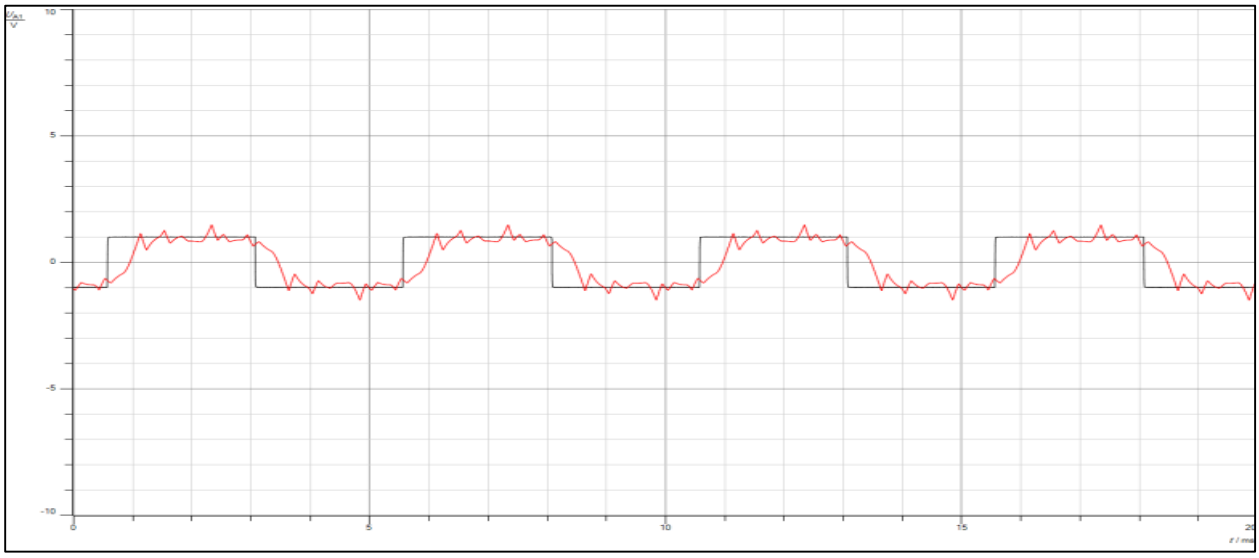


Figure 35 Granular noise in the predicted signal X(t) when f clock = 10 kHz (min).

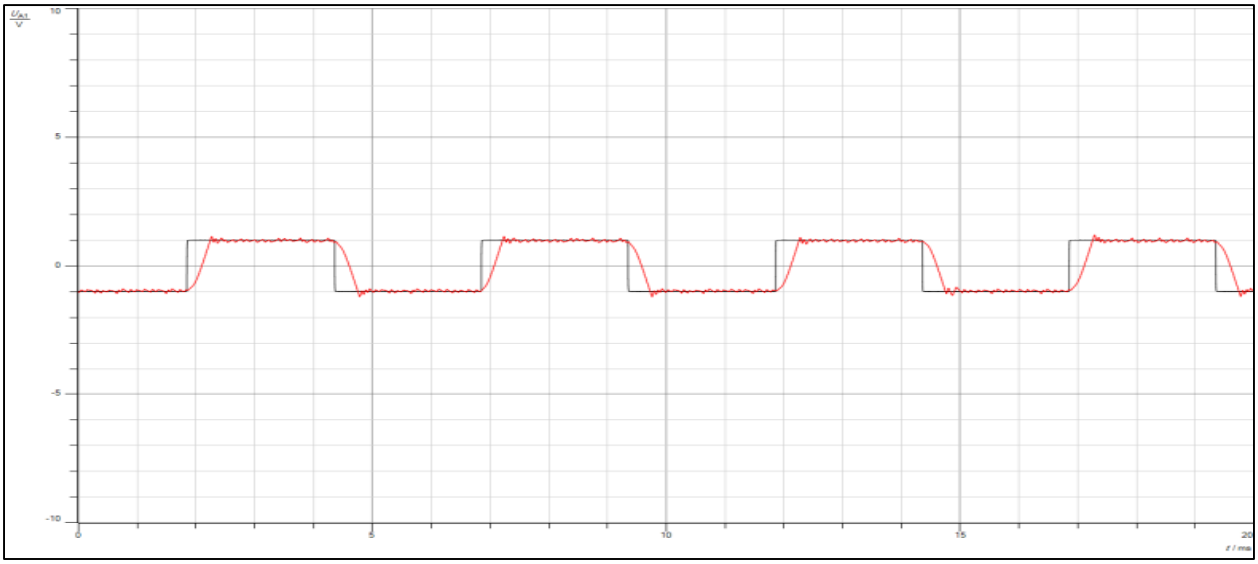


Figure 36 Granular noise in the predicted signal X(t) when f clock = 30 kHz.

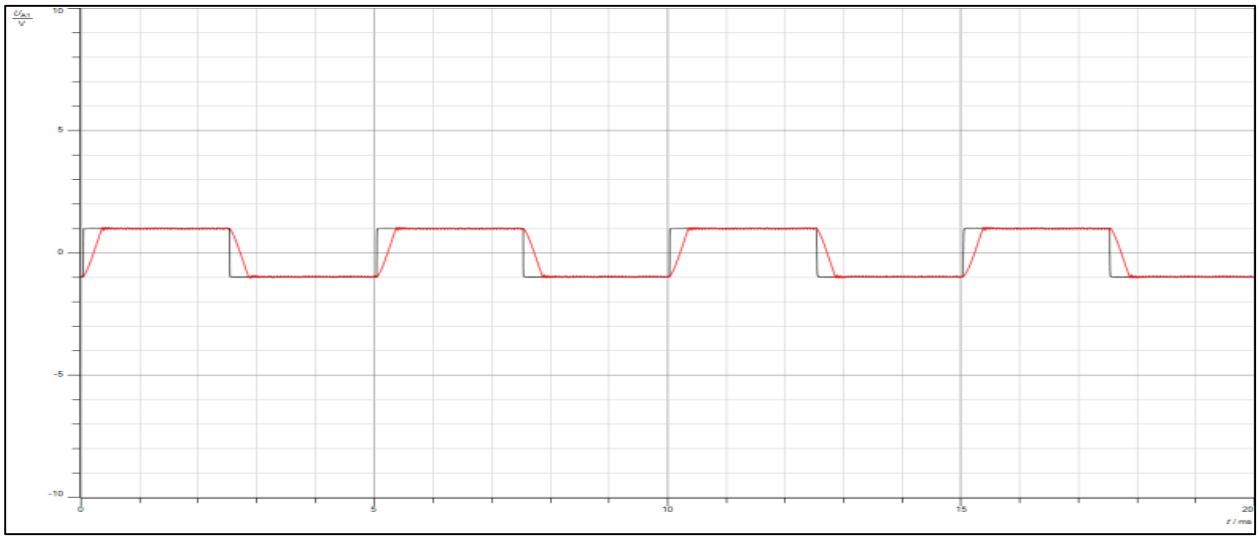


Figure 37 Granular noise in the predicted signal X(t) when f clock = 100 kHz(max).

It is noticed that the results are the **same** as the previous part (LDM).

Part 11: Slope-overload in LDM

The circuit of this part was connected as shown in the following circuit. The clock frequency was set to its maximum value (100 kHz), and the sine wave signal with frequency 100 Hz, and amplitude of 4 Volt was generated by the function generator. Finaly, the bridging plug was connected to LDM, and the measurement was started.

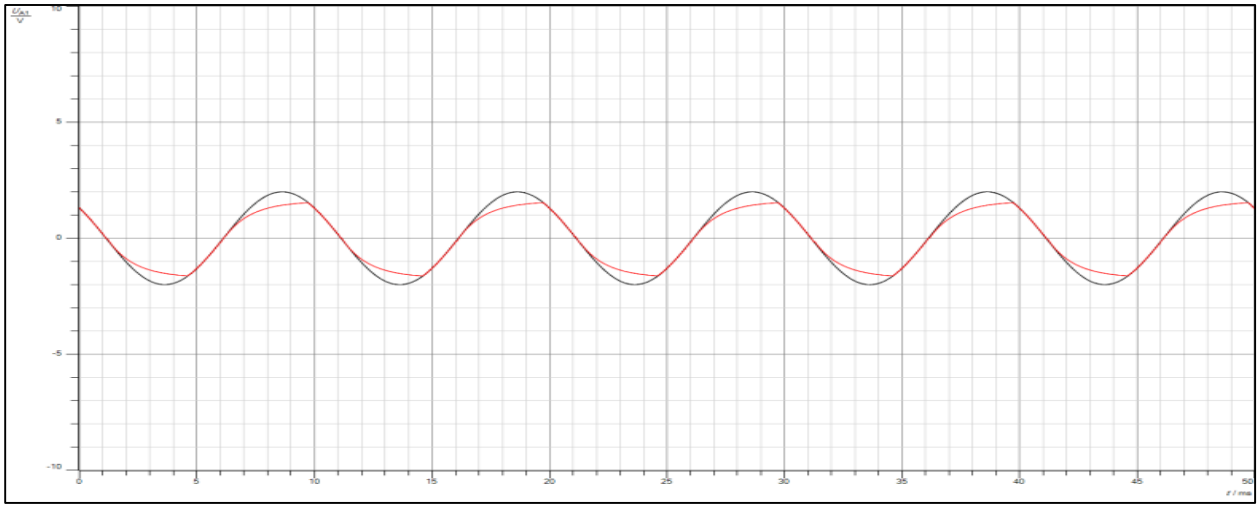


Figure 38 The slop-overload distortion of the sine wave predicted signal in LDM.

After that, the function generator was set to generate pulse train message signal with the same amplitude and frequency, added by 20% duty cycle.

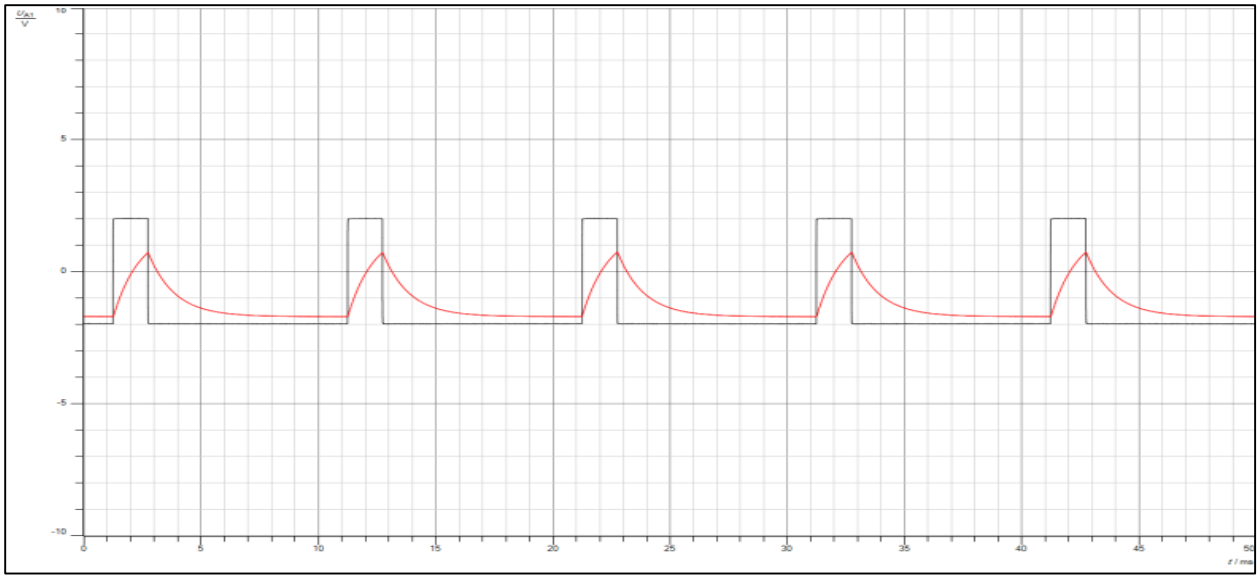


Figure 40 The slop-overload distortion of the pulse train wave predicted signal in LDM when duty cycle 20%.

When changing the duty cycle to 80%, the result is as the following:

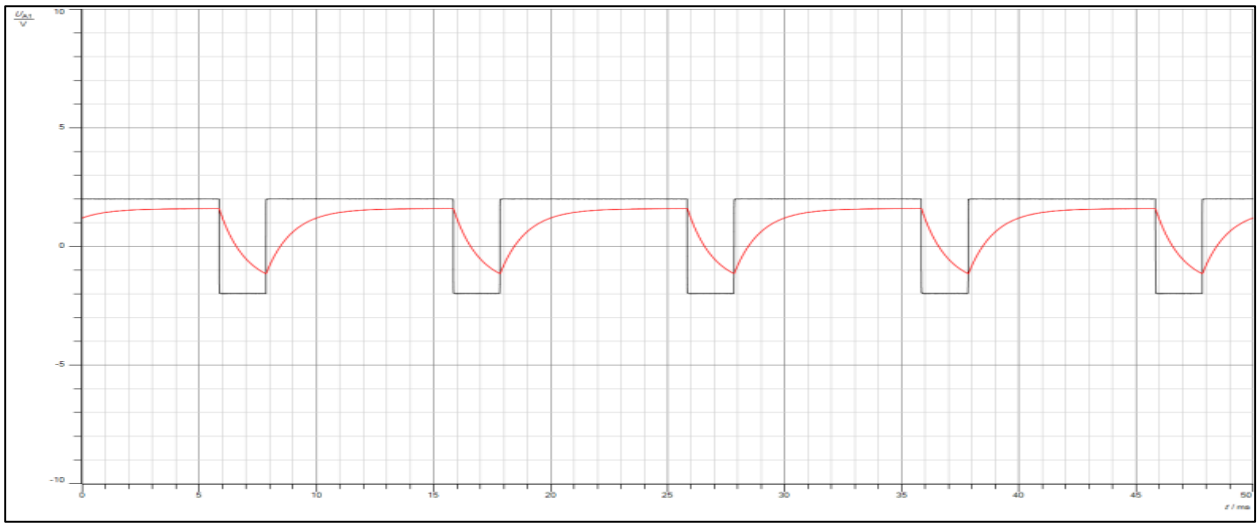


Figure 39 The slop-overload distortion of the pulse train wave predicted signal in LDM when duty cycle 80%.

The previous results show the slop overload of the predicted signal (output signal) when the input signal is a sine wave or pulse train input signal. It is shown that when increasing the value of the duty cycle, in other words, increasing the **ON** period in the pulse train input signal, the slop overload of the output signal decrease. In contrast, the signal with a smaller duty cycle value has a high slope overload in the output signal in Linear Delta Modulation (LDM).

Part 12: Slope-overload in DCDM

The previous circuit connection was used again in this part, but the amplitude was increased to 9 Volt. In addition, the bridging plug was set to DCDM. The following figures represent the results after repeating the measurements of the previous part.

The first result when the input signal is a sine wave:

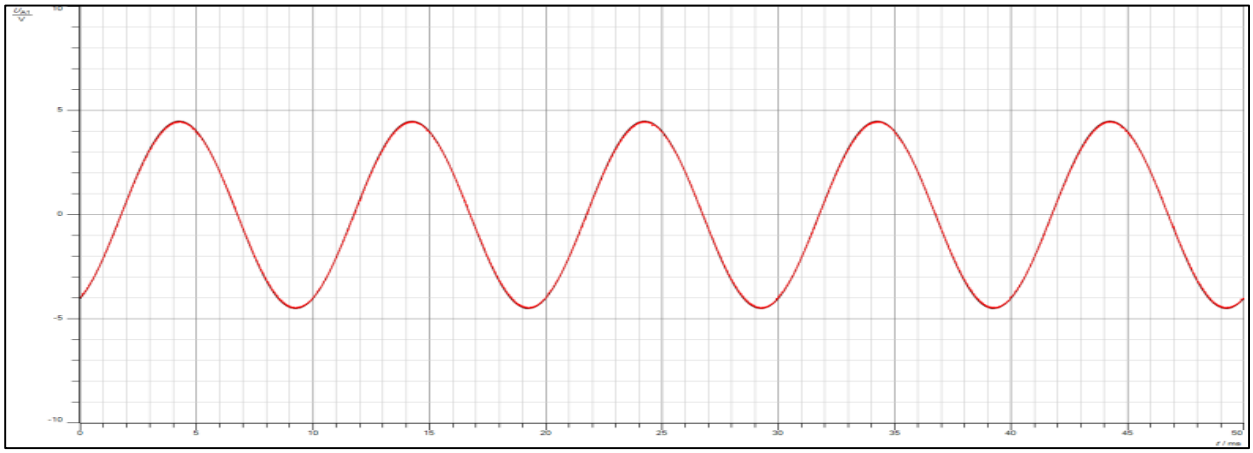


Figure 41 The slop-overload distortion of the sine wave predicted signal in DCDM.

After that, the function generator was set to generate pulse train message signal with the same amplitude and frequency, added by 20% duty cycle.

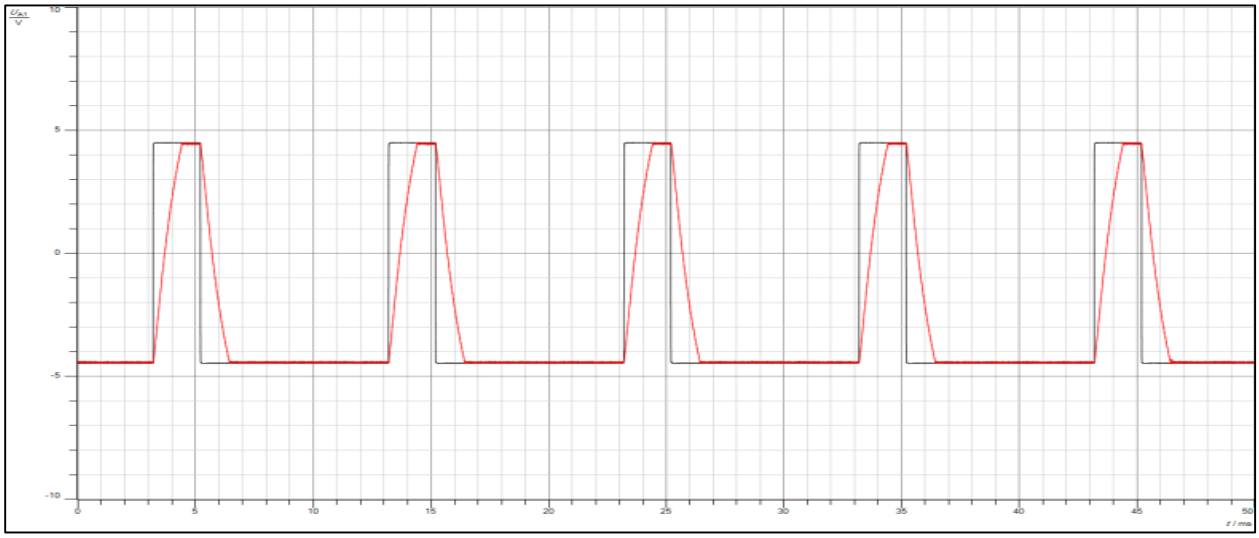


Figure 42 The slop-overload distortion of the pulse train wave predicted signal in DCDM when duty cycle 20%.

And when changing the duty cycle to 80%:

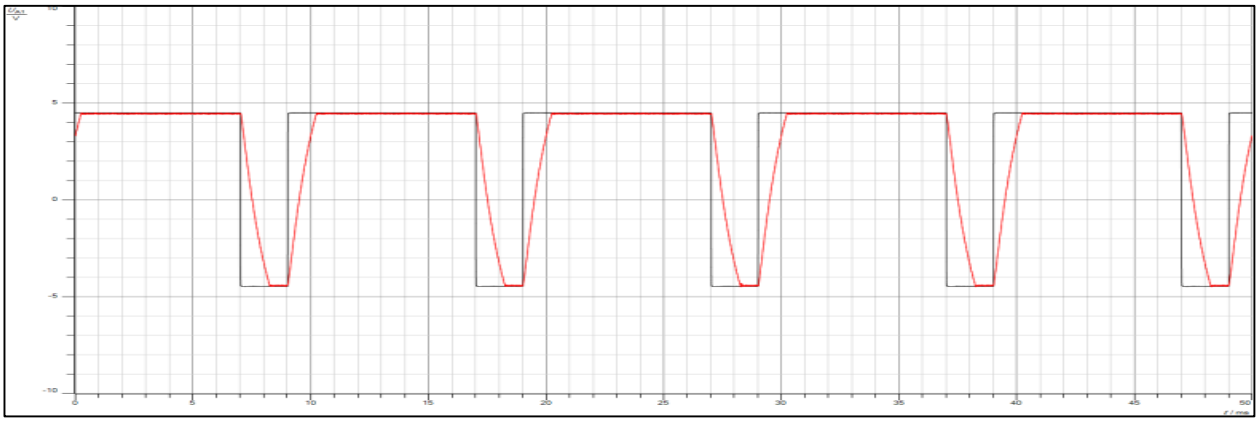


Figure 43 The slop-overload distortion of the pulse train wave predicted signal in DCDM when duty cycle 80%.

As noticed from the previous results, it is shown that the digitally controlled delta modulation (DCDM) has a less degree of slop-overload in both input signal types, the sine wave, and the pulse train than the LDM. This is due to the consistency of the step size in the LDM, in contrast, the DCDM is dynamic, which leads to having a less effect on the slop overload on the predicted signal.

Part 13: Dynamic of LDM and DCDM

In objective of this part is to determine the maximum value of the input voltage for a given frequency which slop overload can be avoided for both delta modulation types, LDM and DCDM. To carry out it, the following circuit was connected, and the clock frequency was set to its maximum value. Additionally, the function generator was set to produce a sine wave input signal with frequency (f =100 Hz), and amplitude (Vss = 1 Volt).

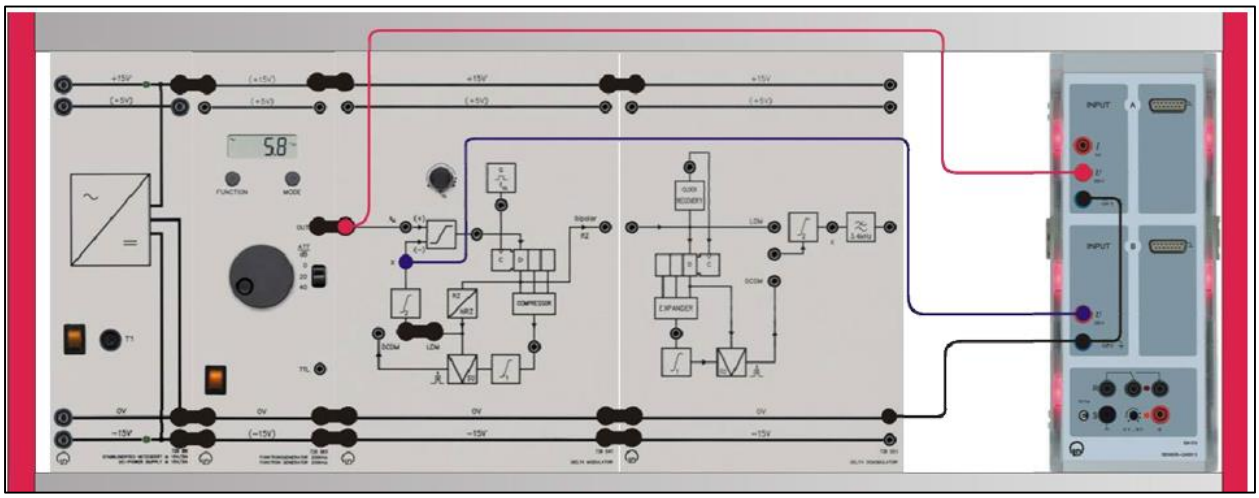


Figure 44 Dynamic of LDM and DCDM circuit connection.

The input voltage was increased gradually until the predication signal X(t) shows the beginning of the slop overload. The following table contains the results when repeating the measurements for the frequency of Sm(t) signal of 200,300,400,500,1000,2000 Hz.

Table 1 Max values of the input voltage in LDM.

Frequency (Hz)	**100**	**200**	**300**	**400**	**500**	**1000**	**2000**
Amax	3.1	2.3	2.2	1.8	1.4	0.7	0.4
D	37.78	35.19	34.8	33.06	30.88	24.86	20

While in the DCDM, the following results were obtained:

Table 2 Max values of the input voltage in DCDM.

Frequency (Hz)	**100**	**200**	**300**	**400**	**500**	**1000**	**2000**
Amax	16.7	12.2	8.4	6.3	5.8	2.8	1.5
D	52.41	49.68	46.44	43.94	43.22	36.90	31.48

For each Amax value, the **Dynamic (D)** was calculated using the following equation:

Equation 1 Dynamic (D) equation.

$$\boldsymbol{D = 20\log(\frac{Amax}{Amin})\ dB, assuming\ that\ Amin = 20m, Vss = 40m.}$$

The next step is to plot the results in **(D Vs. Fm)** for both LDM and DCDM as shown in the following plots:

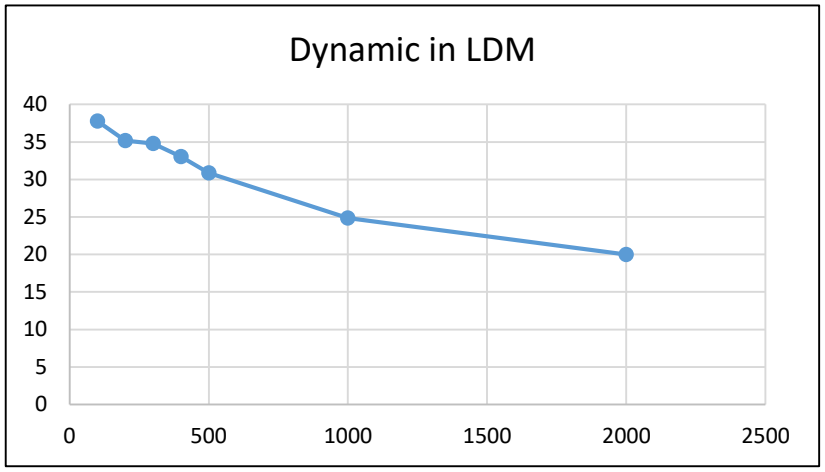


Figure 45 Dynamic Vs. Frequency in LDM.

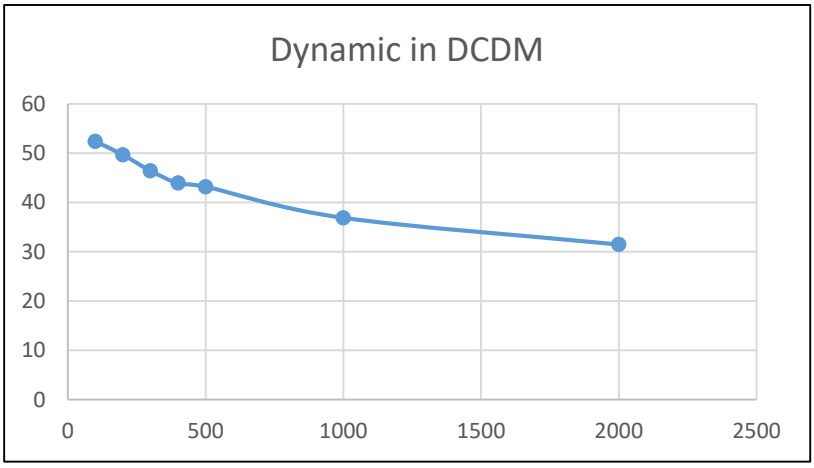


Figure 46 Dynamic Vs. Frequency in DCDM.

From the previous results, it is noticed that the DCDM, the Dynamic values are greater that the values in the LDM because DCDM has a variable step size, while LDM is constant. In addition, when increasing the input message frequency, the maximum amplitude decrease, which leads to decrease also the value of the Dynamic.

Part 15: Demodulation (LDM/DCDM)

The objective of this part is to perform the demodulation process for both types of delta modulation LDM, and DCDM. To perform it, the following circuit was connected, and the clock frequency was set to its maximum value, and the sine wave with amplitude (Vss = 4 Volt), and frequency equals to 100 Hz was generated using the function generator.

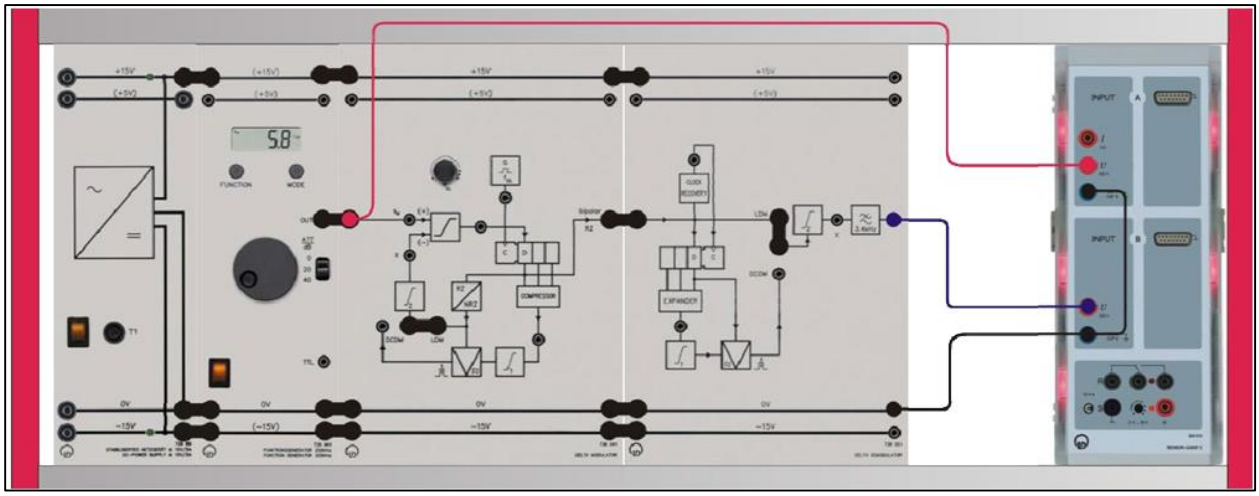


Figure 47 LDM/DCDM Demodulation circuit.

15.1 Demodulation in Linear Delta Modulation (LDM)

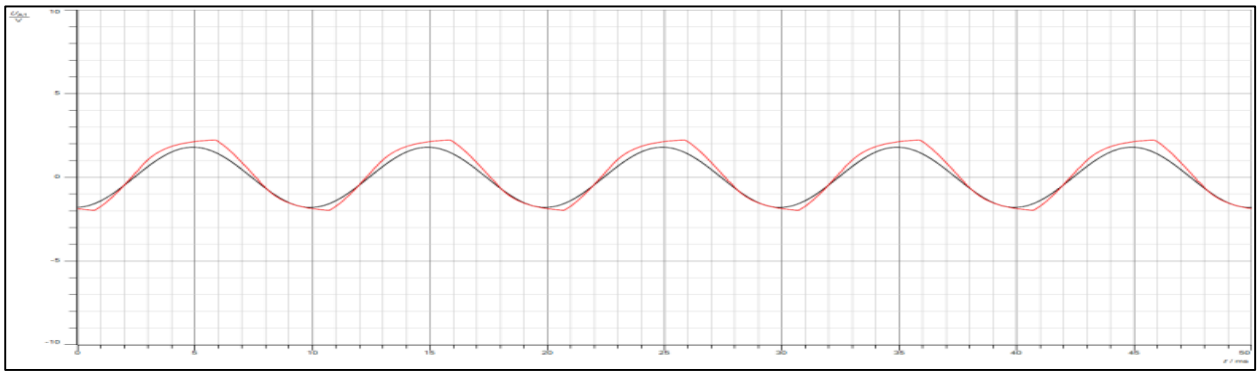


Figure 48 The input sine wave signal and demodulated signal using LDM in time domain f = 100 Hz.

After that, the function generator was set to generate a pulse train signal with duty cycle equals 10%.

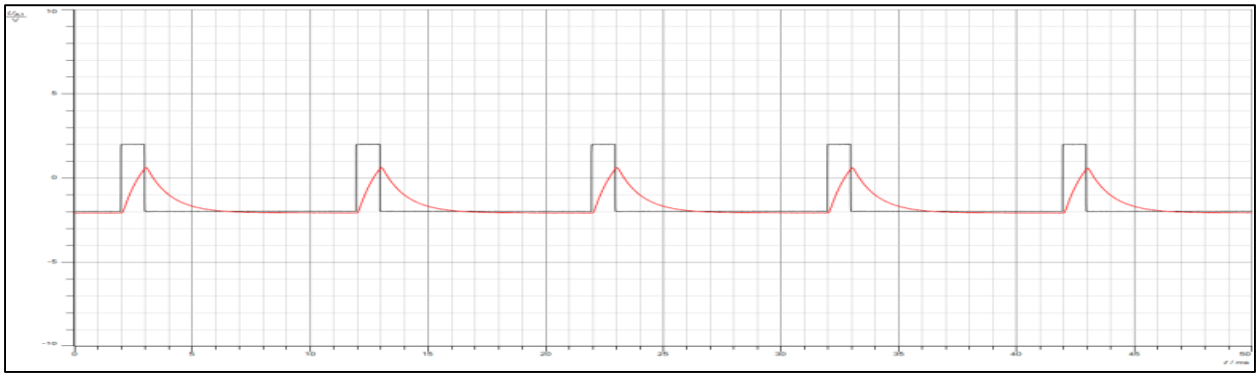


Figure 49 The input pulse train signal and demodulated signal using LDM in time domain, duty cycle = 10%, f=100 Hz.

Finally, it was required to change the input frequency to 300 Hz, and repeat the measurements.

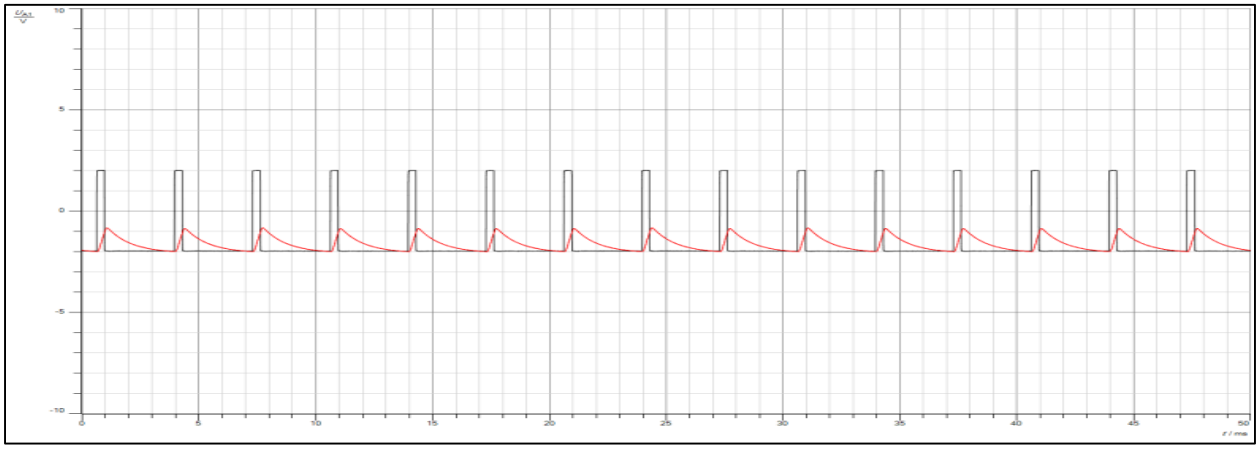


Figure 50 The input pulse train signal and demodulated signal using LDM in time domain, duty cycle = 10%, f=300 Hz.

According to the previous results, it is noticed that the changing the input frequency value affects the demodulated signal, such that increasing the frequency made the demodulated signal becomes too far to the original transmitted signal.

15.2 Demodulation in Digital Controlled Delta Modulation (DCDM)

In this part, the same steps were repeated for DCDM instead of LDM. Firstly, when the input signal is a sine wave, the demodulated signal in DCDM was obtained as the following:

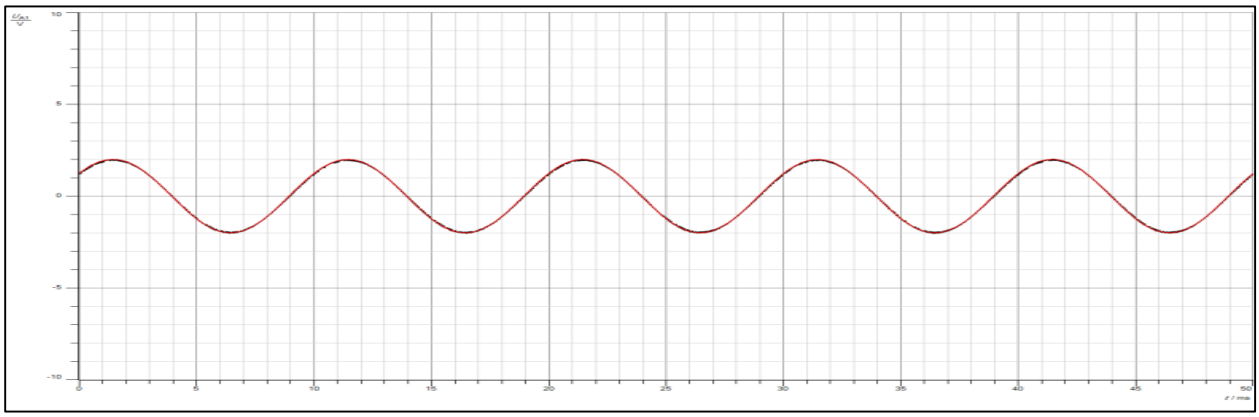


Figure 51 The input sine wave signal and demodulated signal using DCDM in time domain f = 100 Hz.

Now, when changing the input message signal to pulse train with duty cycle = 4%, the demodulated signal was as the following:

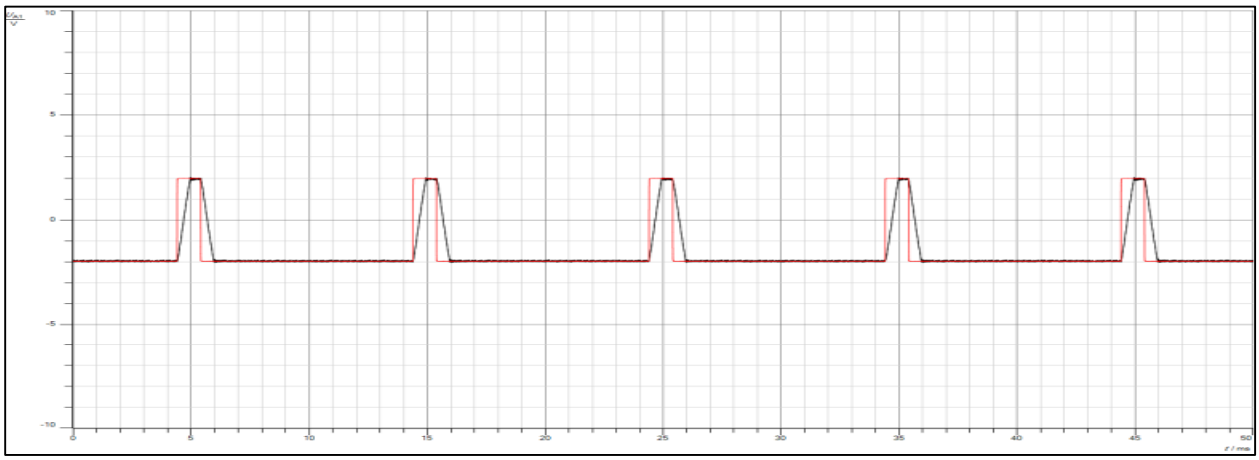


Figure 52 The input pulse train signal and demodulated signal using DCDM in time domain, duty cycle = 10%, f=100 Hz.

Lastly, when changing the input frequency to 300 Hz instead of 100 Hz. The result is as the following:

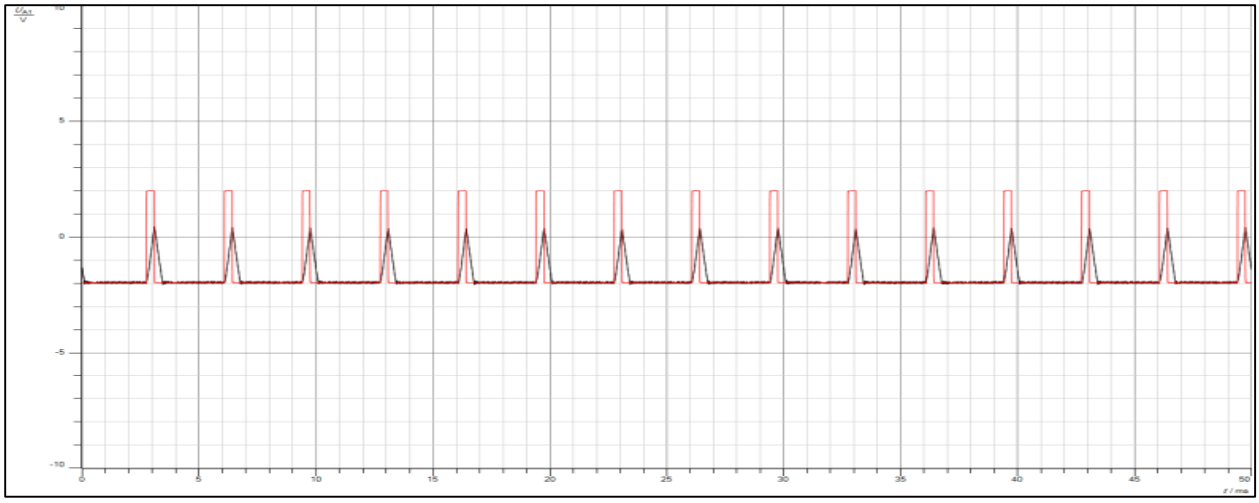


Figure 53 The input pulse train signal and demodulated signal using DCDM in time domain, duty cycle = 10%, f=300 Hz.

From the above results, it is noticed that the demodulated signal in DCDM is closer to the original input signal that using LDM. In addition, changing the input frequency from 100 Hz to 300 Hz affected the demodulated signal such that when increasing the frequency, it makes the demodulated not catching the input signal as appears in figure 53.

Conclusion

In conclusion, this experiment introduced and compared linear delta modulation (LDM) and digital controlled delta modulation (DCDM) techniques. Both linear delta modulation (LDM), and digital controlled delta modulation (DCDM) were examined clearly by generating a sine wave signal practically and comparing it with the predicted signal. Moreover, the concepts of pulse height characteristics for both LDM and DCDM, return-to-zero (RZ), and non-return-to-zero (NRZ) were covered clearly. Also, Granular noise, slope-overloaded, and the dynamic of both linear (LDM) and digital controlled delta modulation (DCDM) was discussed clearly. Finally, the demodulation operation of different input message signals for both types was examined and compared clearly.

References

[1] Hashlamoun, W. (Spring 2020-2021). Communication Slides. Birzeit ; Birzeit University

[2] BYJU'S. "Delta Modulation." Accessed [May 28, 2023]. Available at: https://byjus.com/physics/delta-modulation/

[3] Testbook. "Delta Modulation." Accessed [May 28, 2023]. Available at: https://testbook.com/physics/delta-modulation

[4] ElProCus. "Adaptive Delta Modulation: Block Diagram and Applications." Accessed [May 28, 2023]. Available at: https://www.elprocus.com/adaptive-delta-modulation-block-diagram-and-applications/#:~:text=Adaptive%20delta%20modulation%20decreases%20slope,are%20solved%20using%20this%20modulation .

[5] ElectronicsPost. "What is Slope Overload Distortion and Granular Noise in Delta Modulation and How it is Removed in ADM?" Accessed [May 28, 2023]. Available at: https://electronicspost.com/what-is-slope-overload-distortion-and-granular-noise-in-delta-modulation-and-how-it-is-removed-in-adm/

[6] Google search results for "delta demodulation." Accessed [May 28, 2023]. Available at: https://www.google.com/search?q=delta+demodulation&oq=delta+demodulatin&aqs=chrome.2.69i57j0i13i512l4j0i5i13i30j0i5i10i13i15i30j0i8i13i30l3.5394j0j7&sourceid=chrome&ie=UTF-8

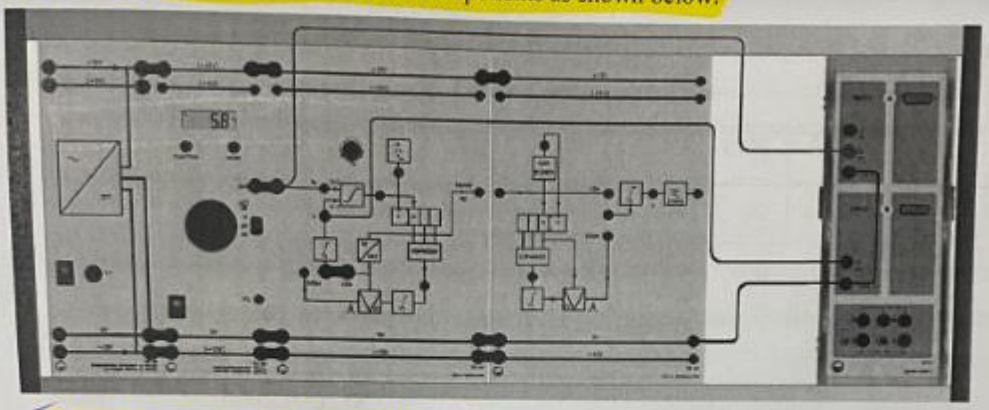
[7] Leybold Shop. "Delta Demodulator." Accessed [May 28, 2023]. Available at: https://www.leybold-shop.com/technology/electrical-engineering/telecommunications-technology/transmission-technology/digital-transmission-technology/modulation-delta/delta-demodulator-736051.html

Appendixes

Part 13: Dynamic of LDM and DCDM

In this part, you will be required to determine the maximum value of the input voltage (for a given frequency) below which slope overload can be avoided for the LDM.

To carry out this experiment, assemble the components as shown below.



9- Set the Clock frequency f_{Clock} = 100 kHz (max)

10- Set the function generator to: Sine, f_m = 100 Hz, V_{SS} = 1 V.

11- Set the bridging plug to LDM (at the input of $\int_2$)

12- Connect the CASSY Sensor UA1 to the modulating signal $S_m(t)$

13- Connect the CASSY Sensor UB1 to the prediction signal X(t) (at the output of $\int_2$)

14- Start the measurement by pressing F9.

15- Change Vss until the prediction signal *X(t)* shows the beginning of the slope overload. This value is denoted as A_{max} (Record it in Table 1).

16- Repeat the measurements for the frequency of $S_m(t)$ signal of 200, 300, 400, 500, 1000, 2000, 3000 Hz.

Frequency (Hz)	100	200	300	400	500	1000	2000	3000
A_{max} for LDM	1.48	1.13	0.77	0.58	0.44	0.26	0.1	

→ UA1

17- Calculate the dynamic D.

8.1 2.3 2.2 1.8 1.4 0.7 0.4

$$D = 20 \log \left(\frac{A_{max}}{A_{min}} \right) dB$$

Note: For A_{Mmin} use the value for granular noise (Assume constant = 20m Vpp).

18- Change the bridging plug to DCDM (at the input of f_2).

19- Reduce Vss to 1V.

20- Change Vss until the prediction signal $X(t)$ shows the beginning of the slope overload. This value is denoted as A_{max} (Record it in Table 2).

21- Repeat the measurements for the frequency of $S_m(t)$ signal of 200, 300, 400, 500, 1000, 2000, 3000 Hz.

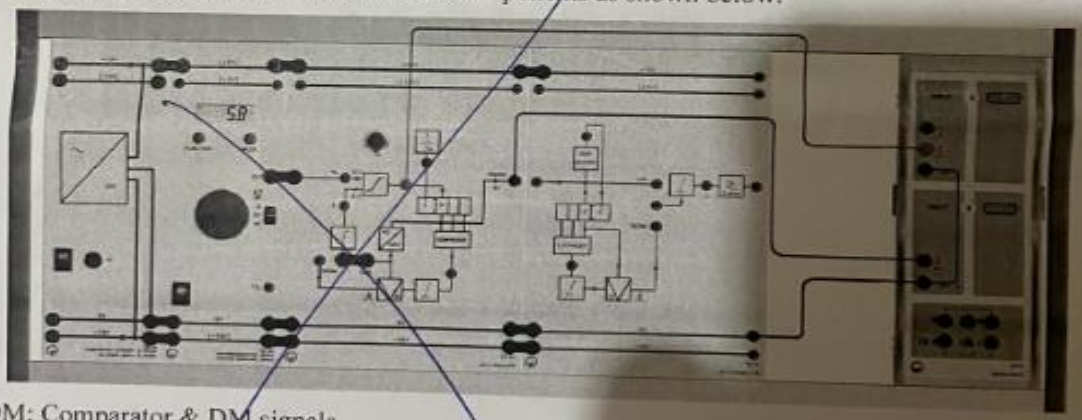
Frequency (Hz)	100	200	300	400	500	1000	2000	3000
A_{max} for DCDM	16.7	12.2	8.4	2,91	2,85	1.44	0,8	
				6.3	5.8	2.8	1.6	

22- Calculate the dynamic D.

- What conclusions can you make with regard to the performance and dynamic response of both types of delta modulation.
- Plot: D Vs. fm for LDM & DCDM

Part 14: Coding and Companding (LDM and DCDM)

To carry out this experiment, assemble the components as shown below.



LDM: Comparator & DM signals

1- Set the Clock frequency f_{Clock} = 10 kHz (min)
2- Set the function generator to: Sine, f_m = 100 Hz, V_{SS} = 1 V.
3- Set the bridging plug to LDM (at the input of f_2)
4- Connect the CASSY Sensor UA1 to the Comparator output.
5- Connect the CASSY Sensor UB1 to the DM output (bipolar/RZ)
6- Start the measurement by pressing F9.