

VLSI DESIGN

FINAL PROJECT

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PROJECT TITLE : TRAFFIC LIGHT CONTROLLER WITH PEDESTRAIN SIGNAL.

BOARD FAMILY : SPARTAN7

1,Design source

```
module traffic_light_controller(  
    input wire clk,  
    input wire reset,  
    input wire pedestrian_request,  
    output reg [2:0] traffic_light,  
    output reg pedestrian_light  
);  
  
    localparam GREEN = 2'b00;  
    localparam YELLOW = 2'b01;  
    localparam RED = 2'b10;  
  
    reg [1:0] state, next_state;  
    reg [3:0] timer;  
    reg pedestrian_waiting;  
  
    always @(posedge clk or posedge reset) begin  
        if (reset) begin  
state <= GREEN;  
            timer <= 0;  
            pedestrian_waiting <= 0;  
        end else begin
```

```

    if (pedestrian_request)
        pedestrian_waiting <= 1;

    if (state == RED && timer >= 10)
        pedestrian_waiting <= 0;
    if (state != next_state)
        timer <= 0;
    else
        timer <= timer + 1;
    state <= next_state;
end
end
always @(*) begin
    case (state)
        GREEN: next_state = (timer >= 10) ? YELLOW : GREEN;
        YELLOW: next_state = (timer >= 3) ? RED : YELLOW;
        RED: next_state = (timer >= 10) ? GREEN : RED;
        default: next_state = GREEN;
    endcase
end
always @(*) begin
    case (state)
        GREEN: begin
            traffic_light = 3'b001;
            pedestrian_light = 0;
        end
        YELLOW: begin

```

```

        traffic_light = 3'b010;
    end
    RED: begin
        traffic_light = 3'b100;
        pedestrian_light = (pedestrian_waiting) ? 1 : 0;
    end
    default: begin
        traffic_light = 3'b001;
        pedestrian_light = 0;
    end
endcase
end
endmodule

```

2,SIMULATION SOURCE

```

`timescale 1ns / 1ps
module tb_traffic_light_controller;

    reg clk;
    reg reset;
    reg pedestrian_request;
    wire [2:0] traffic_light;
    wire pedestrian_light;
    traffic_light_controller uut (
        .clk(clk),
        .reset(reset),
        .pedestrian_request(pedestrian_request),
        .traffic_light(traffic_light),
        .pedestrian_light(pedestrian_light)
    );

```

```

initial begin

    clk = 0;

    forever #5 clk = ~clk;

end

initial begin

    reset = 1;

    pedestrian_request = 0;

    #20 reset = 0;

    #100;

    pedestrian_request = 1;

    #10 pedestrian_request = 0;

    #200;

    pedestrian_request = 1;

    #10 pedestrian_request = 0;

    #300;

    $stop;

end

initial begin

    $monitor("Time=%0t | Traffic Light={R,Y,G}=%b | Pedestrian=%b",

        $time, traffic_light, pedestrian_light);

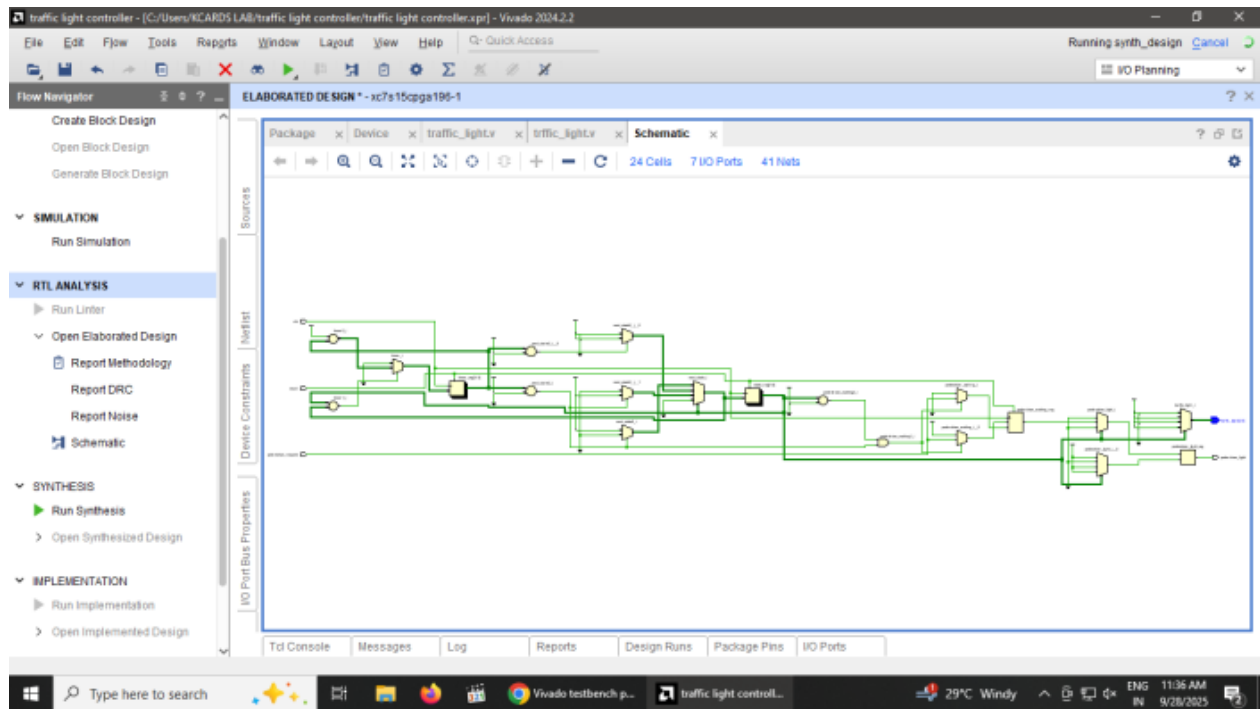
End

+

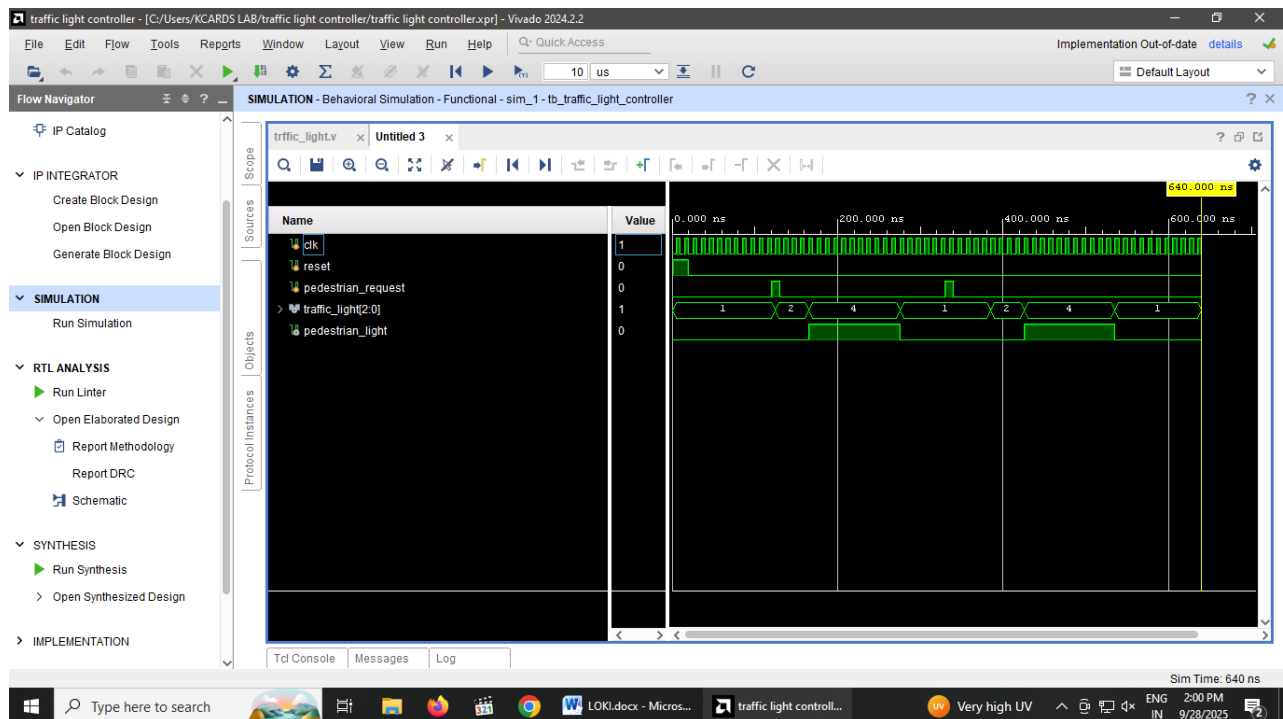
endmodule

```

3,RTL ANALYSYS

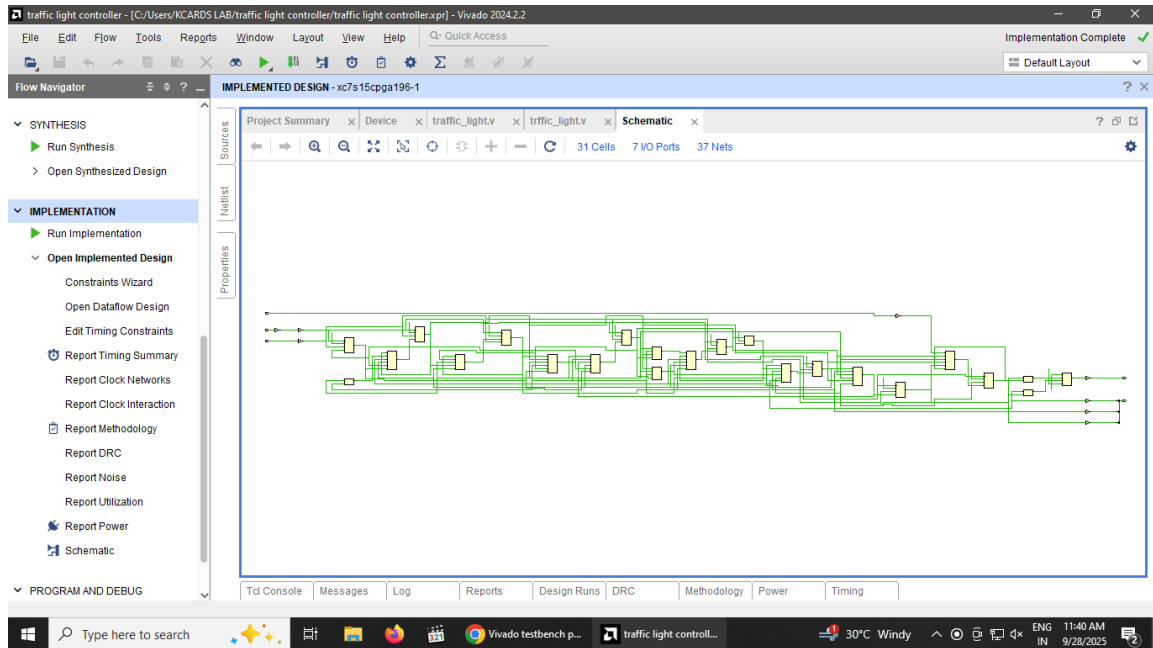


4,simulation

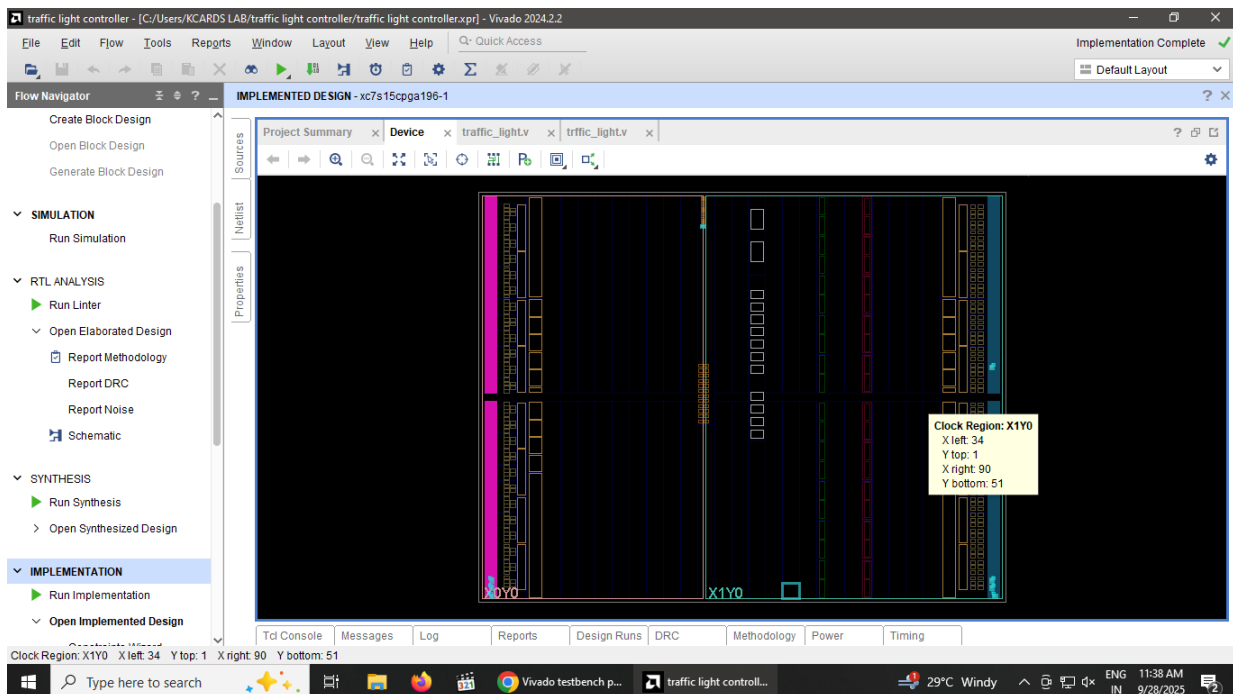


5, synthesis

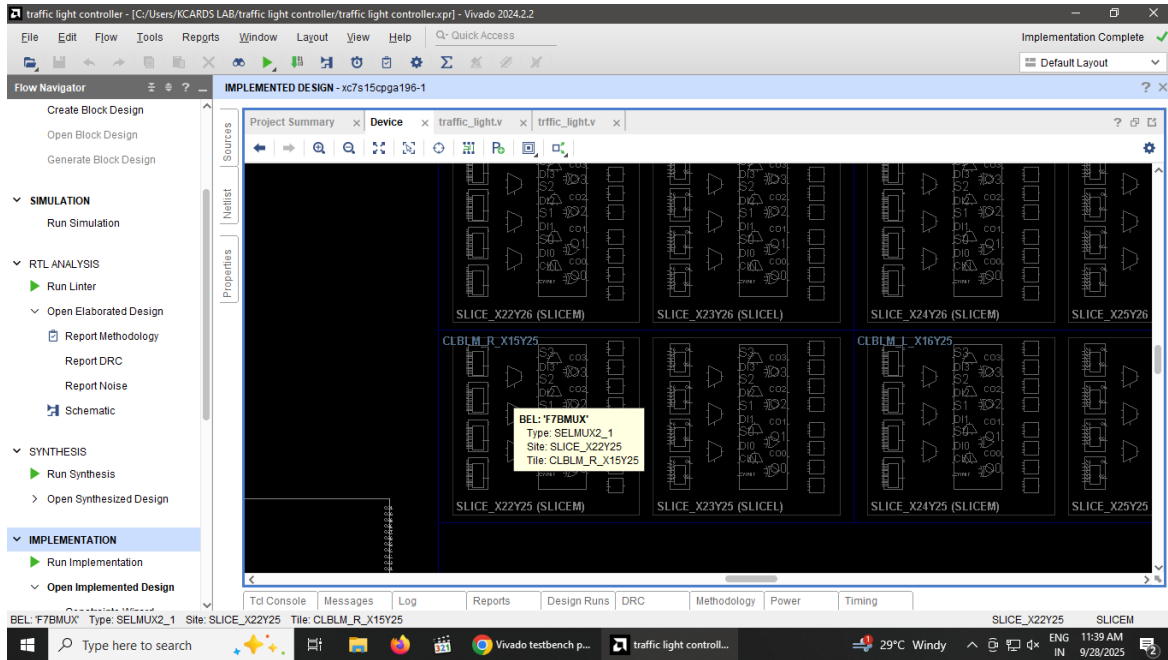
5.1 chamatic:



5.2 Device

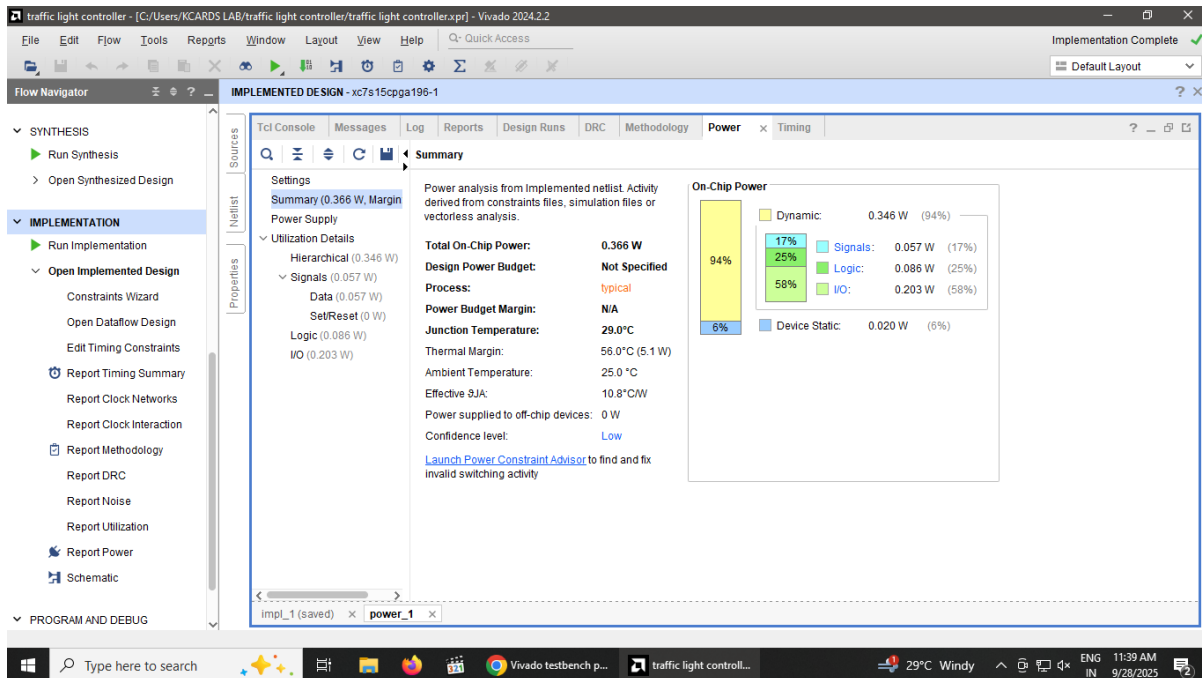


5.3 Graph



6.Synthesis report

6.1 Power:



6.2 Utilization

The screenshot displays the Vivado 2024.2.2 interface with the 'IMPLEMENTED DESIGN - xc7s15cpgg196-1' project. The 'Utilization' tab is selected, showing a table of resource usage for the 'traffic_light_controller' device.

Name	Slice LUTs (8000)	Slice Registers (16000)	Slice (2000)	LUT as Logic (8000)	Bonded IOB (100)	BUFCTRL (16)
traffic_light_controller	11	9	4	11	7	1

The left sidebar shows the 'IMPLEMENTATION' section with various reports and tools. The bottom status bar indicates the system is at 30°C and the date is 9/28/2025.

7,Implementation

The screenshot displays the Vivado 2024.2.2 interface with the 'ELABORATED DESIGN - xc7s15cpgg196-1' project. The 'Schematic' view is selected, showing a single component 'traffic_light[2:0]' connected to a bus '3 I/O Ports 3 Nets'.

The left sidebar shows the 'RTL ANALYSIS' section with various reports and tools. The bottom status bar indicates the system is at 1:58 PM on 9/28/2025.