EE380 (EC) LAB REPORT

Experiment-7

Compensation in Multi-Stage Amplifiers

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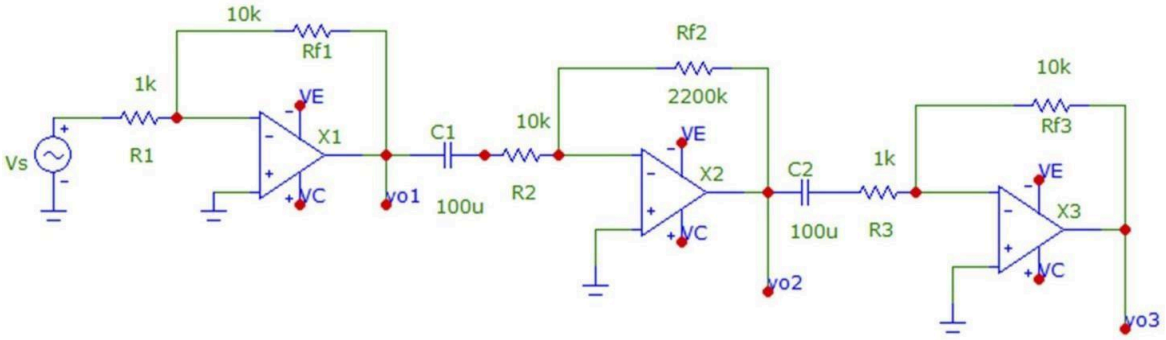
Section: B

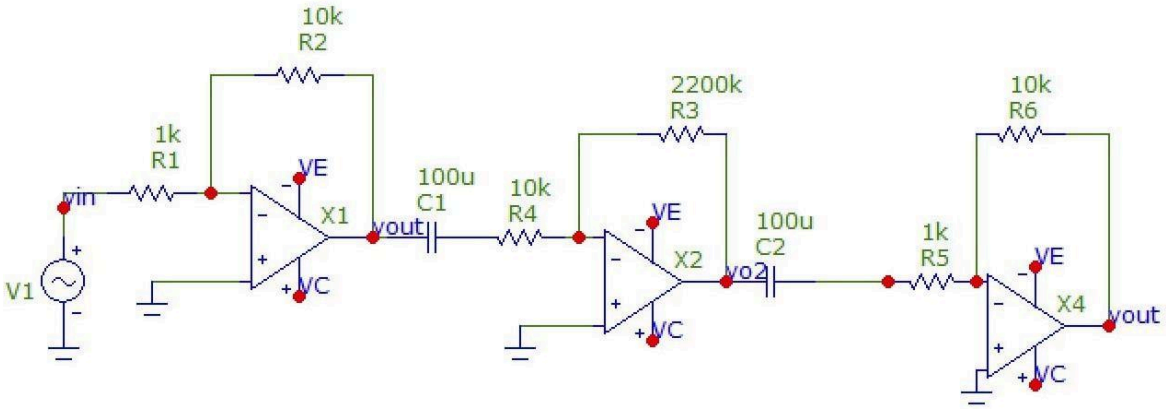
Investigate stability of a multi-stage amplifier shown below and design compensation for different phase margins



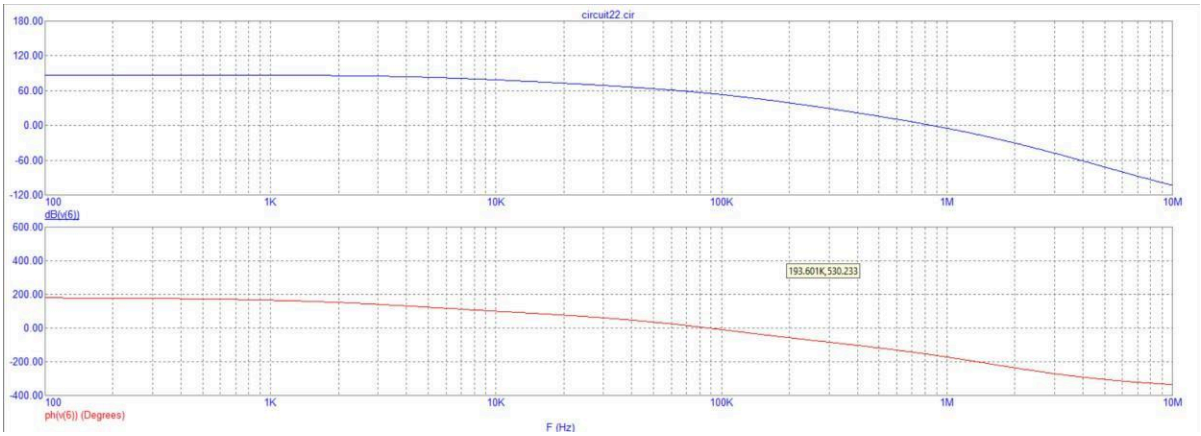
1. Study gain and phase margin for the final output

PRE-LAB

- Design Procedure: Examine the multistage amplifier circuit's gain and phase margin.
- Circuit Diagram



- Circuit Simulation:



- Analysis

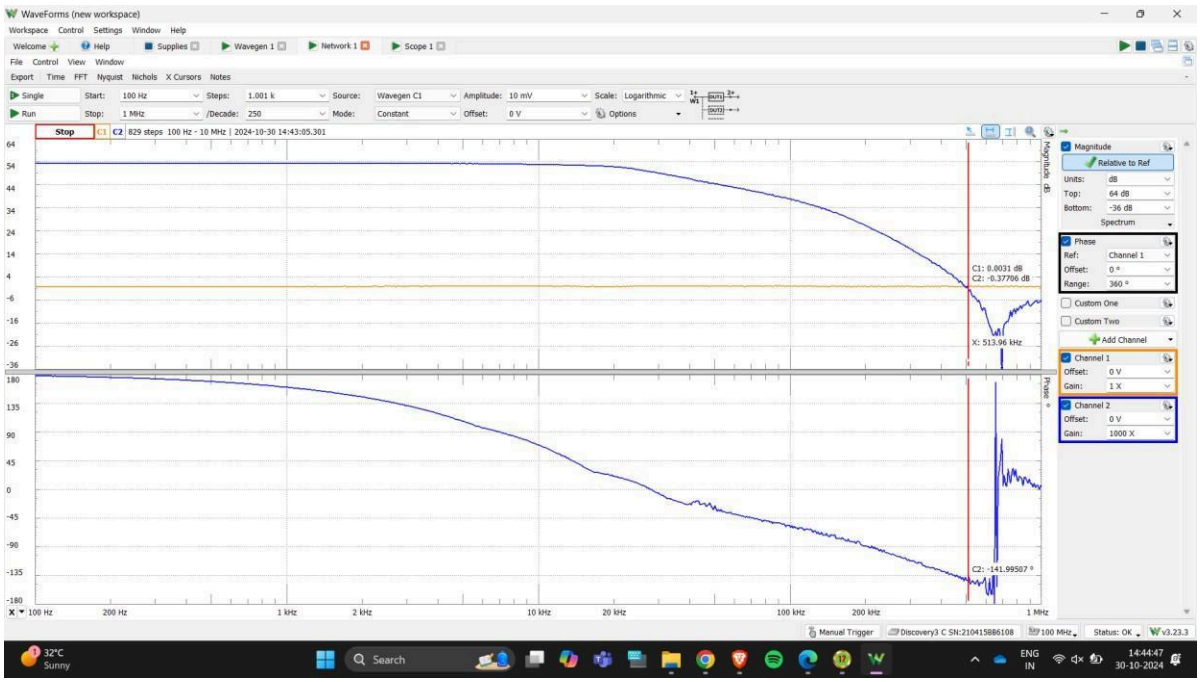
  Gain crossover frequency: 819.689 kHz

  Phase at this Frequency: -153.88 degrees

  Phase Margin: 26.12 degrees

  Gain Margin: -9.04 dB

IN-LAB



POST-LAB

Gain crossover frequency = 512.86 kHz

Phase at gain crossover frequency = -142.1507 degrees

Phase Margin: 180 – 142.1507 = 37.8493 degree

Gain Margin = -26dB

- Analysis

  Gain Margin: Gain at phase crossover frequency

  Phase Margin: 180 degrees + phase at gain crossover frequency

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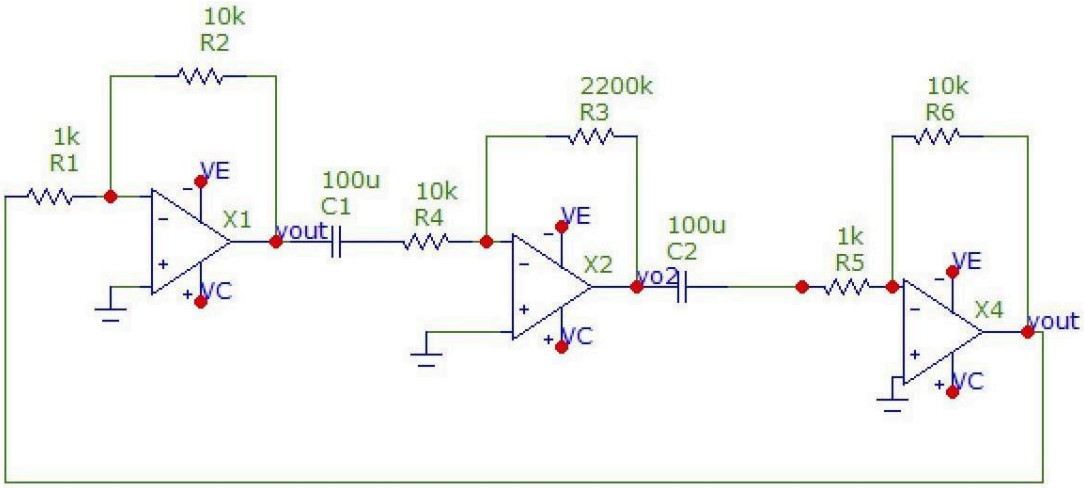
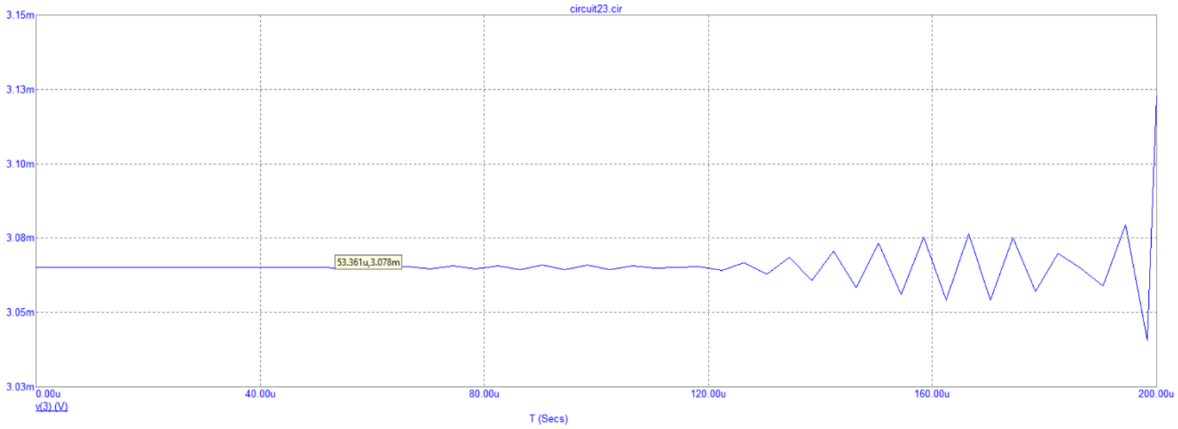
2. Make a unity gain buffer and study the oscillation for zero input voltage

PRE-LAB

- Design Procedure: Monitor the output and provide feedback on the first op-amp's output. Vin has been grounded.
- Circuit Diagram





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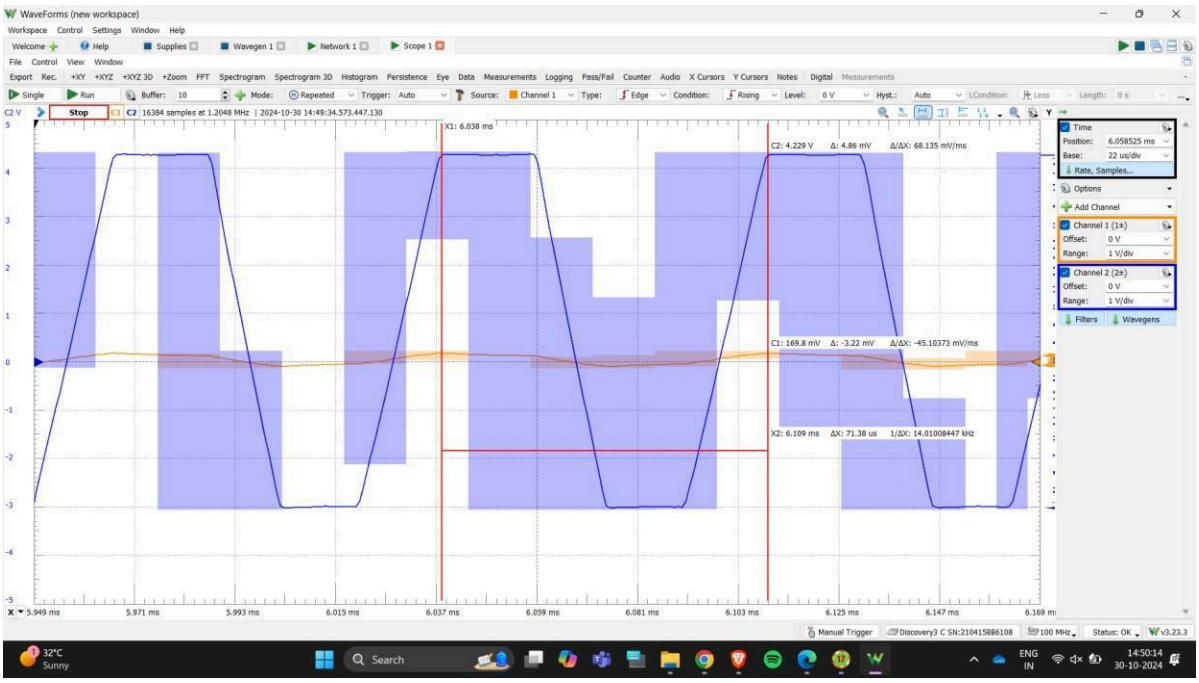
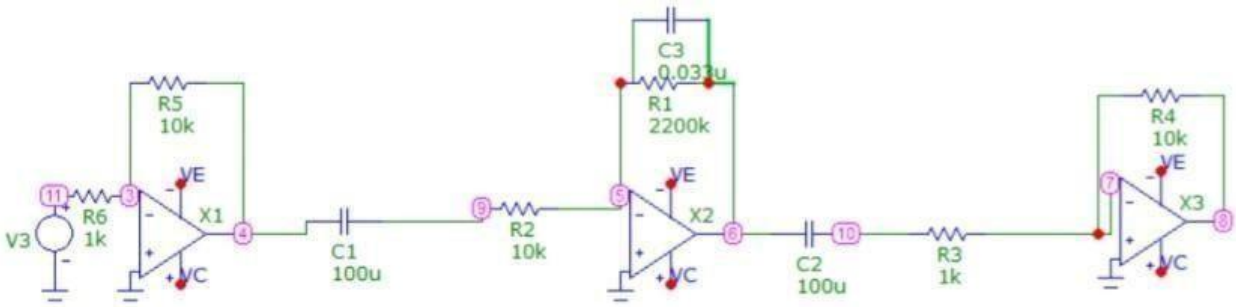


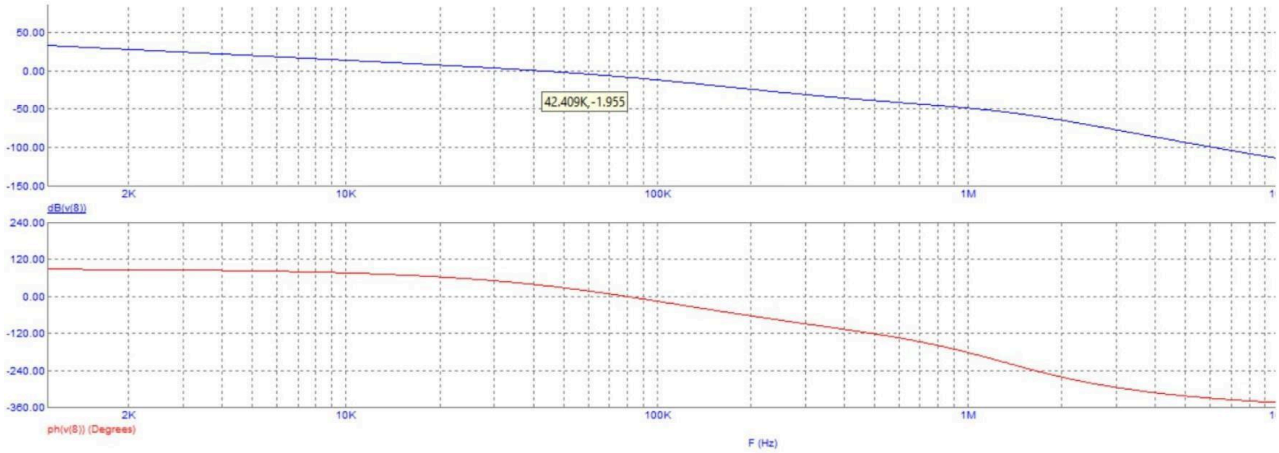
3. Add suitable compensation capacitor to the circuit and study new Gain/Phase margins

PRE-LAB

- Design Procedure: Here, we adjust the frequency response by adding a compensation capacitor to guarantee stability. A phase margin of roughly 25 degrees is what we want.
- Circuit Diagram



- Circuit simulation



- Analysis

$$H(f) = H_O(f) \times \left(\frac{1}{1 + j\frac{f}{f_P}} \right) \qquad f_P = \frac{1}{2\pi R_{f2} C_C}$$

Gain crossover frequency = 43.409 kHz

Phase at gain crossover frequency: 24.121 degrees

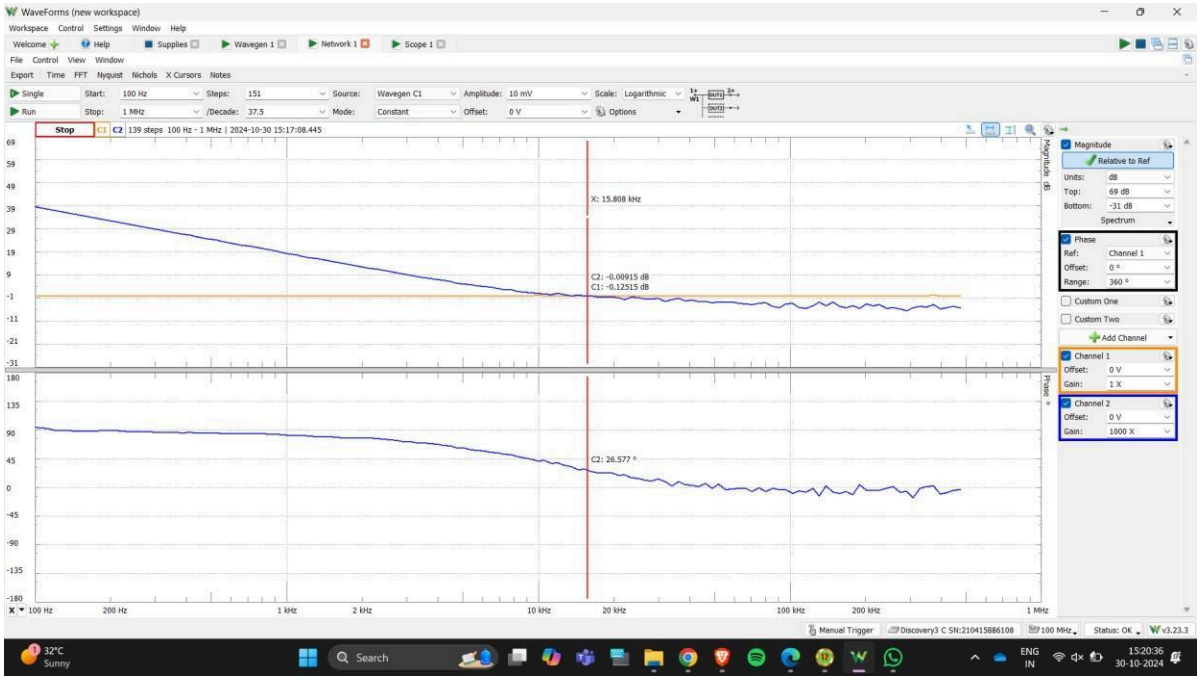
Phase Margin: 24.121 degrees

Gain Margin: -46 dB

Cc = 0.033uF

IN-LAB

- Waveform Output:



POST-LAB

Gain crossover frequency = 16.108 kHz
Phase at this Frequency: 27.077 degrees
Phase Margin: 27.077 degrees
Gain Margin: -23 dB
Cc = 0.033uF

Effect on Gain: The compensating capacitor mostly influences the high-frequency response of the amplifier and may result in a slight reduction in gain at higher frequencies due to the roll-off it introduces. This roll-off limits the bandwidth in return for increased stability. The Bode plot can be examined to observe how the gain curve changes and whether it agrees with theoretical predictions when the capacitor is introduced.

Phase Margin Improvement: The primary function of the compensation capacitor is to increase the phase margin, which reduces the likelihood of oscillations. By examining the phase response, we can assess how successfully the capacitor decreased the phase lag between steps. With the right adjustment, the phase margin should ideally increase, creating a more stable amplifier that doesn't oscillate.

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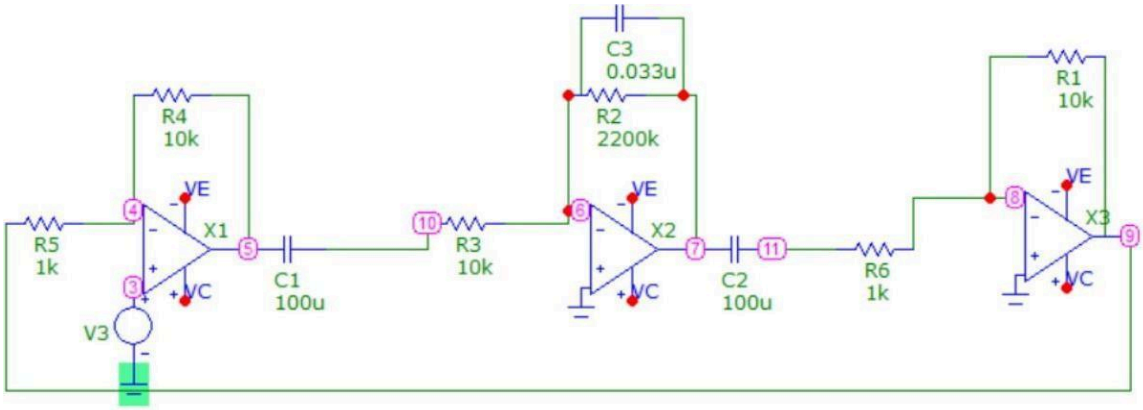
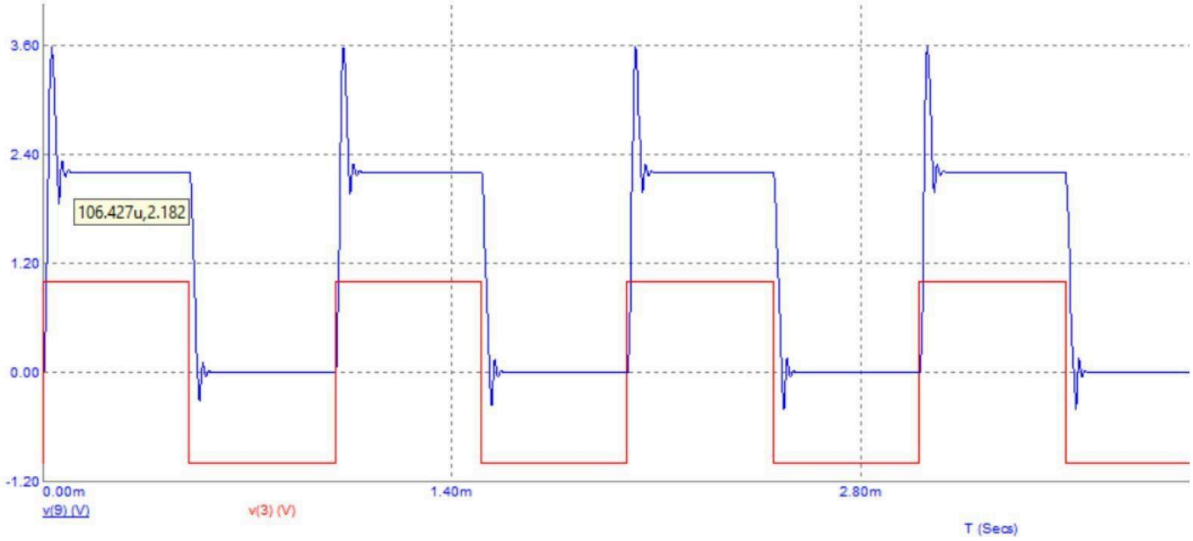
4. Correlate phase margin with overshoot and settling time of unity gain buffer obtained by connecting output vo6 to input and driving it with 1V square wave

PRE-LAB

- Design Procedure: Determine the settling time (the amount of time when the output is 2% or 5% of the stable output) and the phase margin using network analysis.
- Circuit Diagram



- Circuit simulation



- Analysis

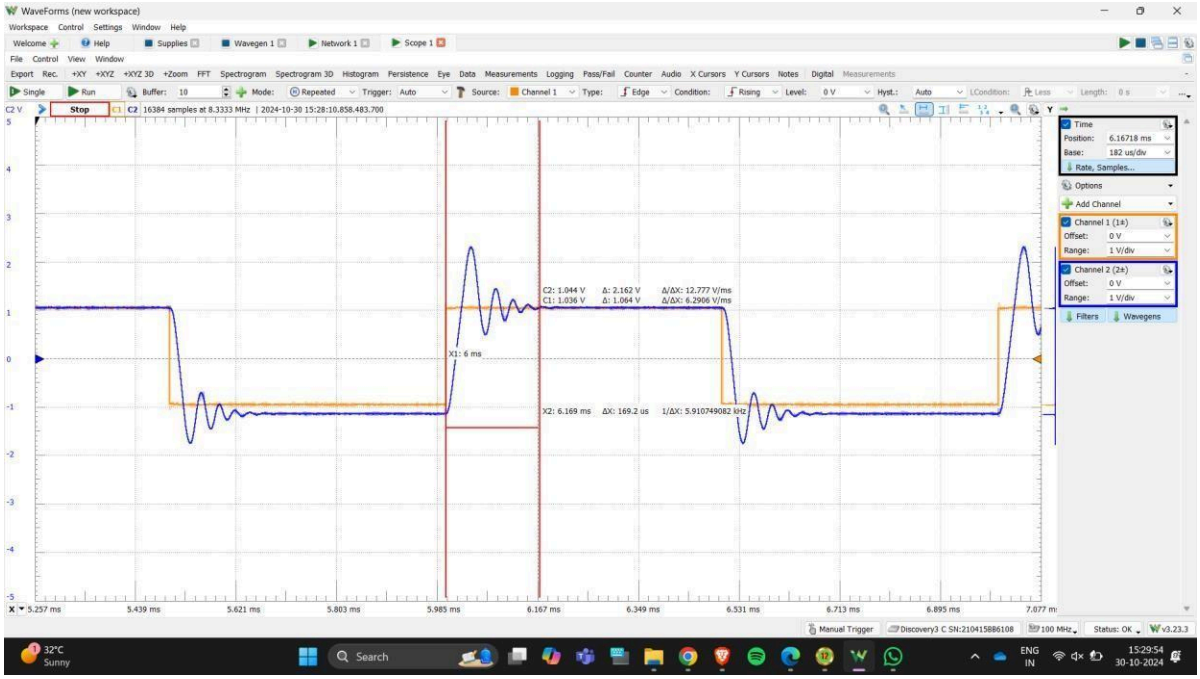
  Vo(max) = 3.6V

  Overshoot = 2.6/3.6 *100 = 72%

  Settling Time = 0.105ms

IN-LAB

- Waveform Outputs:



POST-LAB

Overshoot = (Vo(max) – 1)/Vo(max) *100 Vo(max) = 3V

Overshoot = 55.64%

Settling Time = 169.2 us

- Analysis

Phase Margin and Transient Response: We were able to ascertain the connection between phase margin and these characteristics of transient response by looking at the output waveform.

Analysis of Overshoot: Overshoot is the term used to describe when a step input results in an output that initially exceeds the desired value. A smaller phase margin usually leads to increased overshoot since the circuit is more prone to instability and oscillations.

The "settling time" is the period of time it takes for the output to become close to and stay within a given percentage, typically between 2 and 5% of the final value.
