Module-V
INVERTERS

Overview of Inverters:

In the context of power electronics, the term "inverter" refers to a family of circuits that operate from a source of dc voltage or dc current and transform it into an ac voltage or current. The inverter performs the opposite function of an ac-to-dc converter (see ac-to-dc converters). Despite being a dc source, the input to an inverter circuit is sometimes generated from an ac source, such a utility ac supply. For instance, a utility ac voltage supply may serve as the main source of input power. It is then "inverted" back to ac using an inverter after being converted to dc by an ac to dc converter. In this case, the utility supply's input ac and the final ac output can have different frequencies and magnitudes.

The figure below depicts a single phase half bridge DC-AC inverter.

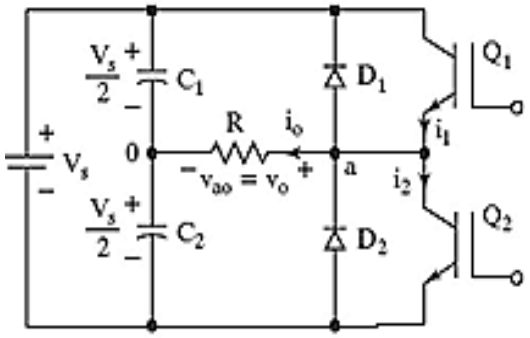


Figure 5.1: DC-AC converter with a single phase half bridge and R load

The following presumptions and conventions are taken into consideration while analysing DC-AC inverters.

It is believed that the current entering node an is positive.

Because they only carry current in one direction, the switches S1 and S2 are unidirectional.

The symbols i1 and i2 stand for the current flowing through S1 and S2, respectively.

The figure below illustrates the switching sequence. In this case, switch S1 is turned on for $0 \leq t \leq T1$, while switch S2 is turned on for $T1 \leq t \leq T2$. The instantaneous voltage across the load is $v_o = Vin/2$ when switch S1 is activated.

The voltage across the load is $v_o = –Vin/2$ when switch S2 is solely activated.

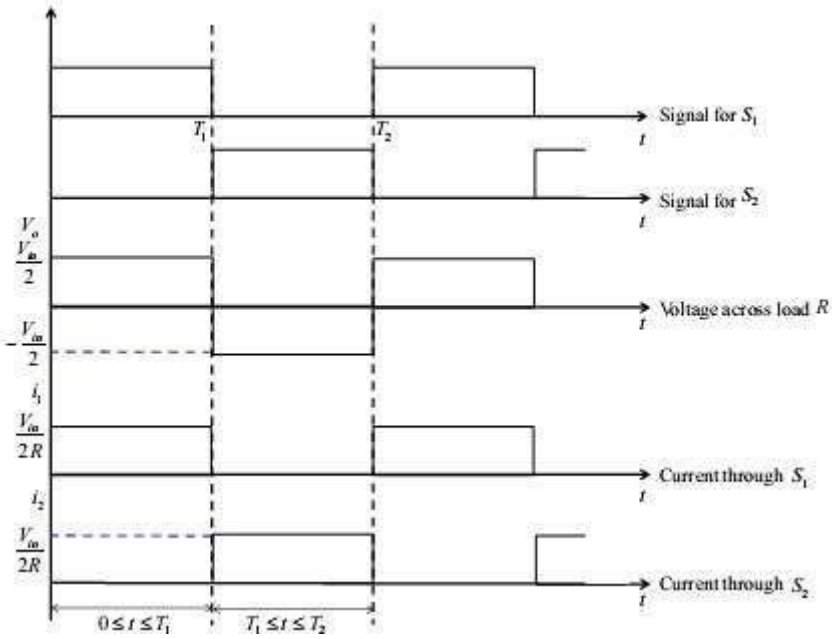


Figure 5.2 shows the output waveforms of a single phase half bridge DC-AC inverter.

The output voltage ν o's root mean square value is determined by

$$V_{o,rms} = \left(\frac{1}{T_1} \int_0^{T_1} \frac{V_{in}^2}{4} dt \right) = \frac{V_{in}}{2}$$

Rectangular in form is the instantaneous output voltage ν o. Fourier series may be used to represent the instantaneous value of ν o as follows:

$$v_o = \frac{a_o}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t)$$

The values of a0 and an are zero because of the quarter wave symmetry along the time axis. The value of bn may be found using

By changing the value of bn in the equation above, we get

$$b_n = \frac{1}{\pi} \left[\int_{\frac{-\pi}{2}}^{0} \frac{-V_{in}}{2} d(\omega t) + \int_0^{\frac{\pi}{2}} \frac{V_{in}}{2} d(\omega t) \right] = \frac{2V_{in}}{n\pi}$$

$$v_o = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_{in}}{n\pi} \sin(n\omega t)$$

The resistor's current (iL) is determined by

$$i_L = \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{R} \frac{2V_{in}}{n\pi} \sin(n\omega t)$$

DC-AC half bridge inverter with R-L and L loads

The figure below depicts a DC-AC converter with an inductive load. With an inductive load, the output voltage cannot instantly alter the load current.

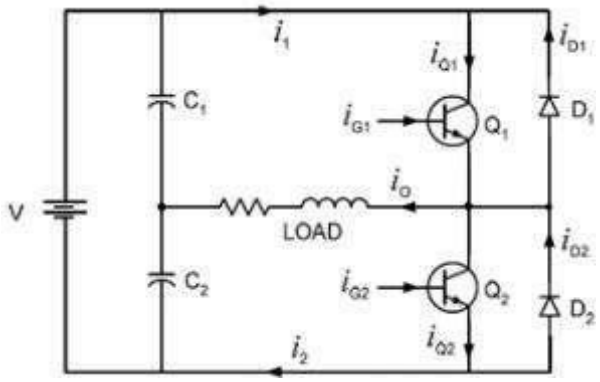


Figure 5.3: DC-AC inverter with a single phase half bridge and RL load

The operation of the DC-AC inverter with an inductive load is as follows: Case 1: The switch S1 is on throughout the time period 0<=t<= T1, and current passes through the inductor from points a to b. As shown in the figure below, the load current would keep flowing through the capacitor C2 and diode D2 after the switch S1 is switched off (case 1) at t-T1 until the current drops to zero.

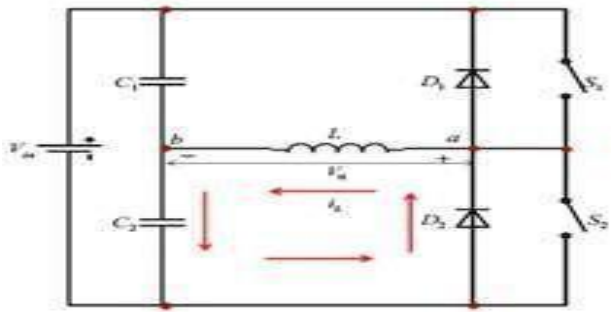


Figure 5.4: DC-AC converter with a single phase half bridge and a load of L

Case 2: As seen in the figure below, the load current passes via the diode D1 and capacitor C1 until it drops to zero when S2 is shut off at t = T1.

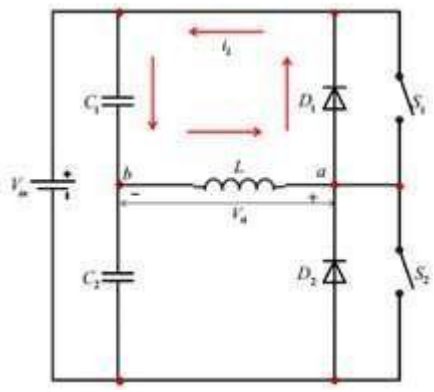


Figure 5.5: DC-AC converter with a single phase half bridge and a load of L

The diodes D1 and D2 are referred to as feedback diodes because they provide energy back to the dc source when they conduct. Another name for these diodes is freewheeling diodes. For a purely inductive load, the current is determined by

$$i_L = \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{\omega n L} \frac{2V_{in}}{n\pi} \sin\left(n\omega t - \frac{\pi}{2}\right)$$

$$i_L = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_{in}}{n\pi\sqrt{R^2 + (n\omega L)^2}} \sin\left(n\omega t - \theta_n\right)$$

The same is true for the R-L burden. One may determine the instantaneous load current as follows:

Where,

$$\theta_n = \tan^{-1}\left(\frac{n\omega L}{R}\right)$$

Single phase full bridge inverter operation

The figure below depicts a DC-AC converter with a single phase bridge. The single phase DC-AC inverters are analysed using the following presumptions and guidelines.

Figure 8's current entering node is seen as positive.

The S1, S2, S3, and S4 switches only carry electricity in one direction, making them unidirectional.

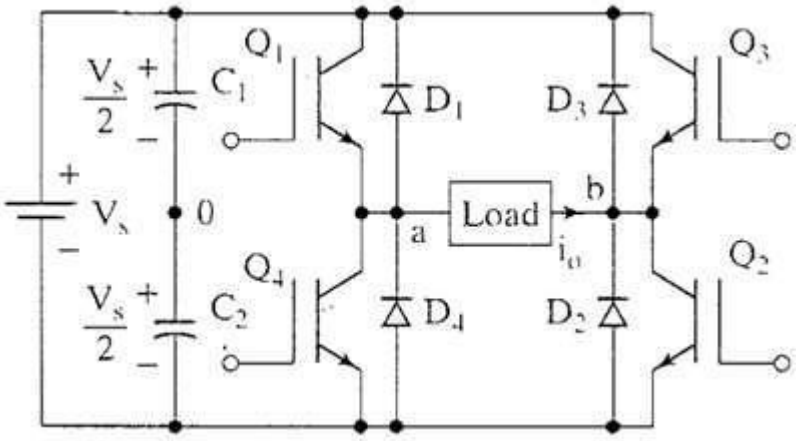


Figure 5.6: DC-AC inverter with R load, single phase, full bridge

The input voltage Vin appears across the load and the current flows from point a to point b when switches S1 and S2 are switched on simultaneously for a time of $0 \leq t \leq T1$.

$\nu o = Vs$ = Q1 – Q2 ON, Q3 – Q4 OFF

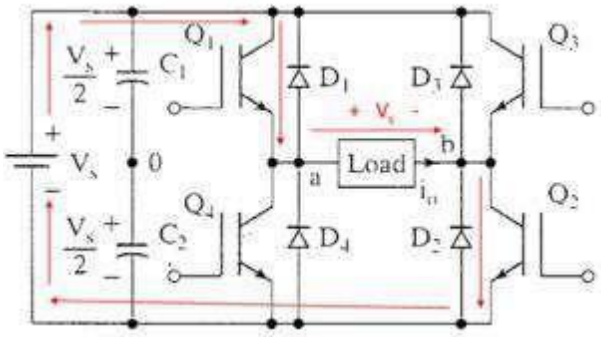


Figure 5.7: DC-AC inverter with R load, single phase, full bridge

The voltage across the load is inverted and the current flows from point b to point an if switches S3 and S4 are switched on for time $T1 \leq t < T2$.

$\nu o = -Vs$ = Q1 – Q2 OFF, Q3 – Q4 ON

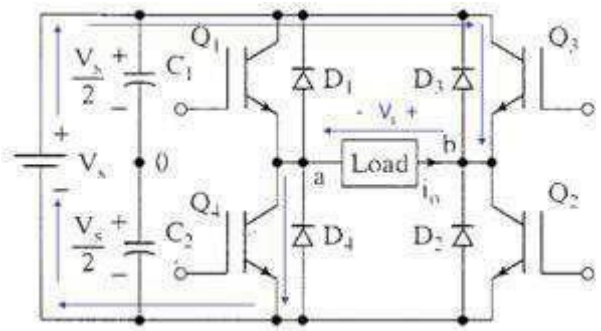


Figure 5.8: Full bridge DC-AC inverter in single phase with R load current directions

The figure below displays the waveforms of voltage and current over the resistive load.

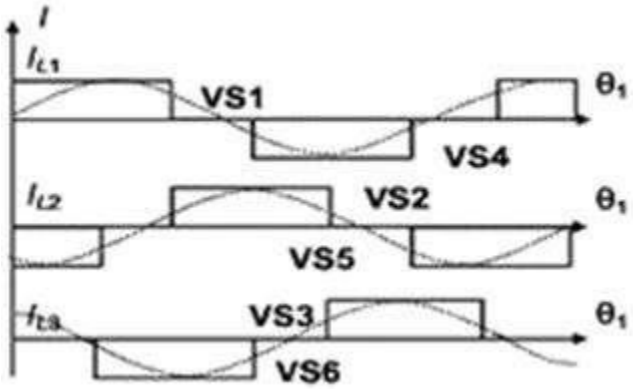


Figure 5.9 Waveforms of a single phase full bridge DC-AC inverter

R-L load single phase full bridge inverter:

For a single-phase load, a single-phase square wave type voltage source inverter generates an output voltage that is square in form. The power switches in these inverters must function at far lower frequencies than those in certain other kinds of inverters, and their control logic is quite basic. Since thyristor switches could only be turned on and off a few hundred times per second, the first generation of inverters that used them were almost always square wave inverters. On the other hand, modern switches, such as IGBTs, operate at switching rates of several kilohertz and are far quicker. Half bridge or full bridge topologies are often used in single-phase inverters. These topologies' power circuits are shown in the figure below.

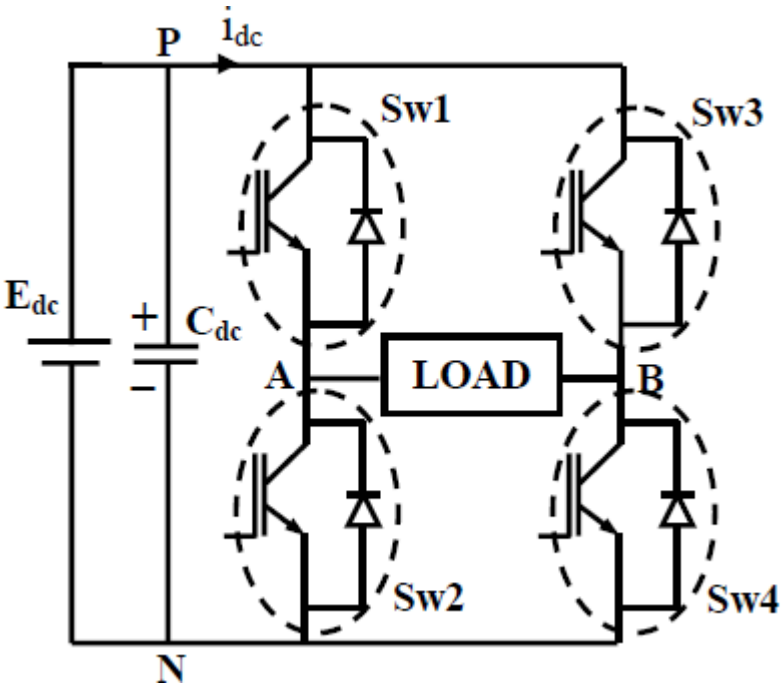


Figure 5.10: DC-AC converter with a single phase full bridge and L load

Assuming perfect circuit conditions, the aforementioned architecture is examined. Consequently, it is assumed that the switches are lossless and that the input dc voltage (Edc) is constant. Two such legs are present in a complete bridge topology. Two series-connected electrical switches, seen in the pictures as dotted lines, make up each leg of the inverter. An uncontrolled diode is placed anti-parallel across an IGBT-type controlled switch in each of these switches. These switches only need to block one polarity of power, yet they may conduct current in both directions. One output point for the load is provided by the junction of the switches in each leg of the inverter.

Series inverter:

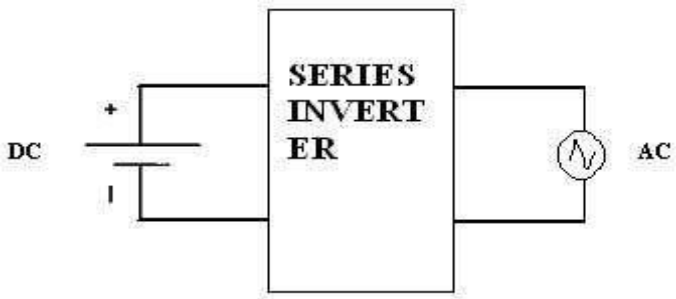


Figure 5.11: Series inverter block diagram

The load is linked in series with the commutating components L and C in a series inverter. A series RLC resonant circuit is what this is. The output's positive and negative half cycles are produced by the two SCR.

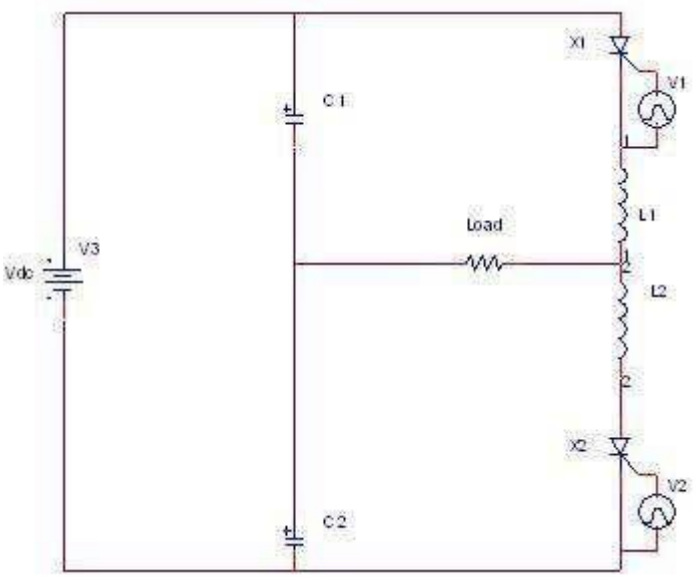


Figure 5.12: Series inverter circuit schematic

When SCR T1 is activated, current may pass via L1, the load, and C2 in the first half of the output currents, resulting in charging. Through SCR1, L1, and the load, the capacitor C1, which is already charged at this moment, discharges. As a result, the input source draws 50% of the current while the capacitor draws 50%. Likewise, via the load, L2, and SCR2, C1 will be charged and C2 will discharge in the second half of the output current. Once again, 50% of the load current comes from the DC input source, with the remaining 50% coming from the capacitor. To get AC voltage and current, the SCRs T1 and T2 are alternately activated.

How a parallel inverter works

A commutating capacitor C, an output transformer, an inductor L, and two SCRs T1 and T2 make up the single phase parallel inverter circuit. Vo and Io are the output voltage and current, respectively. L's role is to maintain a steady source current. As this is being operated,

Through the transformer, the inverter and capacitor C are connected in parallel with the load. Thus, it is known as a parallel inverter.

The following modes provide an explanation of how this inverter operates. Mode I

SCR T1 is conducting in this mode, and current flows through the top part of the main winding. SCR T2 is not in use. Consequently, an emf Vs is generated across the primary winding's upper and lower halves.

Stated otherwise, the capacitor C charges to a voltage of 2 Vs with the top plate as positive. The total voltage across the main winding is 2 Vs.

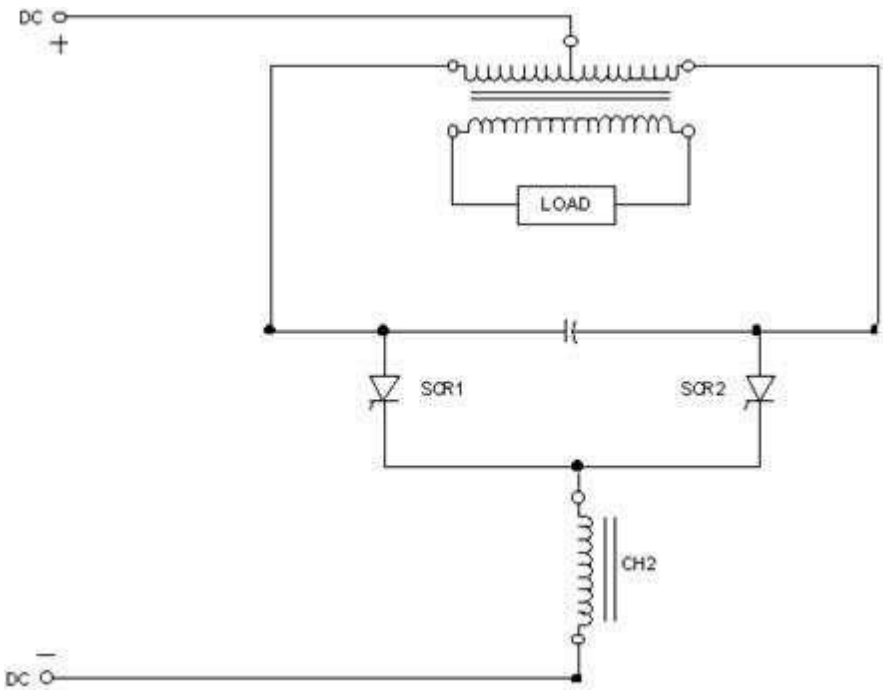


Figure 5.13: Parallel inverter circuit schematic

Mode II

A trigger pulse is applied to T2's gate at time to turn it on. Capacitor voltage 2Vs is switched off at this point in time (t=0) since it appears as a reverse bias across T1. Through T2 and the bottom part of the main winding, a current Io starts to flow. At time t=t1, the capacitor is now charged from +2V to -2V (top plate as negative). Additionally, the load voltage shifts from Vs at t=0 to -Vs at t=t1.

Mode III

T1 may be switched ON at any moment when the capacitor is charged to –Vs. When T1 is triggered, the capacitor voltage of 2Vs creates a reverse bias across T2, turning T2 OFF. The capacitor begins to discharge and charge in the reverse way, with the top plate being positive, after T2 is turned off.

Parallel Commutated Inverter:

A schematic of the traditional parallel commutated square wave inverter bridge may be seen in Figure 1. Since most other circuits use this circuit or a version of it, it is included here for explanatory purposes. The waveform that is produced and sent to the load is essentially a square wave with a period that is dictated by the rate at which SCRs 1 through 4 are gated on, and a peak-to-peak amplitude that is double the DC supply voltage. By concurrently applying signals to the gate terminals of SCRs 1 and 4 or SCRs 2 and 3, the SCRs are activated in pairs. A current will flow from the source's positive terminal via its negative terminal if SCRs 1 and 4 are the first two to be turned on. This will create a voltage connection on the load from left to right, plus to negative.

At the same time, capacitor C1's left terminal will be positively charged in relation to its right negative terminal. The impedance of the load almost entirely determines the steady-state load current flowing through the different components. Almost all of the source voltage appears across the load because Chokes 1 and 2 and SCRs 1 and 4 exhibit very low steady-state dips. SCRs 1 and 4 will continue to conduct until the conclusion of the half cycle, at which time the gates are removed, leaving SCRs 1 and 4 in conduction together with the now-activated SCRs 2 and 3. In the absence of chokes 1 and 2, activating the second set of SCRs would result in very low impedance, temporarily preventing the source from short-circuiting.

Capacitor C1 now discharges with a current that travels ahead via SCR 2 and into the cathode of SCR 1 before returning to the capacitor's negative terminal. As long as the reverse current flowing through the SCR is long enough for the SCR to once again become blocking, this direction of current flow renders SCR 1 non-conductive. C1 discharges concurrently via SCR 4 in the opposite direction and through SCR 3 in the forward direction. Similar to SCR 1, this will make SCR 4 non-conductive. This whole process is known as commutation, and it usually takes less than 50 microseconds in a contemporary inverter. Chokes 1 and 2 must have enough transient impedance at this time to stop the DC source's current from rising noticeably.

Two purposes are served by diodes 1, 2, 3, and 4. Returning any stored energy that could be "kicked back" from the load to its source is the first step. Additionally, they prevent the choke from producing a strong transient voltage just after commutation.

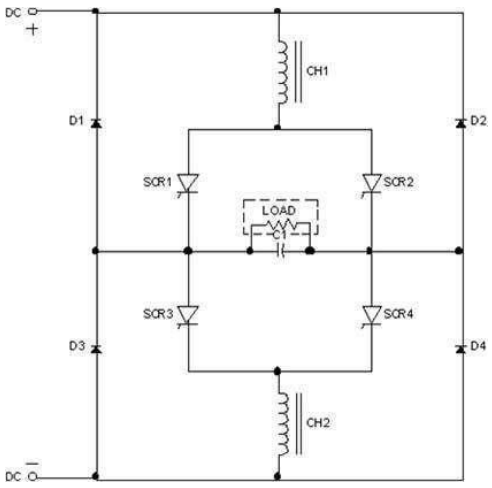


Figure 5.14: Parallel commutated inverter circuit schematic

Three-phase converters from DC to AC

High power applications often employ three phase inverters. A three-phase inverter provides the following benefits:

The output voltage waveform's frequency might vary widely since it is dependent on the switches' switching rate.

By altering the inverter's output phase sequence, the motor's rotational direction may be reversed.

By altering the dc link voltage, the ac output voltage may be managed.

Figure 2 depicts the typical setup of a three-phase DC-AC inverter. The switches may receive two different kinds of control signals:

180-degree conduction

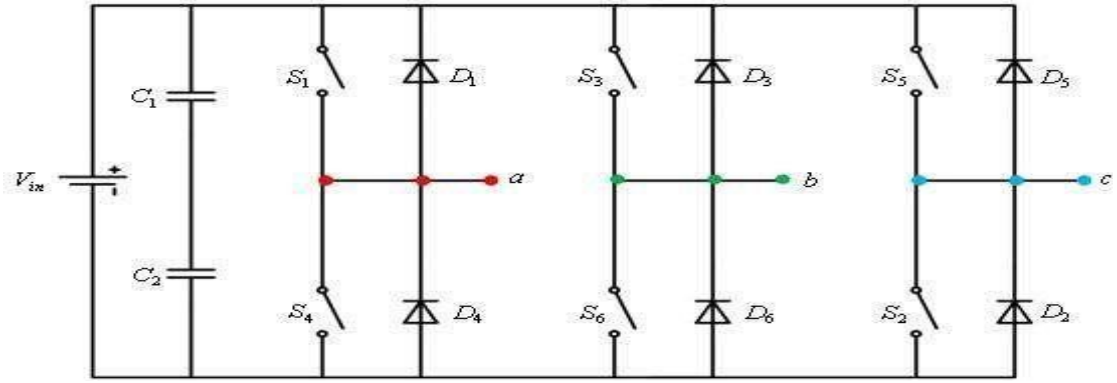


Figure 5.15: Three-phase bridge inverter circuit schematic

Conduction at 180 Degrees with Star-Connected Resistive Load

Figure depicts the three-phase inverter's layout with a resistive load linked to a star. The following protocol is adhered to:

• It is considered that a current is positive when it leaves a node point (a, b, or c) and enters the neutral point (n).

Every one of the three resistances is equal.

When operating in this mode, every switch conducts 180 degrees. Because of this, three switches are always on. The terminal an is linked to the input DC source's positive terminal when S1 is turned on. Likewise, terminal a connects to the input DC source's negative terminal when S4 is turned on. Each of the cycle's six operating modes has a 60° duration, and the following is a description of each mode:

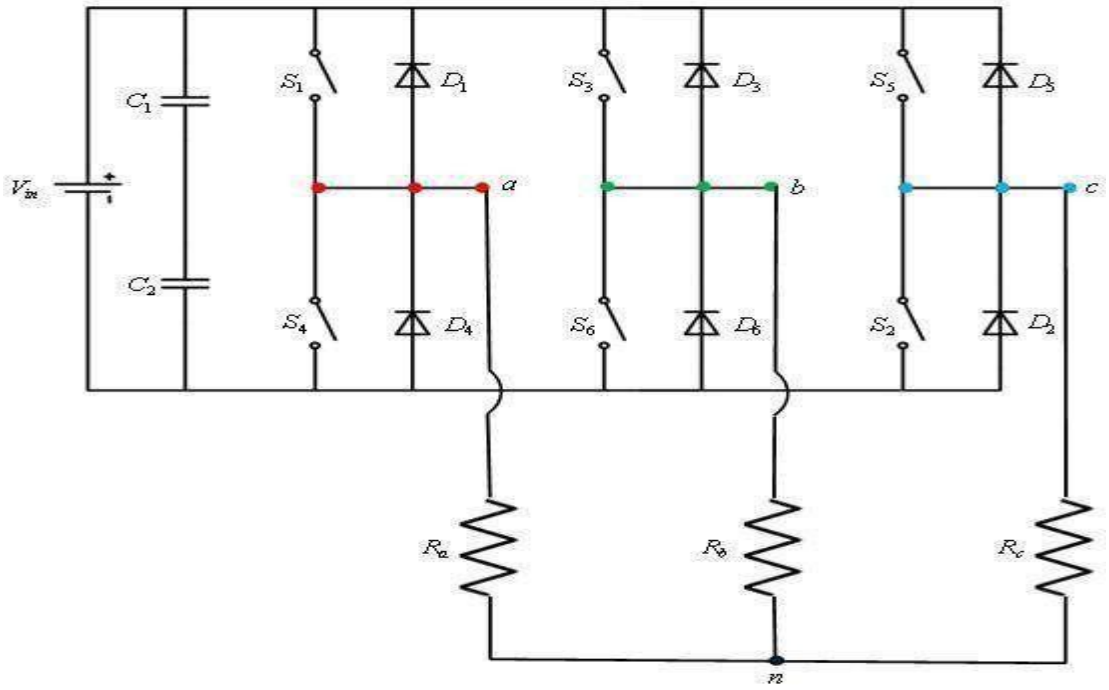


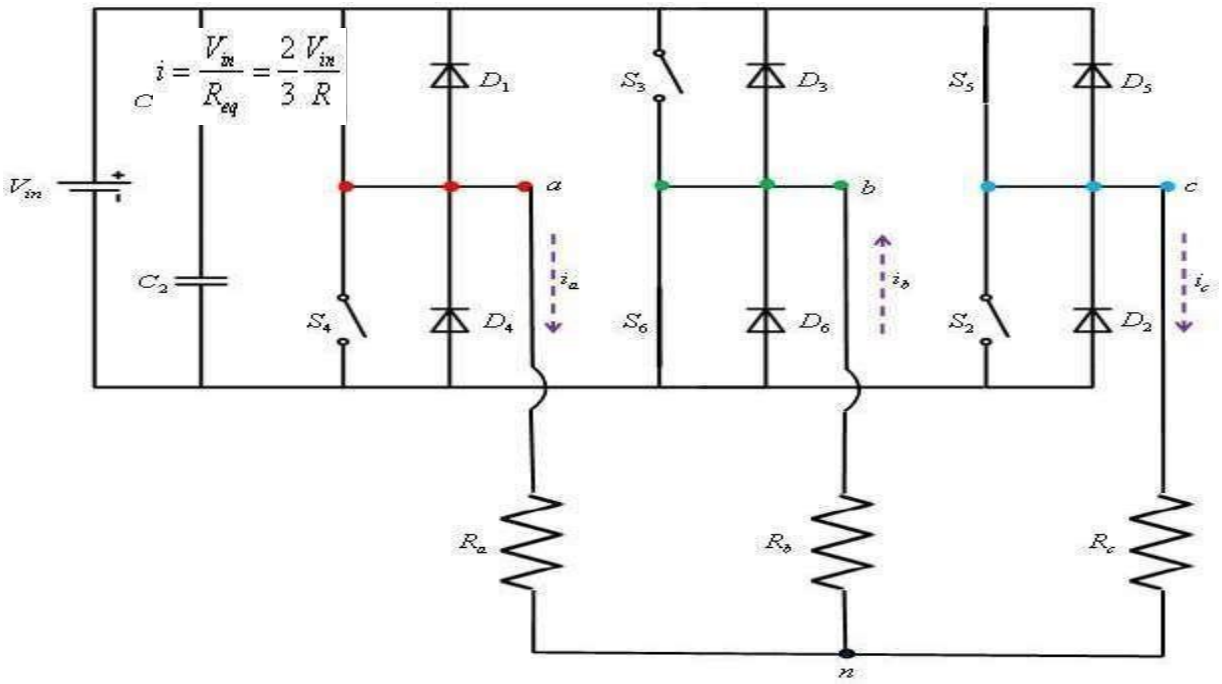
Figure 5.16: Three-phase bridge inverter circuit schematic with a load linked to a star

Mode 1: In this mode, the switches S5, S6, and S1 are activated for a predetermined amount of time. Consequently, the terminals a and c are linked to the input DC source's positive terminal and the

The negative terminal of the DC source is linked to terminal b. Figure depicts the flow of current via Ra, Rb, and Rc as well as the corresponding circuit. The circuit shown in Figure has an equal resistance of

(1) $$R_{eq} = R + \frac{R}{2} = \frac{3R}{2}$$

The DC input source's supplied current is



(2)

The ia and ib currents are

(3) $$i_a = i_c = \frac{1}{3}\frac{V_{in}}{R}$$

In consideration of the present convention, the current ib is

(4) $$i_b = -i = -\frac{2}{3}\frac{V_{in}}{R}$$

Once the currents flowing through each branch have been established, the voltage across each branch is

(5) $$v_{an} = v_{cn} = i_a R = \frac{V_{in}}{3};\ v_{bn} = i_b R = -\frac{2V_{in}}{3}$$

Figure 5.17: Three-phase bridge inverter operating in mode 1 with a load connected to a star

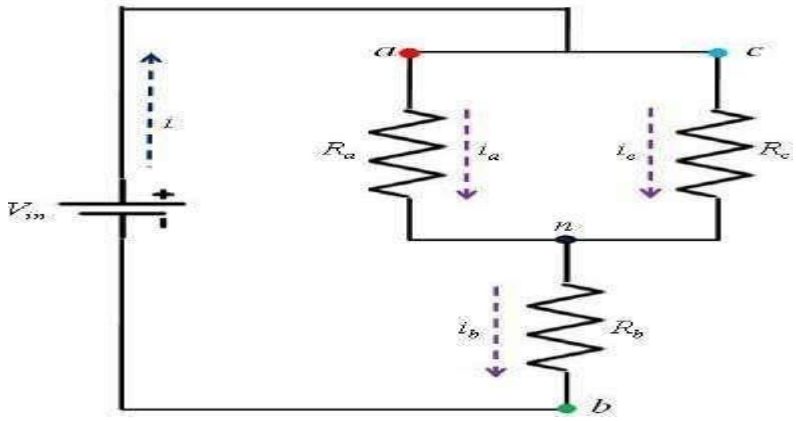


Figure 5.18: Mode 1 operation with current flow

Mode 2: The switches S6, S1, and S2 are activated for a period of time in this mode. Figure 1 depicts the current flow, whereas Figure 2 shows the corresponding circuits. After the

explanation provided for mode 1, the voltage drops and currents flowing across each branch are provided by

(6) $$i_b = i_c = \frac{1}{3}\frac{V_{in}}{R};\ i_a = -\frac{2}{3}\frac{V_{in}}{R}$$

(7)

$$v_{bn} = v_{cn} = \frac{V_{in}}{3};\ v_{an} = -\frac{2V_{in}}{3}$$

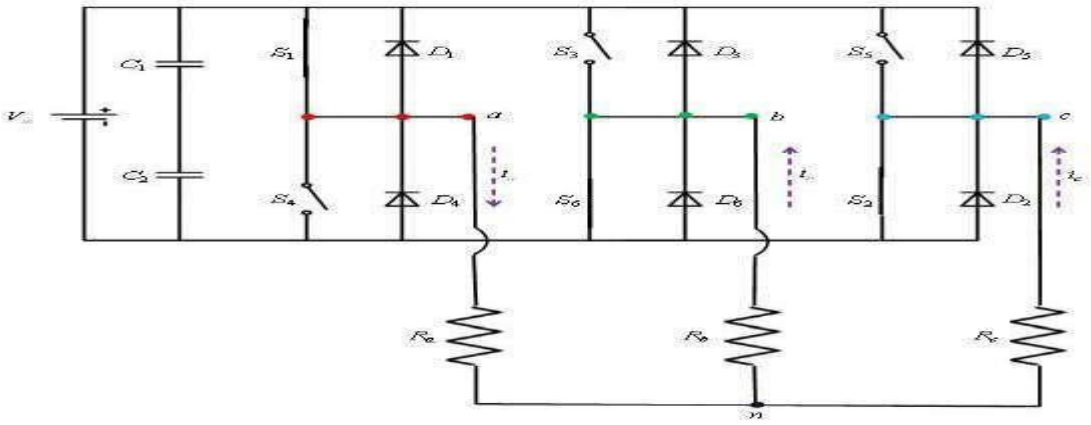


Figure 5.19 Three-phase bridge inverter operating in mode two with a load connected to a star

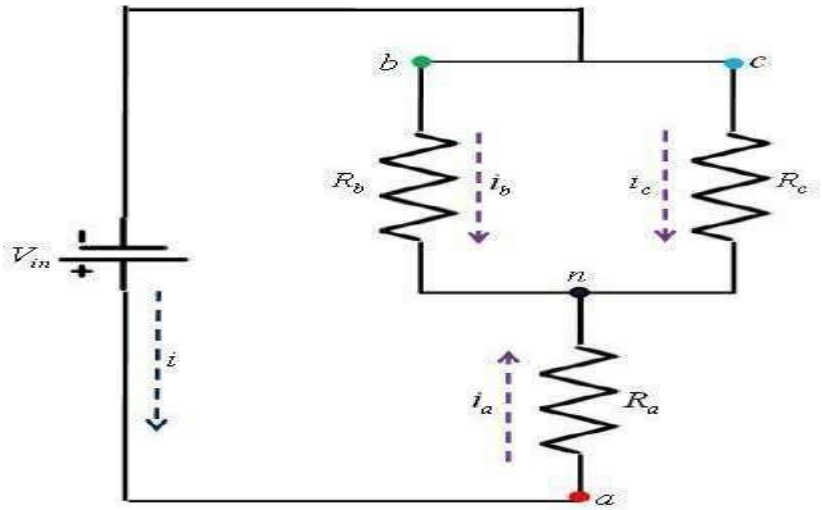


Figure 5.20: Mode 2 operation with current flow

Mode 3: The switches S1, S2, and S3 are turned on during this mode. Figure 1 depicts the current flow, whereas Figure 2 shows the corresponding circuits. The voltage and current magnitudes

are:

$$i_a = i_b = \frac{1}{3}\frac{V_{in}}{R};\ i_c = -\frac{2}{3}\frac{V_{in}}{R}$$

(8)

$$v_{an} = v_{bn} = \frac{V_{in}}{3};\ v_{cn} = -\frac{2V_{in}}{3}$$

(9)

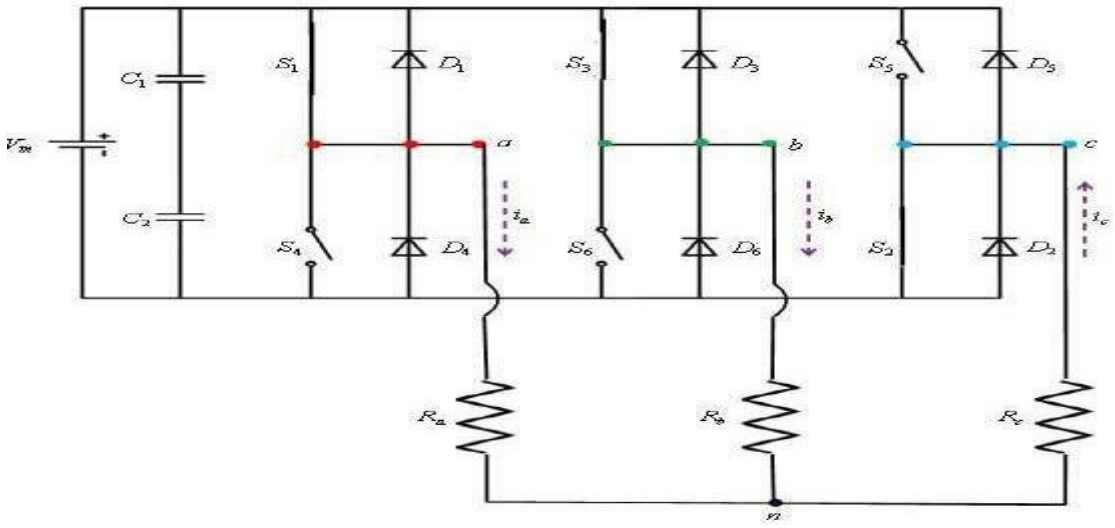


Figure 5.21: Three-phase bridge inverter operating in mode three with a load connected to a star

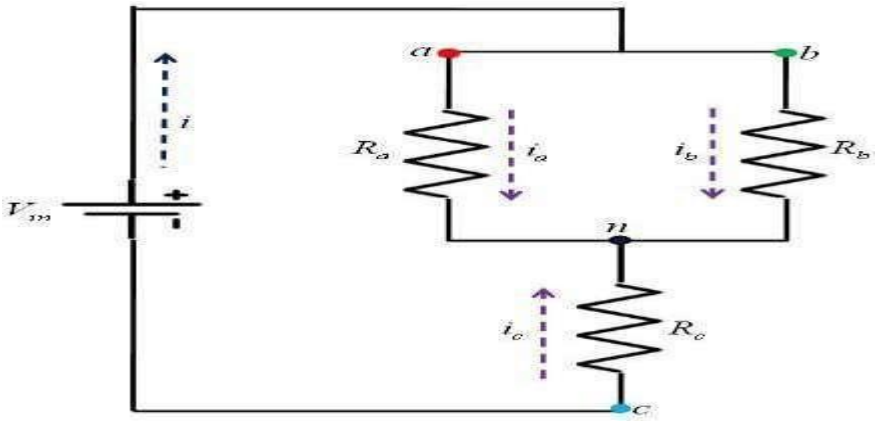


Figure 5.23: Mode 3 operation with current flow

The analogous circuits for modes 4, 5, and 6 will be identical to those for modes 1, 2, and 3, respectively. Each mode's voltages and currents are as follows:

for mode 4 (10).

$$\left.\begin{aligned} i_a = i_c = -\frac{1}{3}\frac{V_{in}}{R};\ i_b = \frac{2}{3}\frac{V_{in}}{R} \\ v_{an} = v_{cn} = -\frac{V_{in}}{3};\ V_{bn} = \frac{2V_{in}}{3} \end{aligned}\right\}$$

for mode 5 (11).

$$\left.\begin{aligned} i_b = i_c = -\frac{1}{3}\frac{V_{in}}{R};\ i_a = \frac{2}{3}\frac{V_{in}}{R} \\ v_{bn} = v_{cn} = -\frac{V_{in}}{3};V_{an} = \frac{2V_{in}}{3} \end{aligned}\right\}$$

for mode 6 (12).

$$\left.\begin{aligned} i_a = i_b = -\frac{1}{3}\frac{V_{in}}{R};\ i_c = \frac{2}{3}\frac{V_{in}}{R} \\ v_{an} = v_{bn} = -\frac{V_{in}}{3};V_{cn} = \frac{2V_{in}}{3} \end{aligned}\right\}$$

Figure displays the plots of the currents (ia, ib, and ic) and phase voltages (van, vbn, and vcn).

The line voltages may also be calculated using the phase voltages as a guide:

$$v_{ab} = v_{an} - v_{bn}$$
$$v_{bc} = v_{bn} - v_{cn}$$
$$v_{ca} = v_{cn} - v_{an}$$

(13)

Figure also displays the line voltage charts. The phase and line voltages may be represented using Fourier series as follows:

$$v_{an} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{in}}{3n\pi}\left[1 + \sin\frac{n\pi}{2}\sin\frac{n\pi}{6}\right]\sin(n\omega t)$$
$$v_{bn} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{in}}{3n\pi}\left[1 + \sin\frac{n\pi}{2}\sin\frac{n\pi}{6}\right]\sin\left(n\omega t - \frac{2n\pi}{3}\right)$$
$$v_{cn} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{in}}{3n\pi}\left[1 + \sin\frac{n\pi}{2}\sin\frac{n\pi}{6}\right]\sin\left(n\omega t - \frac{4n\pi}{3}\right)$$

(14)

$$v_{ab} = v_{an} - v_{bn} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{in}}{n\pi} \sin\frac{n\pi}{2} \sin\frac{n\pi}{3} \sin\left(n\omega t + \frac{n\pi}{6}\right)$$

$$v_{bc} = v_{bn} - v_{cn} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{in}}{n\pi} \sin\frac{n\pi}{2} \sin\frac{n\pi}{3} \sin\left(n\omega t - \frac{n\pi}{2}\right)$$

$$v_{ca} = v_{cn} - v_{an} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{in}}{n\pi} \sin\frac{n\pi}{2} \sin\frac{n\pi}{3} \sin\left(n\omega t - \frac{7n\pi}{6}\right)$$

(15)

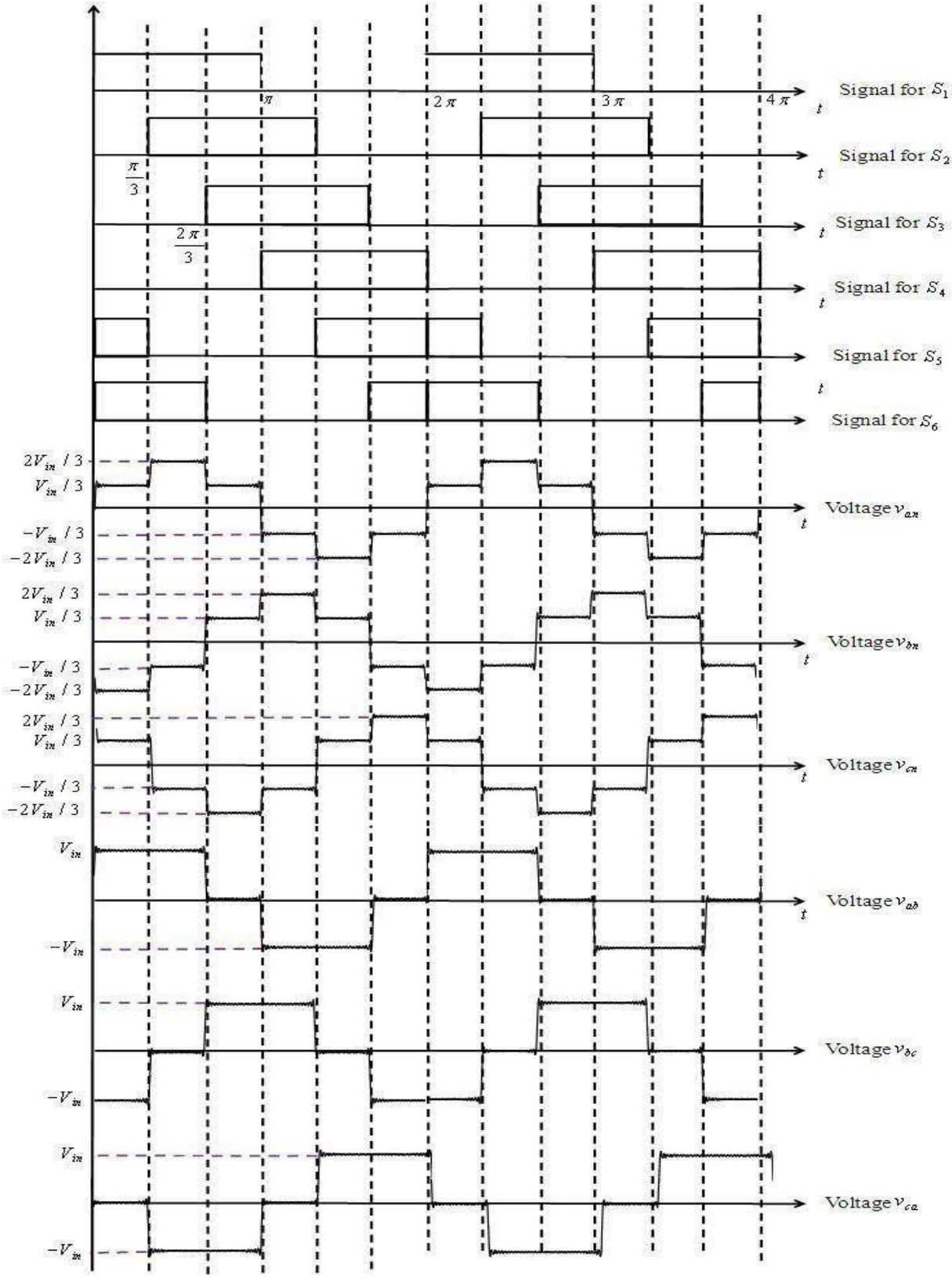


Figure 5.24: Three-phase bridge inverter's line and phase voltages

Three-phase DC-AC converters having a conduction mode of 120 degrees

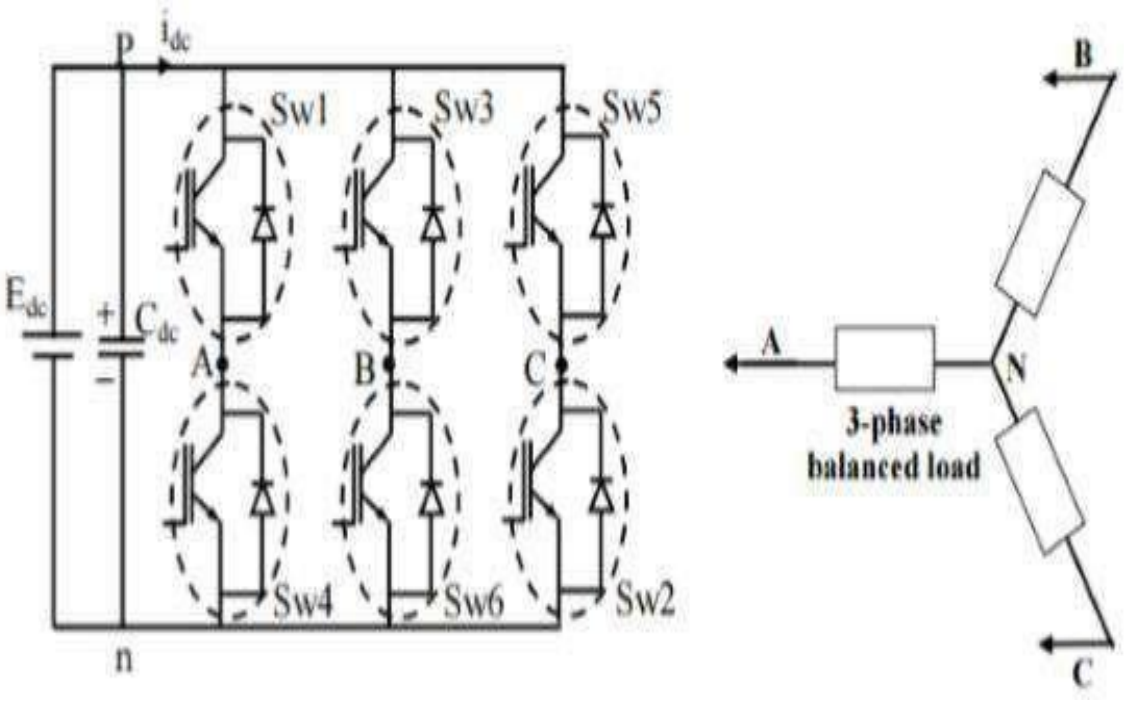


Figure 5.25: Three-phase bridge inverter circuit schematic

120° conduction mode

Every electrical equipment is in a conduction state for 120° while using this conduction mode. Because it produces a six-step waveform over all of its phases, it works best with a delta connection in a load. Since each device conducts at a mere 120°, there are only ever two devices conducting at any one time.

The load's terminal A is attached to the source's positive end, while terminal B is attached to its negative end. The load's terminal C is in a state known as the floating state. Additionally, as can be seen below, the phase voltages match the load voltages.

Line voltages VAB = V = phase voltages

With VBC = -V/2 and VCA = -V/2

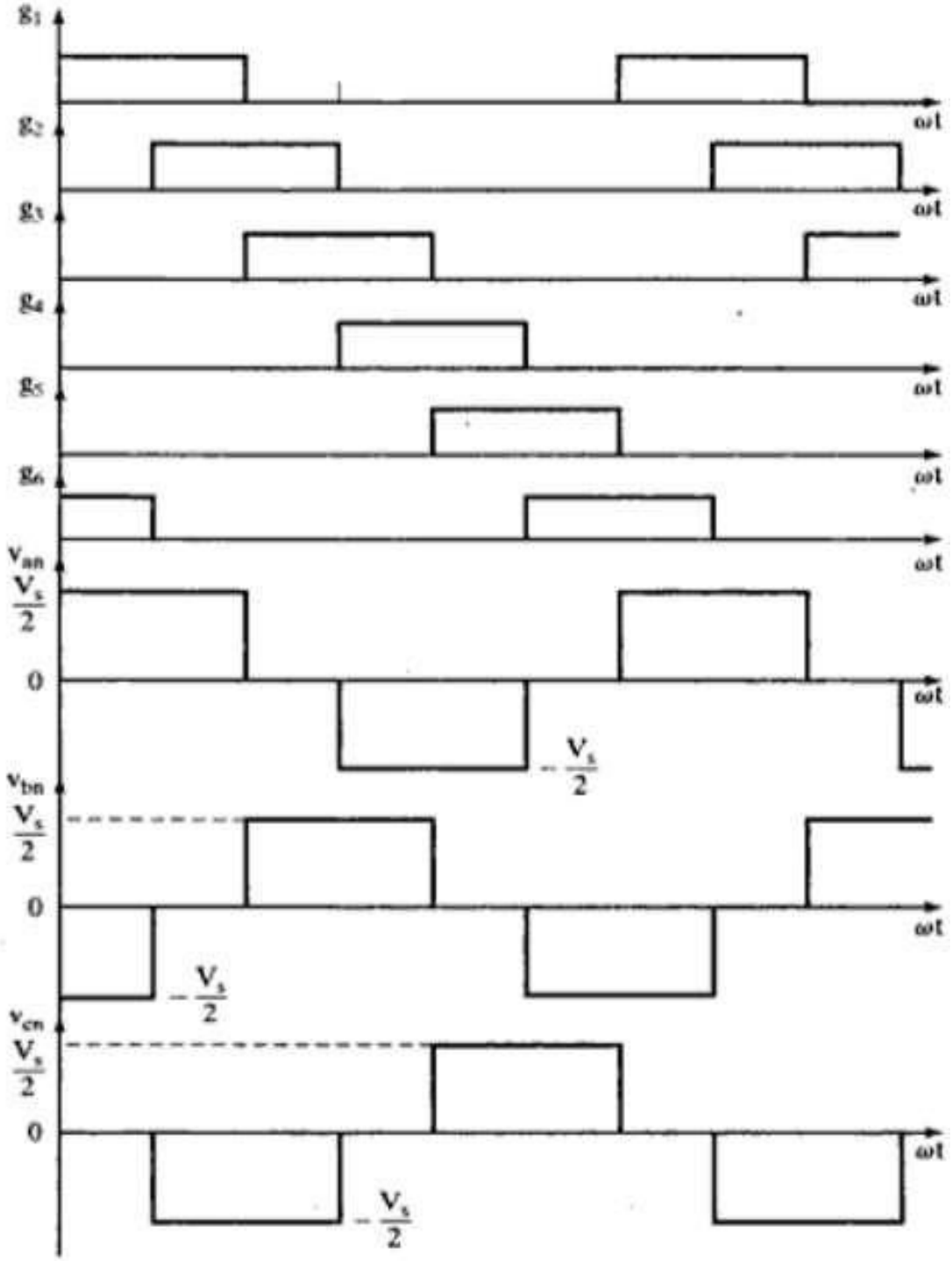


Figure 5.26: Three-phase bridge inverter's line and phase voltages

Techniques for controlling inverter voltage

Techniques for pulse width modulation

One method for lowering a load current's overall harmonic distortion (THD) is PWM. It makes use of a rectangular/square pulse wave that, once its pulse width has been modified, yields a variable average waveform value f(t). T provides the modulation time period. Consequently, the average value of the waveform is provided by

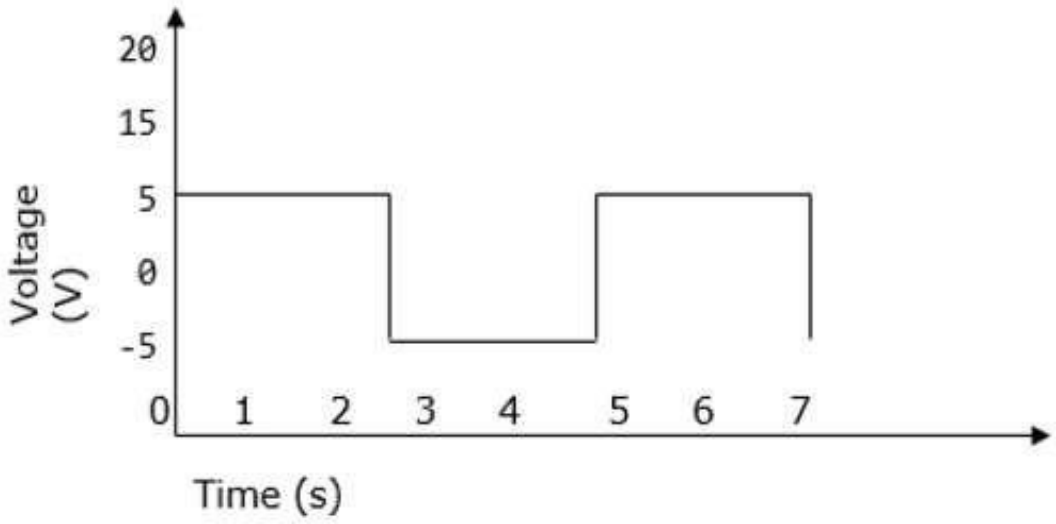


Figure 5.27: PWM approach using a square waveform

Sinusoidal Pulse Width Modulation:

The switches of a basic source voltage inverter may be switched on and off as necessary. The switch is switched on or off once throughout each cycle. The waveform is square as a consequence. On the other hand, an enhanced waveform with a harmonic profile is produced if the switch is activated repeatedly.

By contrasting the intended modulated waveform with a high-frequency triangular waveform, the sinusoidal PWM waveform is produced. The DC bus's output voltage is either positive or negative, depending on whether the signal's voltage is higher or lower than the carrier waveform's.

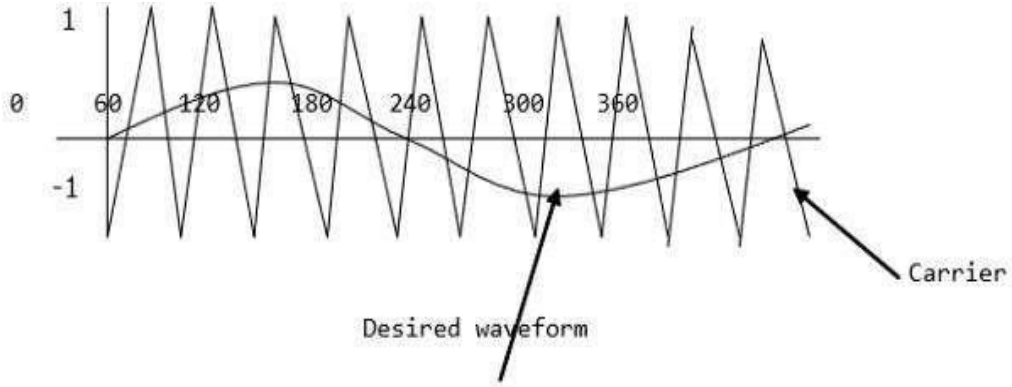


Figure 5.28: Waveform of a sinusoidal PWM

Am and Ac stand for sinusoidal amplitude and carrier triangle amplitude, respectively. Am/Ac provides the modulating index m for sinusoidal PWM.

Modified sinusoidal PWM waveform:

For power management and power factor optimisation, a modified sinusoidal PWM waveform is used. By altering the PWM converter, the primary idea is to transfer grid-delayed current to the voltage grid. As a result, both power factor optimisation and power efficiency are increased.

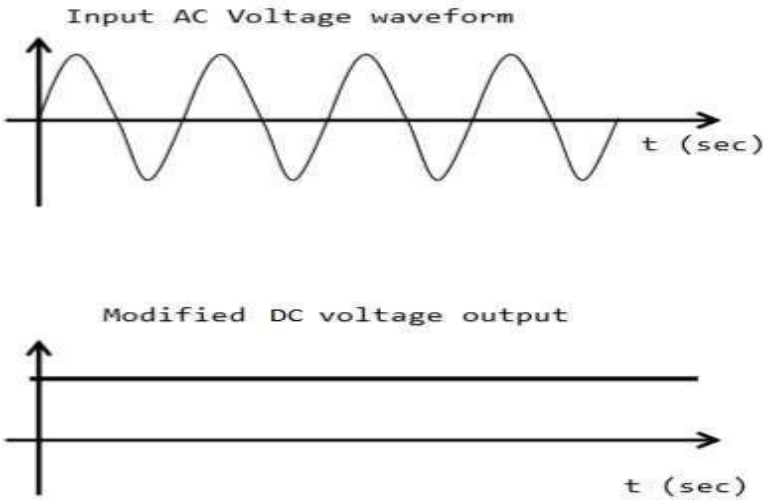


Figure 5.29: Modified PWM waveform with sinusoidal waves

Several PWM:

Although the multiple PWM produces a large number of outputs with varying values, the time period during which they are generated remains constant. PWM inverters may function at high output voltages.

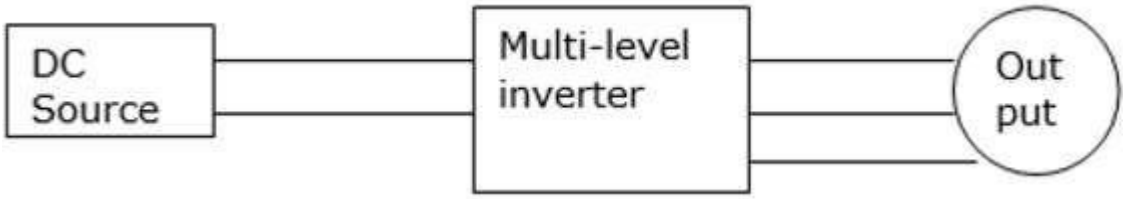


Figure 5.30: Multiple PWM method block diagram

A multiple PWM creates the sinusoidal waveform seen below.

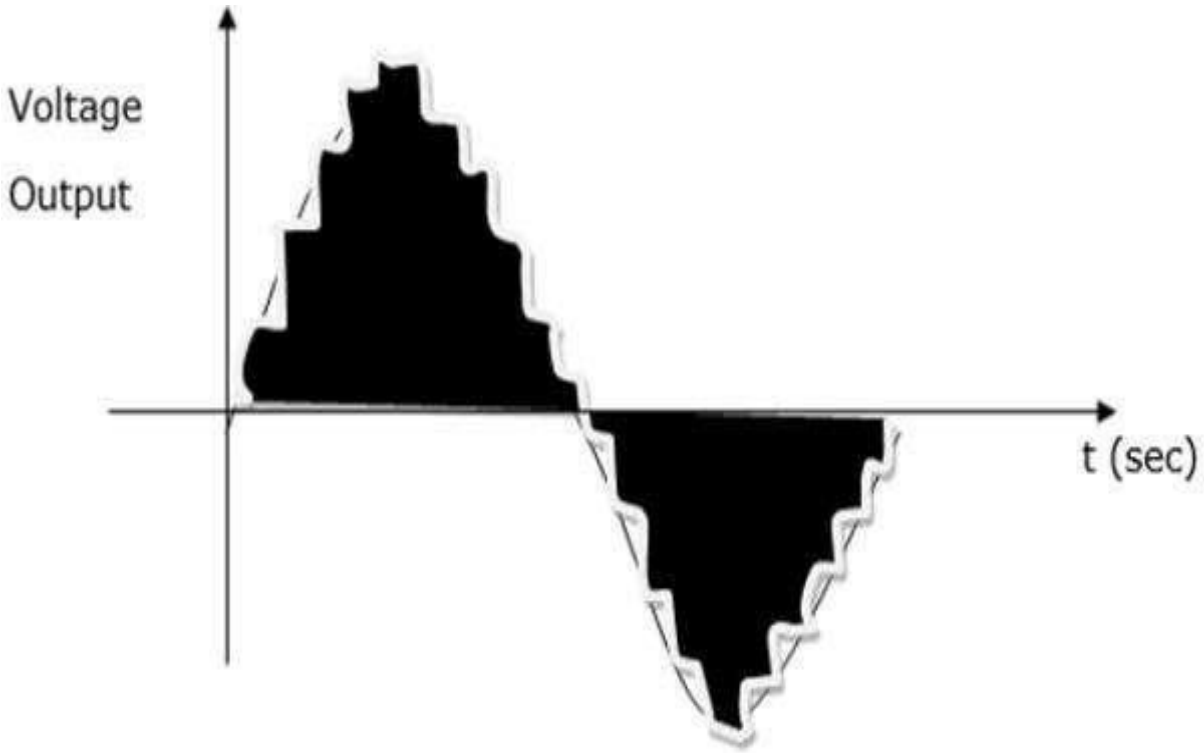


Figure 5.31: Multiple PWM method waveform

Voltage and Harmonic Regulation

A harmonic is a periodic waveform whose frequency is a multiple integral of the fundamental power at a frequency of 60 Hz. Conversely, total harmonic distortion (THD) is the sum of the contributions from all harmonic current frequencies.

The pulse that indicates how many rectifiers are being utilised in a certain circuit is what defines harmonics.

The formula for it is h=(n×P)+1or−1.

In this case, n − is an integer between 1 and 4.

P - The quantity of rectifiers

Isolation transformers, line reactors, power system restructuring, and harmonic filters are some ways to lessen harmonics, which affect the output of voltage and current.

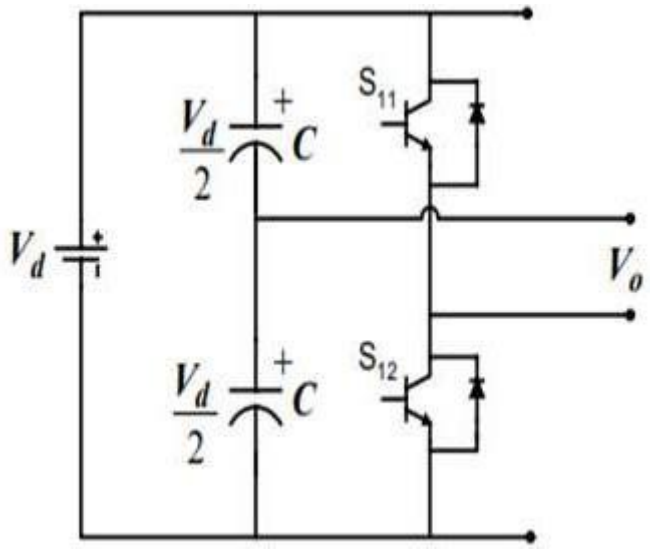


Figure 5.32: Half bridge PWM inverter schematic diagram

How sinusoidal pulse width modulation works

In industrial applications, the sinusoidal PWM (SPWM) method—also referred to as the sub-oscillation, sub-harmonic, or triangulation method—is widely used. The half-bridge circuit architecture for a single-phase inverter, shown in Figure, is used to illustrate the SPWM.

A high-frequency triangular carrier wave is compared to a sinusoidal reference of the target frequency in order to achieve SPWM. The modulated pulse's commutation and switching instants are determined by the intersection of and waves. The PWM system is shown in Figure, where vr is the reference, or modulating signal, and vc is the peak value of the triangular carrier wave. The triangle and modulation signal with an arbitrary frequency and magnitude are shown in the figure. The switches in the inverter shown in Figure are controlled by comparing the control signal with the triangle wave that is mixed in a comparator. The comparator output is high when the sinusoidal wave is larger than the triangle wave; otherwise, it is low.

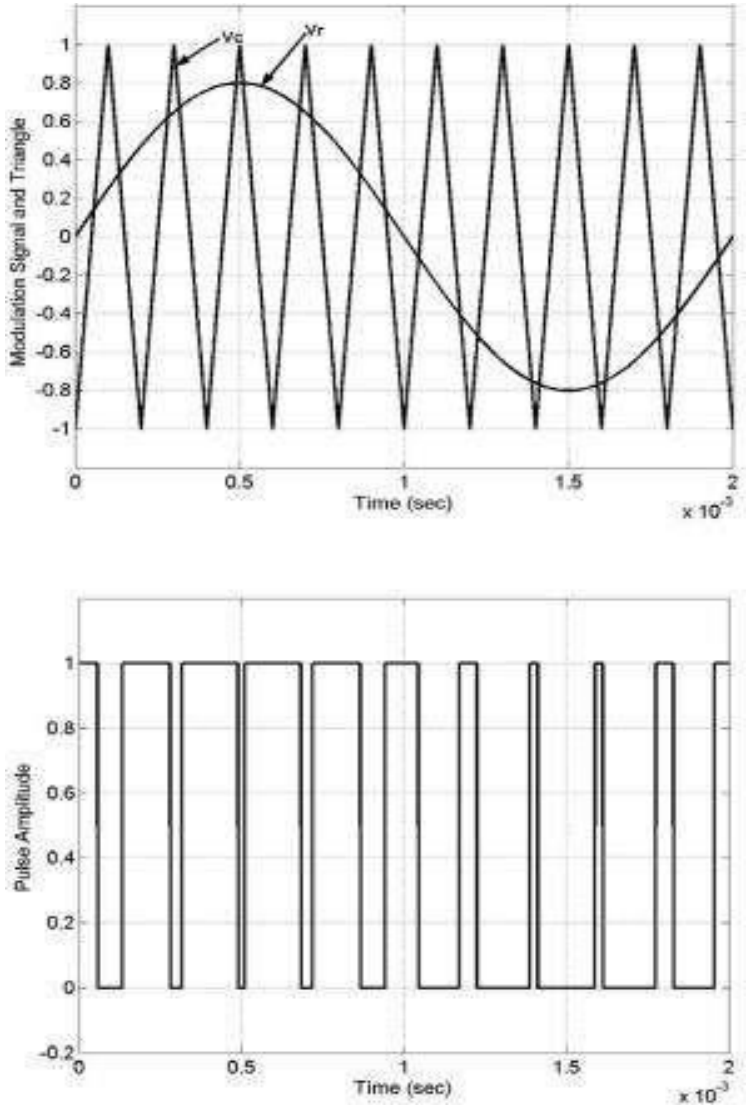


Figure 5.33: Half bridge PWM inverter switching pulses and sine-triangle comparison

In a trigger pulse generator, the comparator output is processed such that the inverter's output voltage wave has a pulse width that matches the comparator output pulse width. The modulation index (MI), which regulates the output voltage waveform's harmonic content, is the magnitude ratio of Vr/VC. The output voltage's basic component magnitude is proportional to MI. Typically, the triangle wave's amplitude is maintained at a consistent level. The definition of the frequency modulation ratio is

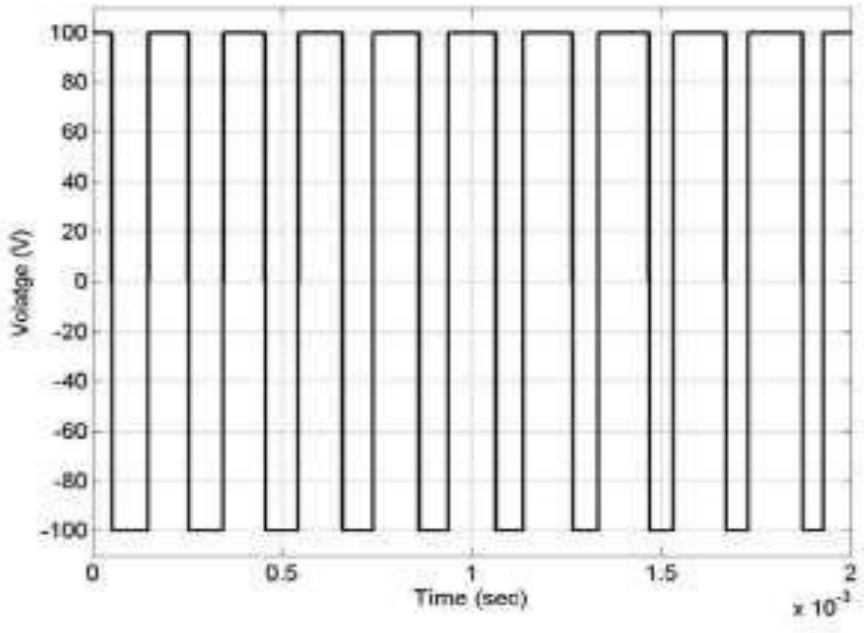


Figure 5.34: Half-Bridge inverter output voltage

Functioning of a single-phase current source inverter with optimal switches

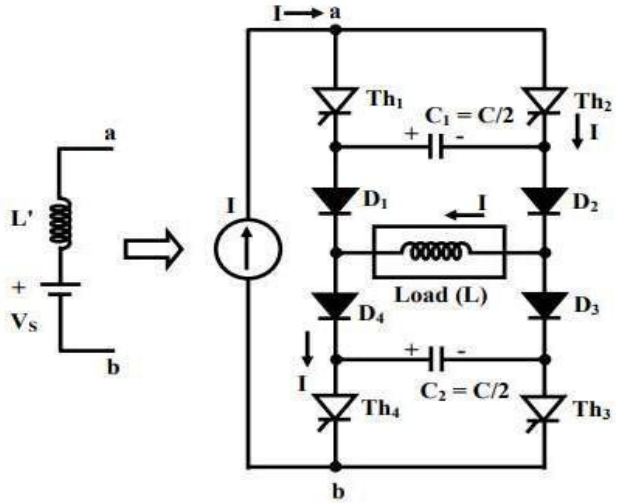


Figure 5.35: ASCI type single phase current source inverter (CSI)

Fig. depicts the circuit of a single-phase Current Source Inverter (CSI). 5.35. Auto-Sequential Commutated Inverter (ASCI) is the name given to this sort of operation. Here, a continuous current source is expected, which may be achieved by connecting the current-limited dc voltage source in series with an appropriate inductance, which has to be high. To create a waveform of current that is almost square, the thyristor pairs Th1 & Th3 and Th2 & Th4 are alternately switched ON. C1 and C2, two commutating capacitors, are employed in the top and lower halves, respectively. To stop the commutating capacitors from discharging into the load, each thyristor is linked in series with four diodes, D1–D4. As can be seen from the waveforms (Fig. 5.36), the inverter's output frequency is adjusted as usual by adjusting the half time period, T/2, at which the thyristors in a pair are activated by pulses supplied to the corresponding gates by the control circuit. Because the reason or reasons are generally known, the inductance (L) is assumed to represent the load in this instance. There are two modes that describe the operation.

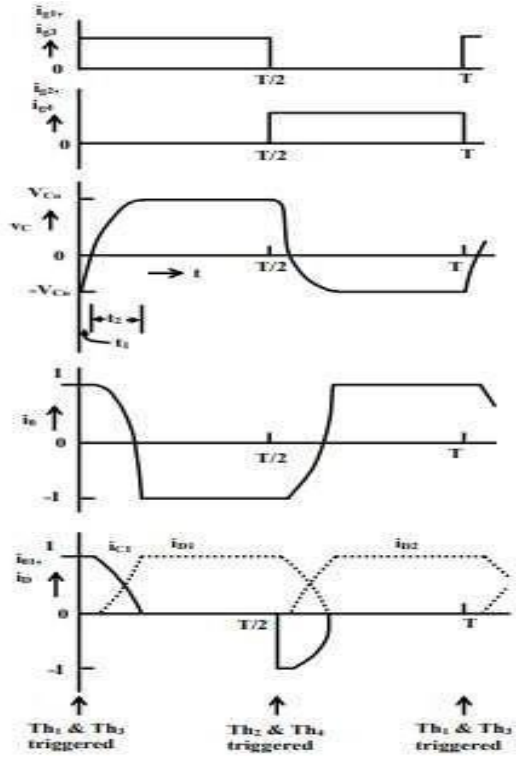


Figure 5.36 shows the single phase current source inverter's output waveforms.

Mode I: Fig. displays the circuit for this mode. 5.37. These are the presumptions. The current (I) flows along the route, Th2, D2, load (L), D4, Th4, and source, I, as soon as the thyristor pair, Th − t = 0 2 & Th4, is conducting (ON). At first, the commutating capacitors are charged uniformly with the specified polarity, i.e. This indicates that the left hand plate is negative and the right hand plate is positive for both capacitors. Two capacitors must be pre-charged if they are not originally charged.

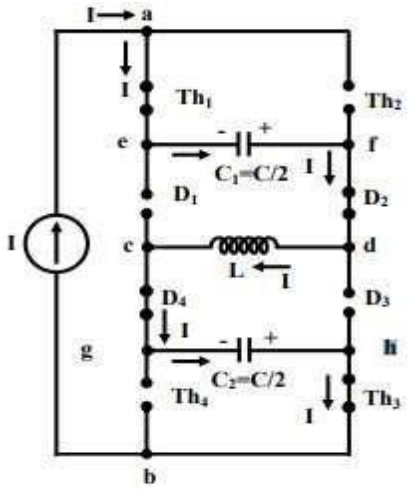


Figure 5.37: CSI's Mode I operation

Mode II: Fig. displays the circuit for this mode. 5.38. Although D2 and D4 diodes are already conducting, at

Diodes, D1 and D3, and tt 1 get forward biassed and begin conducting. As a result, all four diodes, D1–D4, conduct at the end of time t1. Consequently, the load (L) and the commutating capacitors are now linked in parallel.

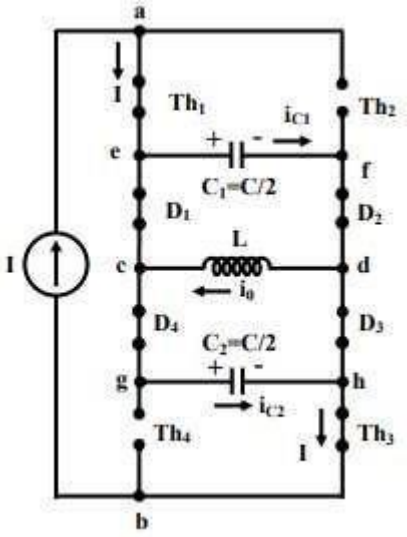


Figure 5.38: CSI operating in Mode II

Commutated Load CSI

The circuit for commutation from one pair of thyristors to the second pair uses four diodes and two commutating capacitors. It has already been shown that forced commutation may not be required in VSI if the load is capacitive. This section discusses the functioning of a single-phase CSI with a capacitive load (Fig. 5.39). It should be mentioned that the resistive load (R) and the capacitor (C) are presumed to be connected in parallel. As will be shown, the charge, or voltage, needed to force-commutate the conducting thyristor pair is stored in the capacitor, C. The circuit's input is either a voltage source with a high inductance or a constant current source, as was the case in the previous lesson.

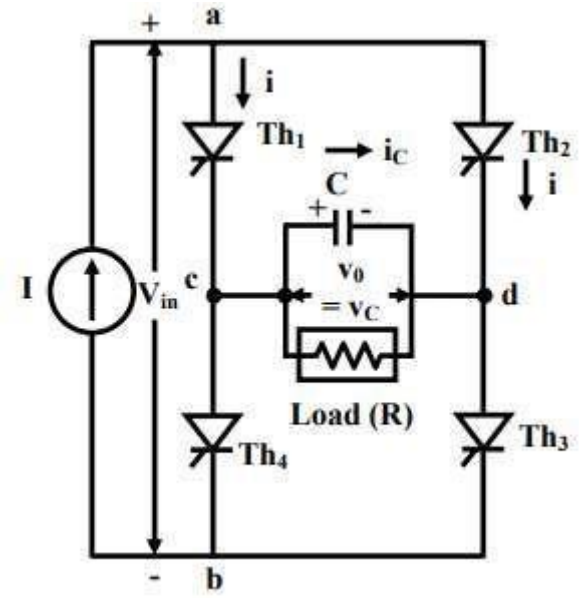


Figure 5.39: Load-commutated CSI circuit schematic

The same power-switching devices—four thyristors in a full-bridge configuration—are used here. Fig. illustrates the load current and voltage moving in a positive manner. 5.40 The capacitor contains a left plate that is negative and a right plate that is positive before t = 0. The thyristor pair, Th2 & Th4, was conducting at the moment. The conducting thyristor pair, Th2 & Th4, is reverse biassed by the capacitor voltage C = −Vv 1 and shuts off instantly when (at t = 0), the thyristor pair, Th1 & Th3, is activated by the pulses supplied at the gates. Th1, the load (a parallel combination of R and C), Th3, and the source are all in the present route. ITi is the current flowing through the thyristors, and the output current is

Iac = I

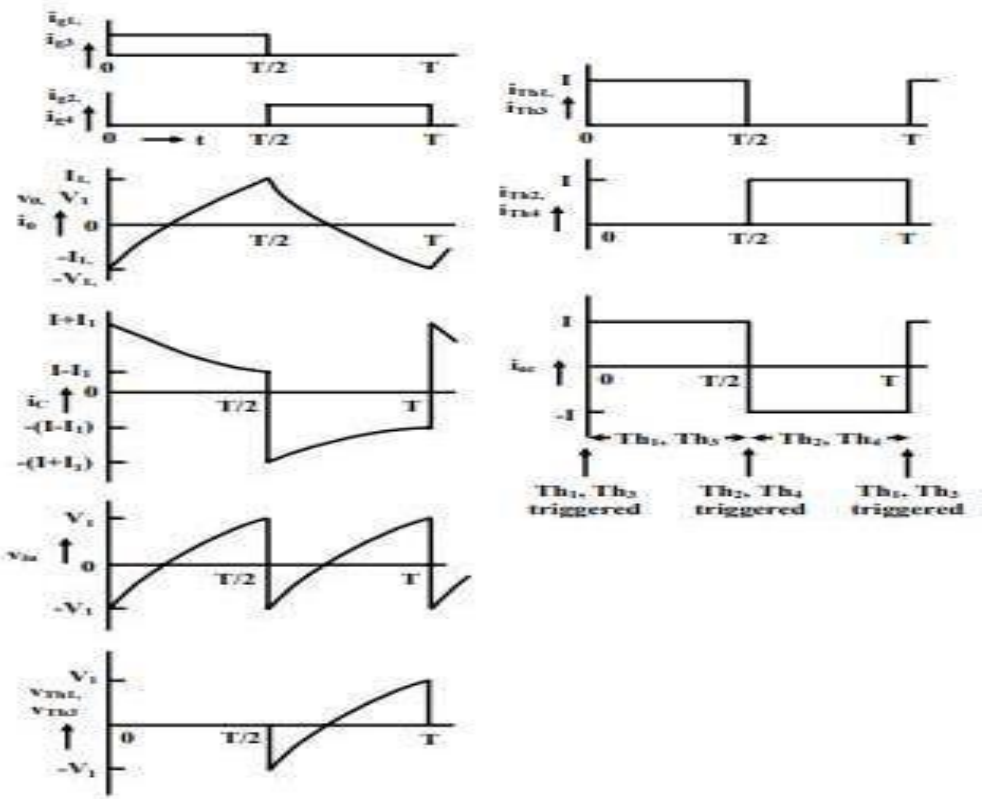


Figure 5.40 shows the load-commutated CSI's voltage and current waveforms.

Numerical Issues

The resistance load of a single-phase half bridge inverter is 2.4 W, and the d.c. 48 V input voltage, ascertain:

voltage of the RMS output at the fundamental frequency

Power output P0

The mean and maximum currents of every transistor

The maximum blocking voltage of every transistor.

distortion factor and total harmonic distortion.

distortion factor and harmonic factor at the lowest harmonic level.

Answer:

E1 = 0.9 ¥ 48 = 43.2 V is the fundamental frequency's RMS output voltage.

Output power = E 2/R = (48)2/2.4 = 960 W; RMS output voltage, Eorms = E = 48 V.

(v) RMS harmonic voltage

$$En = \left[\sum_{n=3,5,7}^{8} E_n^2\right]^{1/2}$$

$$= (E^2_{orms} - E_1{}^2_{rms})^{1/2}$$

$$= [(48)^2 - (43.2)^2]^{1/2}$$

$$= 20.92 \text{ V.}$$

$$\therefore \quad \text{THD} = \frac{20.92}{43.2} = 48.43\%.$$

(vi)
$$\text{D.F.} = \frac{\left[\sum_{n=3,5,7}^{\infty} \left(E_n/n^2\right)^2\right]^{1/2}}{0.9}$$

$$= \frac{0.03424}{0.9} = 3.8\%$$

(vii) Lowest order harmonic is the third harmonic. RMS value of third harmonic is

$$E_{3rms} = E_{1rms}/3$$

$$\therefore \quad H.F_3 = E_{3rms}/E_{1rms} = 33.33\%$$

and
$$D.F._3 = (E_{3rms}/3^2)/E_{1rms}$$

$$= 1/27 = 3.704\%.$$

Ip is equal to Ed/R = 48/2.4 = 20 A, which is the peak transistor current. Ip/2 = 10 A is the average transistor current.

maximum voltage for reverse blocking,

48 V is VBR.

Determine the average output voltage and rms output voltage at fundamental frequency for a single phase full bridge inverter with a resistive load of R = 10 Ω and an input voltage of 100 V.

R=10Ω and L=10 mH are used to supply an RL load from a single PWM full bridge inverter. Determine the overall harmonic distortion in the load current and output voltage if the source voltage is 120V. Each pulse has a width of 120° and an output frequency of 50 Hz.