

UNIT III

BIPOLAR JUNCTION TRANSISTOR

3.1 INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogous to vacuum triode and is comparatively smaller in size. It is used as amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

3.2 CONSTRUCTION OF BJT AND ITS SYMBOLS

The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the **Emitter (E)**, the **Base (B)** and the **Collector (C)** respectively. There are two basic types of bipolar transistor construction, **PNP** and **NPN**, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- 1. Active Region - the transistor operates as an amplifier and $I_c = \beta I_b$
- 2. Saturation - the transistor is "fully-ON" operating as a switch and $I_c = I_{(saturation)}$
- 3. Cut-off - the transistor is "fully-OFF" operating as a switch and $I_c = 0$

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types **PNP** and **NPN**, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type(fig 1).

Bipolar Transistor Construction

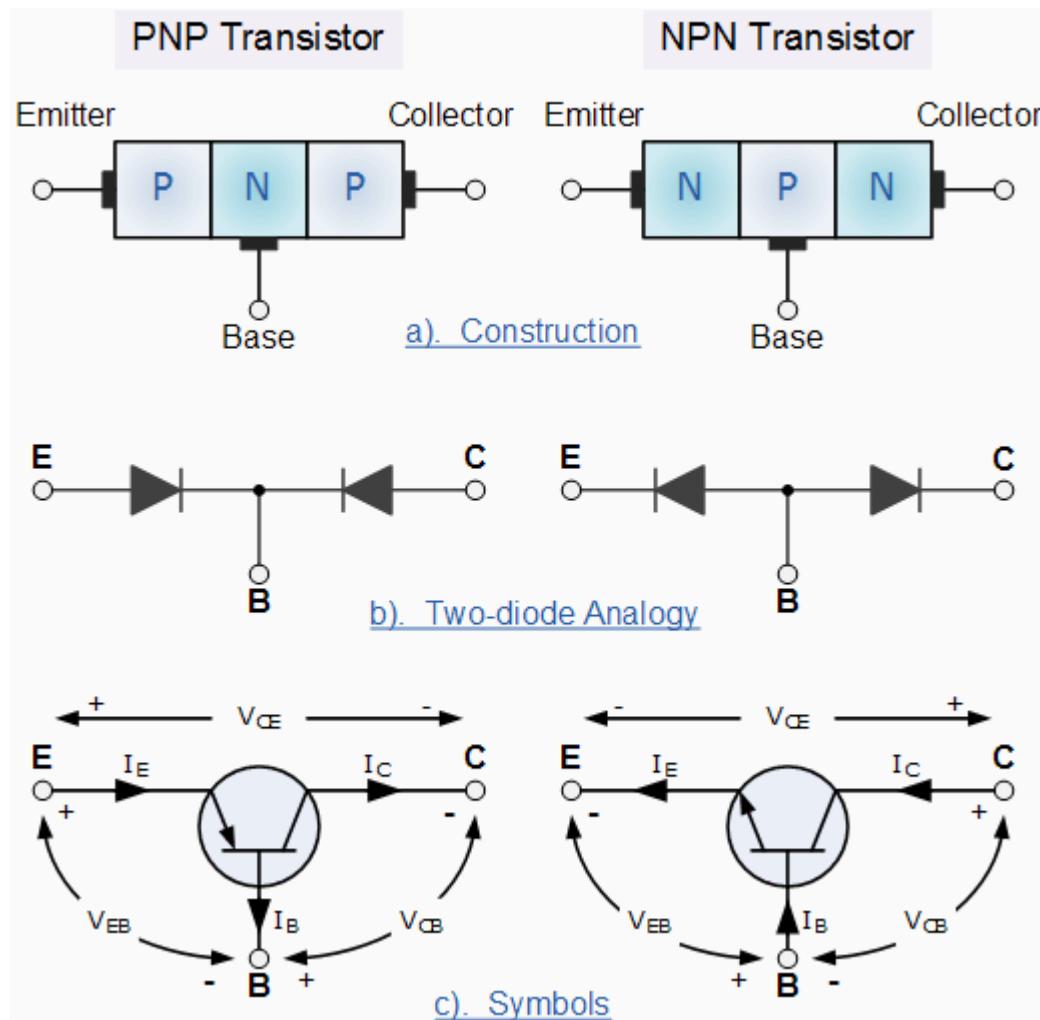


Fig 3.1 Bipolar Junction Transistor Symbol

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

3.3 TRANSISTOR CURRENT COMPONENTS:

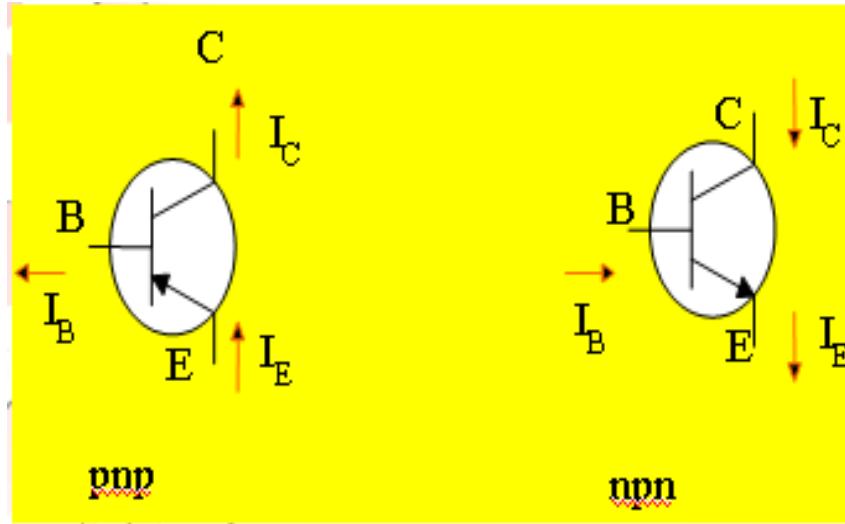


Fig 3.2 Bipolar Junction Transistor Current Components

The above fig 3.2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current I_E consists of hole current I_{pE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into emitter).The ratio of hole to electron currents, I_{pE} / I_{nE} , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter do not contribute carriers, which can reach the collector.

Not all the holes crossing the emitter junction J_E reach the the collector junction J_C

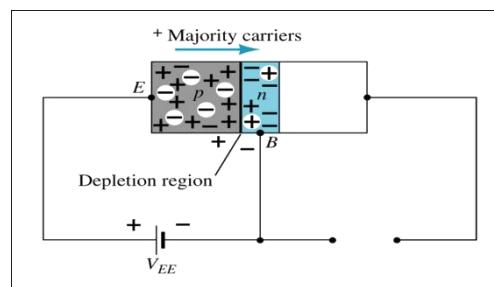
Because some of them combine with the electrons in n-type base. If I_{pc} is hole current at junction J_C there must be a bulk recombination current ($I_{pE} - I_{pc}$) leaving the base.

Actually, electrons enter the base region through the base lead to supply those charges, which have been lost by recombination with the holes injected in to the base across J_E . If the emitter were open circuited so that $I_E=0$ then I_{pC} would be zero. Under these circumstances, the base and collector current I_C would equal the reverse saturation current I_{CO} . If $I_E \neq 0$ then

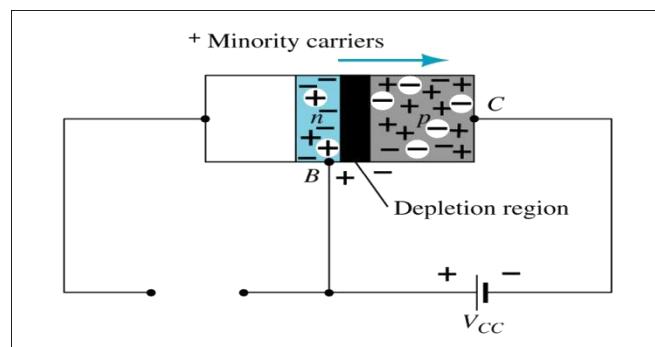
$$I_C = I_{CO} - I_{pC}$$

For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in opposite direction. Assumed referenced direction for I_{CO} i.e. from right to left, then for a p-n-p transistor, I_{CO} is negative. For an n-p-n transistor, I_{CO} is positive. The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

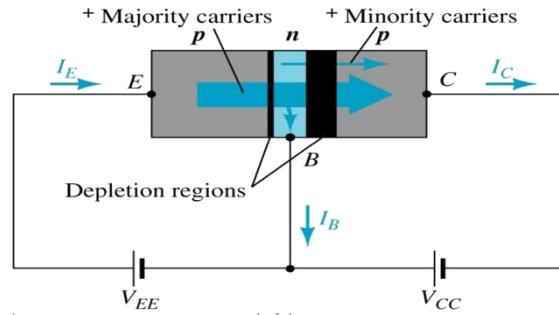
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.



3.3a Forward-biased junction of a pnp transistor



3.3b Reverse-biased junction of a pnp transistor



3.3c Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will through n-type material to the base terminal. Resulting I_B is typically in order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal

Applying KCL to the transistor :

$$I_E = I_C + I_B$$

The comprises of two components – the majority and minority carriers

$$I_C = I_{C\text{majority}} + I_{C\text{Ominority}}$$

$I_{CO} - I_C$ current with emitter terminal open and is called leakage current

Various parameters which relate the current components is given below

Emitter efficiency:

$$\gamma = \frac{\text{current of injected carriers at } J_E}{\text{total emitter current}}$$

$$\gamma = \frac{I_{PE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

Transport Factor:

$$\beta^* = \frac{\text{injected carrier current reaching } J_C}{\text{injected carrier current at } J_E}$$

$$\beta^* = \frac{I_{pC}}{I_{nE}}$$

Large signal current gain:

The ratio of the negative of collector current increment to the emitter current change from zero (cut-off) to I_E the large signal current gain of a common base transistor.

$$\alpha = \frac{-(I_C - I_{CO})}{I_E}$$

Since I_C and I_E have opposite signs, then α , as defined, is always positive. Typically numerical values of α lies in the range of 0.90 to 0.995

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{nE}} * \frac{I_{pE}}{I_E} \quad \alpha = \beta^* \gamma$$

The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio α^* is unity. α^* is the ratio of total current crossing J_C to hole arriving at the junction.

3.4 Bipolar Transistor Configurations

As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no Current Gain.
- 2 Common Emitter Configuration - has both Current and Voltage Gain.
- 3. Common Collector Configuration - has Current Gain but no Voltage Gain.

3.5 COMMON-BASE CONFIGURATION

Common-base terminology is derived from the fact that the base is common to both input and output of the configuration. The base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

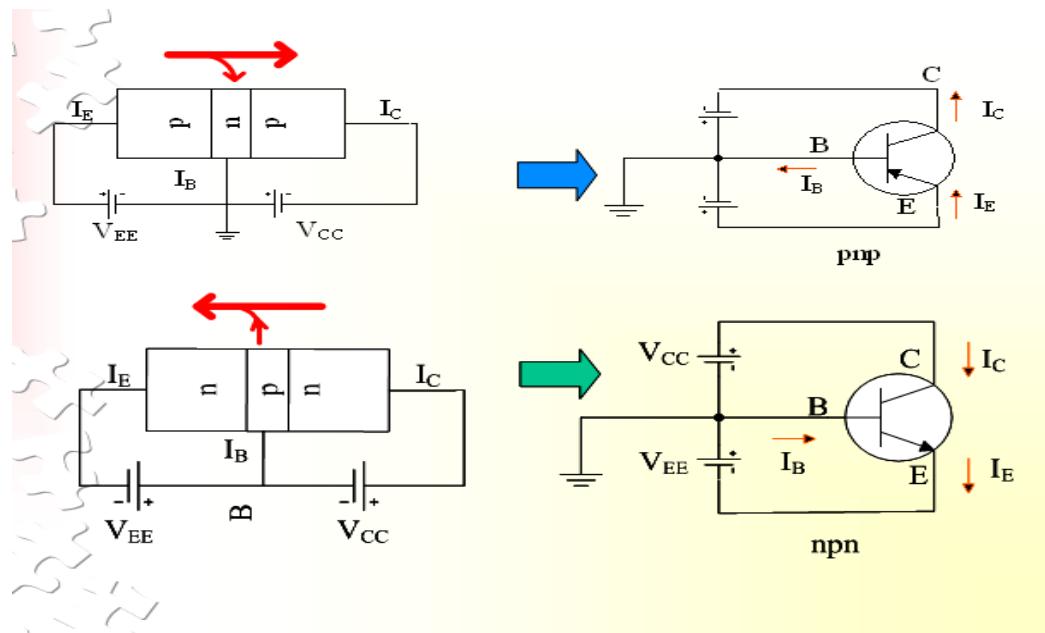


Fig 3.4 CB Configuration

To describe the behavior of common-base amplifiers requires two sets of characteristics:

1. Input or driving point characteristics.
2. Output or collector characteristics

The output characteristics has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A

- Saturation region- region of the characteristics to the left of $V_{CB} = 0V$

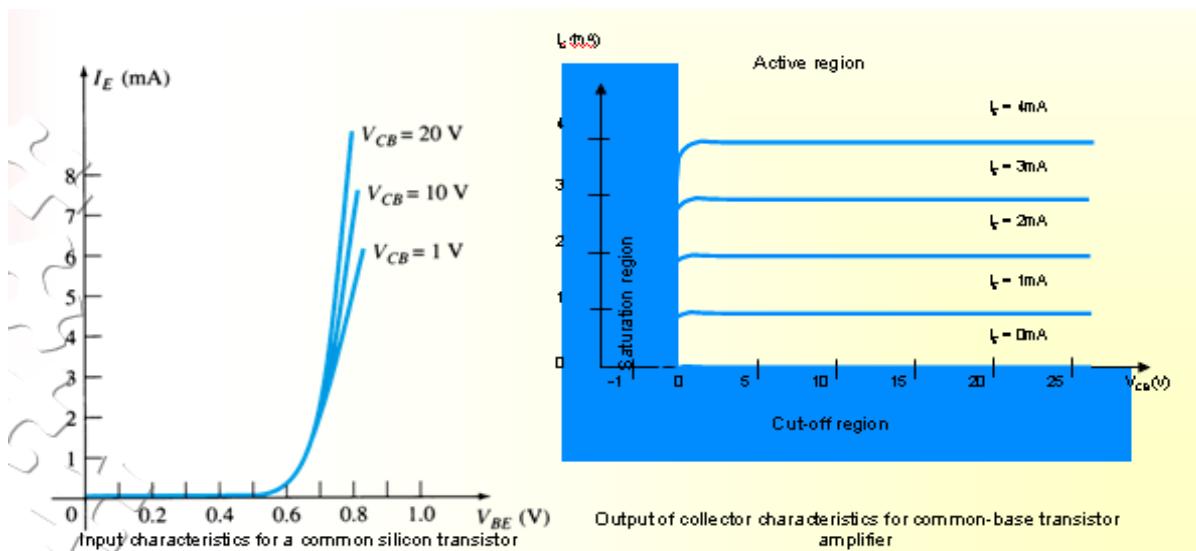


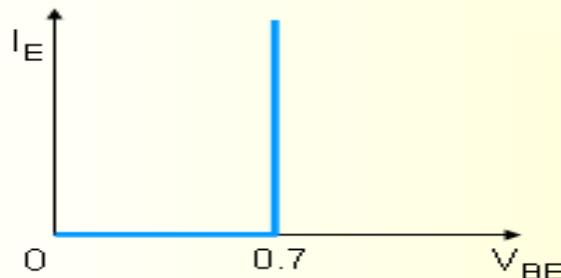
Fig 3.5 CB Input-Output Characteristics

Active region	Saturation region	Cut-off region
<ul style="list-style-type: none"> • I_E increased, I_C increased • BE junction forward bias and CB junction reverse bias • Refer to the <u>graf</u>, $I_C \approx I_E$ • I_C not depends on V_{CB} • Suitable region for the transistor working as amplifier 	<ul style="list-style-type: none"> • BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to I_C • The allocation for this region is to the left of $V_{CB} = 0V$. 	<ul style="list-style-type: none"> • Region below the line of $I_E=0A$ • BE and CB is reverse bias • no current flow at collector, only leakage current

The curves (output characteristics) clearly indicate that a first approximation to the relationship between I_E and I_C in the active region is given by

$$I_C \approx I_E$$

Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be $V_{BE} = 0.7V$



In the dc mode the level of I_C and I_E due to the majority carriers are related by a quantity called alpha
 $\alpha = \alpha_{dc}$

$$I_C = \alpha I_E + I_{CBO}$$

It can then be summarize to $I_C = \alpha I_E$ (ignore I_{CBO} due to small value)

For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by α_{ac}

Alpha a common base current gain factor that shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of α is typical from $0.9 \sim 0.998$.

Biassing: Proper biassing CB configuration in active region by approximation $I_C \approx I_E$ ($I_B \approx 0 \text{ uA}$)

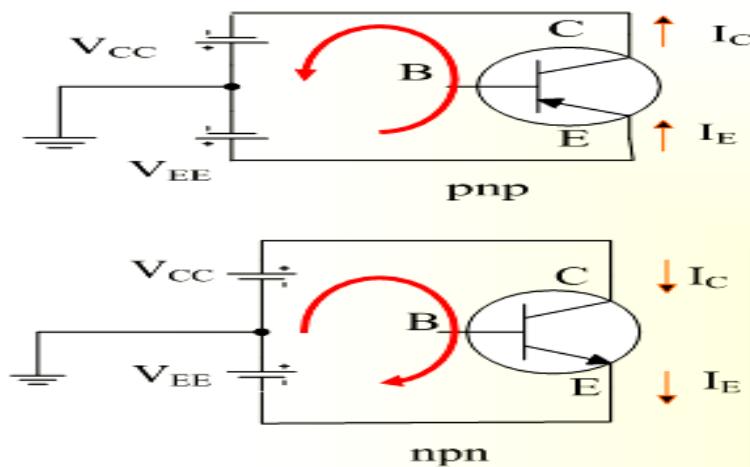


Fig 3.6 CE Configuration

3.6 TRANSISTOR AS AN AMPLIFIER

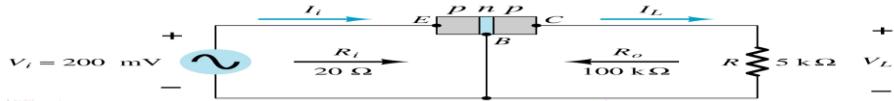


Fig 3.7 Basic Transistor Amplifier Circuit

Common-Emitter Configuration

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals.emitter is usually the terminal closest to or at ground potential.

Almost amplifier design is using connection of CE due to the high gain for current and voltage.

Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region

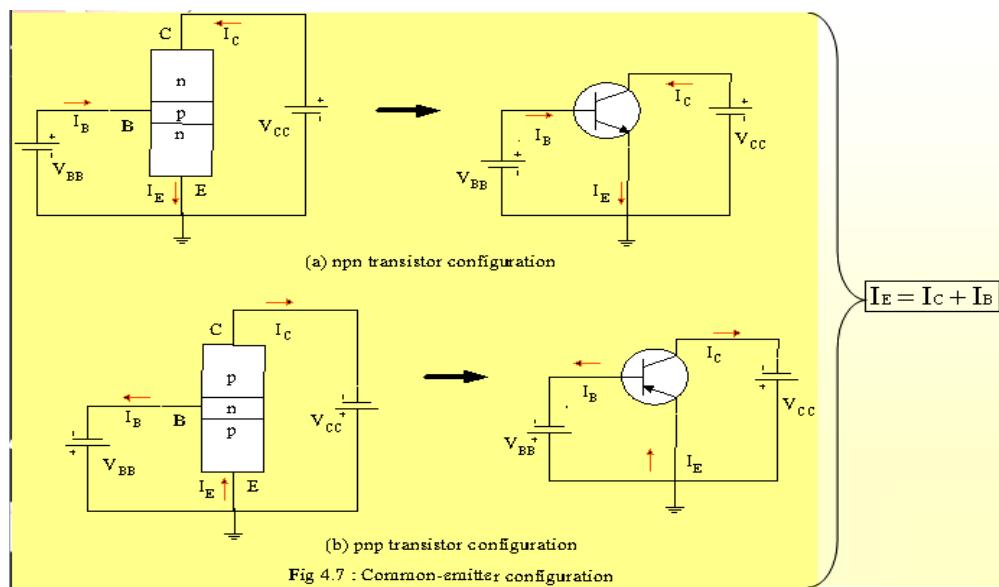


Fig 3.8 CE Configuration

I_B is microamperes compared to miliamperes of I_C .

I_B will flow when $V_{BE} > 0.7V$ for silicon and $0.3V$ for germanium

Before this value I_B is very small and no I_B .

Base-emitter junction is forward bias Increasing V_{CE} will reduce I_B for different values.

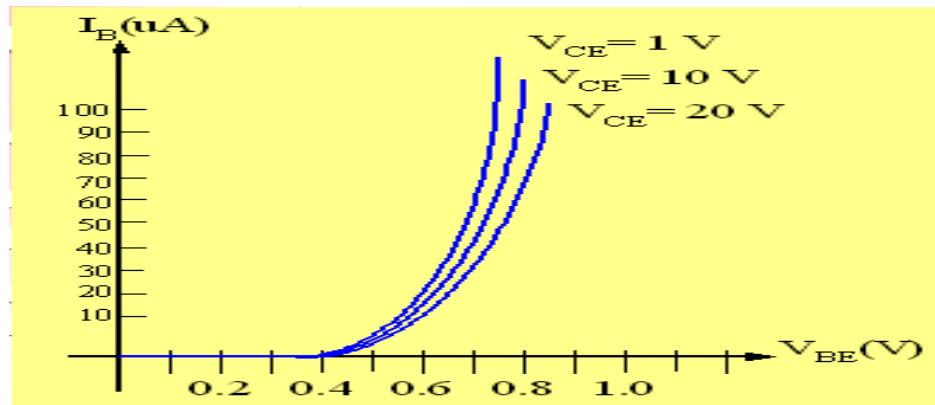


Fig 3.9a Input characteristics for common-emitter npn transistor

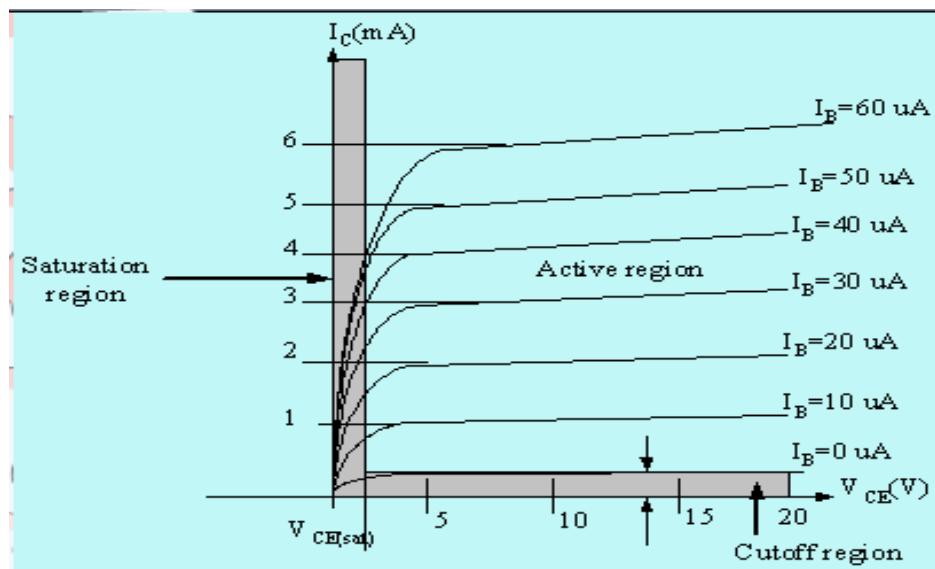


Fig 3.9b Output characteristics for common-emitter npn transistor

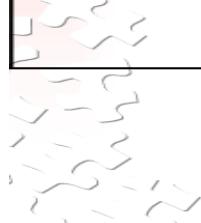
For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing of V_{CE}

$V_{CE} > V_{CESAT}$ I_C not totally depends on $V_{CE} \rightarrow$ constant I_C

I_B (uA) is very small compare to I_C (mA). Small increase in I_B cause big increase in I_C

$I_B=0$ A $\rightarrow I_{CEO}$ occur.

Noticing the value when $I_C=0$ A. There is still some value of current flows.

Active region	Saturation region	Cut-off region
<ul style="list-style-type: none"> B-E junction is forward bias C-B junction is reverse bias can be employed for voltage, current and power amplification 	<ul style="list-style-type: none"> B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. The value of V_{CE} is so small. Suitable region when the transistor as a logic switch. NOT and avoid this region when the transistor as an amplifier. 	<ul style="list-style-type: none"> region below $I_B=0\mu A$ is to be avoided if an undistorted o/p signal is required B-E junction and C-B junction is reverse bias $I_B=0$, I_C not zero, during this condition $I_C=I_{CEO}$ where is this current flow when B-E is reverse bias.

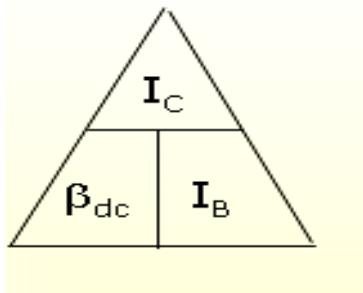


Beta (β) or amplification factor

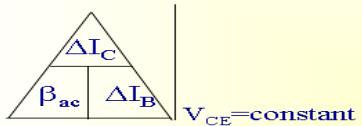
The ratio of dc collector current (I_C) to the dc base current (I_B) is dc beta (β_{dc}) which is dc current gain where I_C and I_B are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation:

$$30 < \beta_{dc} < 300 \rightarrow 2N3904$$

On data sheet, $\beta_{dc}=hfe$ with h is derived from ac hybrid equivalent cct. FE are derived from forward-current amplification and common-emitter configuration respectively.



For ac conditions, an ac beta has been defined as the changes of collector current (I_C) compared to the changes of base current (I_B) where I_C and I_B are determined at operating point. On data sheet, $\beta_{ac} = hfe$. It can be defined by the following equation:

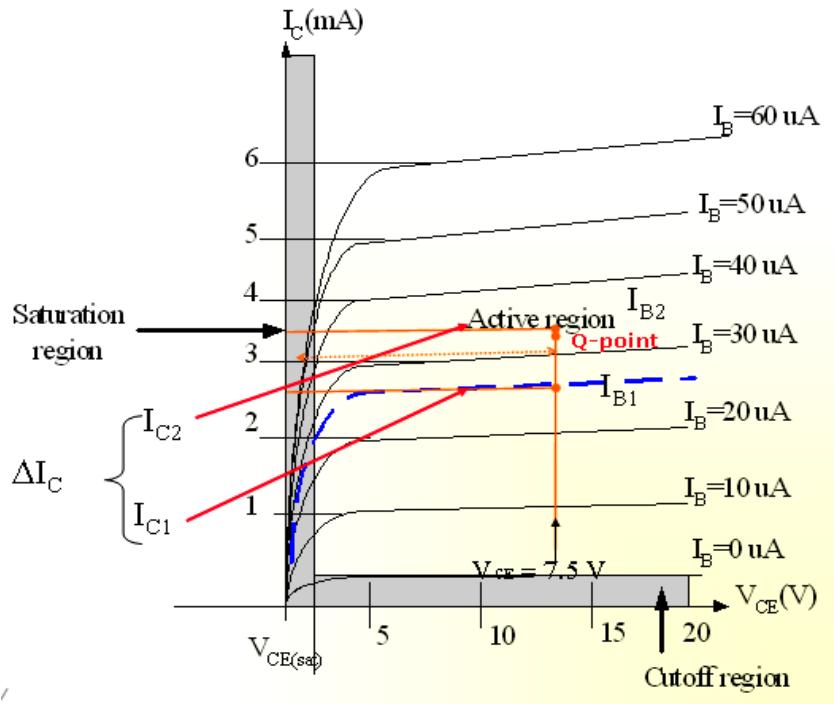


From output characteristics of common emitter configuration, find β_{ac} and β_{dc} with an

Operating point at $I_B = 25 \mu A$ and $V_{CE} = 7.5V$

$$\begin{aligned}\beta_{ac} &= \frac{\Delta I_C}{\Delta I_B} \Big| V_{CE} = \text{constant} \\ &= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2 \text{ mA} - 2.2 \text{ mA}}{30 \mu A - 20 \mu A} \\ &= \frac{1 \text{ mA}}{10 \mu A} = 100\end{aligned}$$

$$\begin{aligned}\beta_{dc} &= \frac{I_C}{I_B} \\ &= \frac{2.7 \text{ mA}}{25 \mu A} \\ &= \underline{\underline{108}}\end{aligned}$$



Relationship analysis between α and β

CASE 1

$$I_E = I_C + I_B \quad (1)$$

substitute equ. $I_C = \beta I_B$ into (1) we get

$$\underline{I_E = (\beta + 1)I_B}$$

CASE 2

$$\text{known} : \alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha} \quad (2)$$

$$\text{known} : \beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta} \quad (3)$$

substitute (2) and (3) into (1) we get,

$$\underline{\underline{\alpha = \frac{\beta}{\beta + 1}}} \quad \text{and} \quad \underline{\underline{\beta = \frac{\alpha}{1 - \alpha}}}$$

3.7 COMMON – COLLECTOR CONFIGURATION

Also called emitter-follower (EF). It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point. The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is

similar with common-emitter configuration. Common-collector circuit configuration is provided with the load resistor connected from emitter to ground. It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.

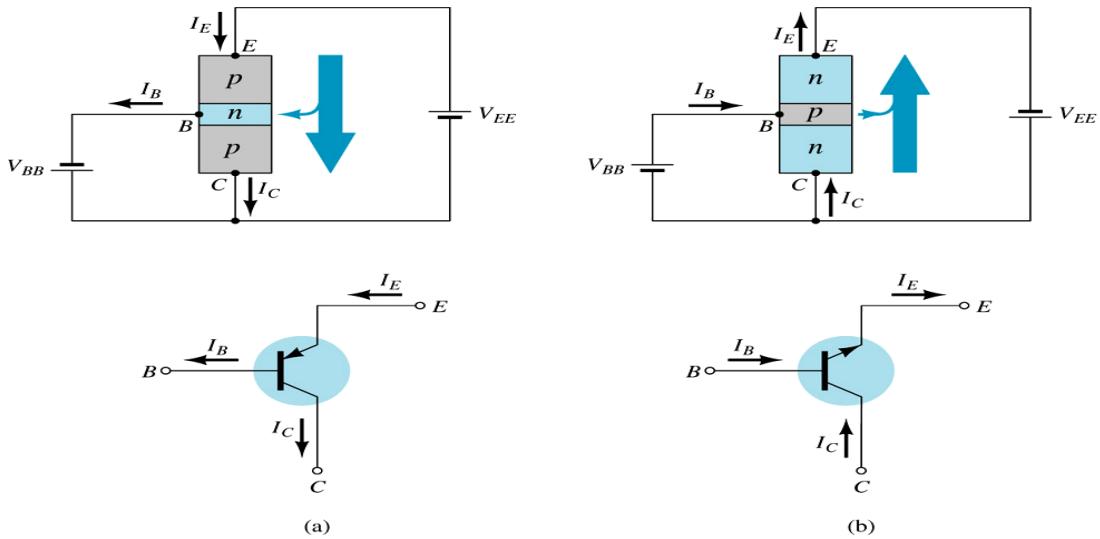


Fig 3.10 CC Configuration

For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range

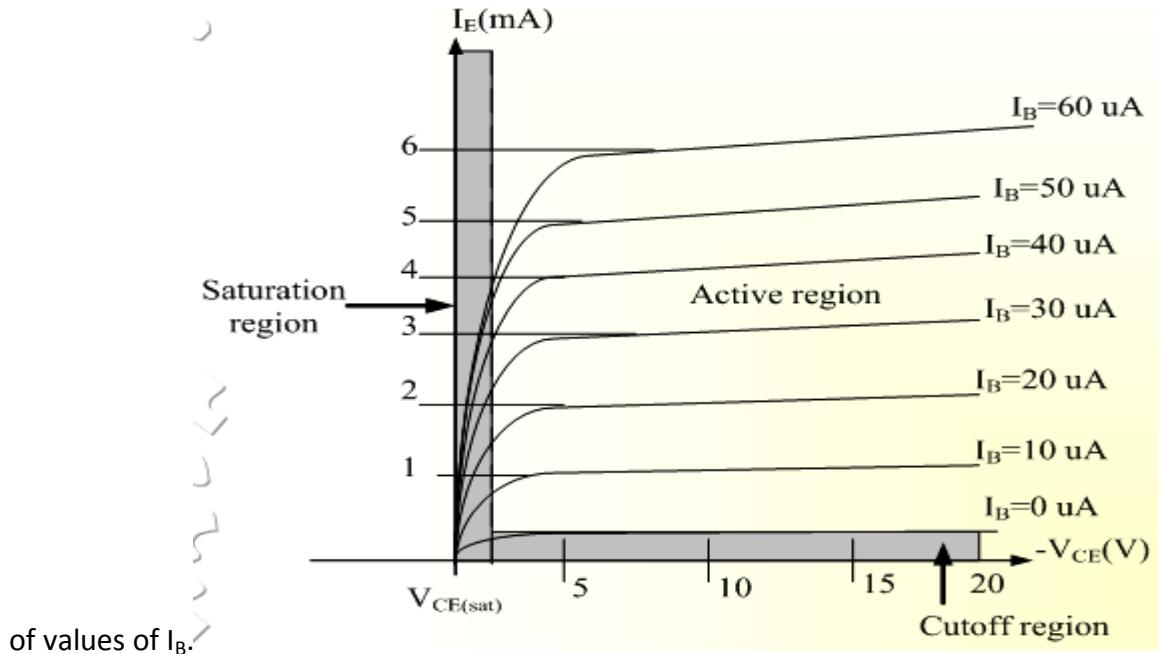


Fig 3.11 Output Characteristics of CC Configuration for npn Transistor

Limits of operation

Many BJT transistor used as an amplifier. Thus it is important to notice the limits of operations. At least 3 maximum values is mentioned in data sheet.

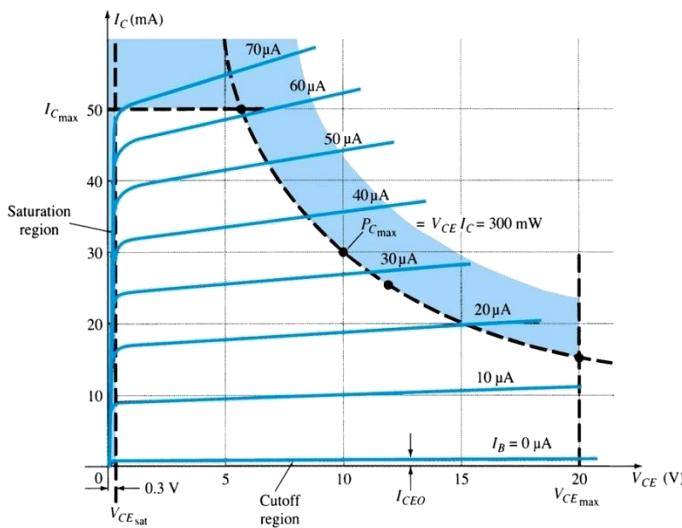
There are:

- a) Maximum power dissipation at collector: P_{Cmax} or P_D
- b) Maximum collector-emitter voltage: V_{CEmax} sometimes named as $V_{BR(CEO)}$ or V_{CEO} .
- c) Maximum collector current: I_{Cmax}

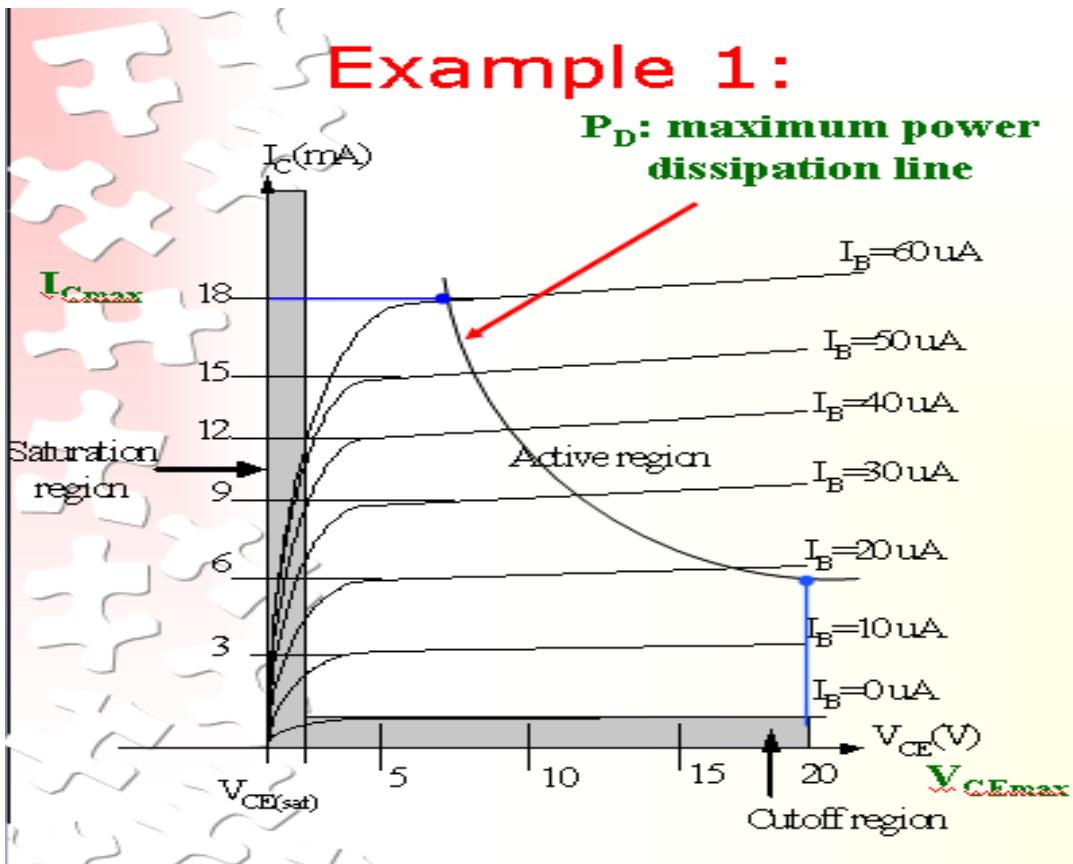
There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are:
transistor need to be operate in active region!

$$I_C < I_{Cmax}$$

$$P_C < P_{Cmax}$$



Note: V_{CE} is at maximum and I_C is at minimum ($I_{Cmax}=I_{CEO}$) in the cutoff region. I_C is at maximum and V_{CE} is at minimum ($V_{CE max} = V_{cesat} = V_{CEO}$) in the saturation region. The transistor operates in the active region between saturation and cutoff.



Refer to the fig. Example; A derating factor of $2\text{mW}/^{\circ}\text{C}$ indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

Step 1:

The maximum collector power dissipation,

$$P_D = I_{C\text{MAX}} \times V_{CE\text{max}} = 18\text{mA} \times 20\text{V} = 360\text{mW}$$

Step 2:

At any point on the characteristics the product of and must be equal to 360mW .

Ex. 1. If choose $I_{C\text{max}} = 5\text{ mA}$, substitute into the (1), we get

$$V_{CE\text{max}} I_{C\text{max}} = 360\text{mW}$$

$$V_{CE\text{max}}(5\text{ m}) = 360/5 = \underline{7.2\text{ V}}$$

Ex.2. If choose $V_{CEmax}=18$ V, substitute into (1), we get

$$V_{CEmax}I_{Cmax} = 360 \text{ mW}$$

$$(10) I_{CMAX}=360m/18=20 \text{ mA}$$

Derating P_{Dmax}

P_{DMAX} is usually specified at 25°C.

The higher temperature goes, the less is P_{DMAX}

Example; A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

BJT HYBRID MODEL

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

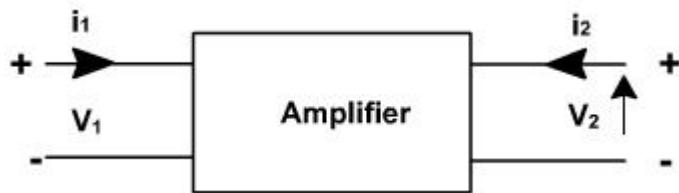


Fig. 1

A two-port network is represented by four external variables: voltage V_1 and current i_1 at the input port, and voltage V_2 and current i_2 at the output port, so that the two-port network can be treated as a black box modeled by the relationships between the four variables, V_1, V_2, i_1, i_2 . Out of four variables two can be selected as are independent variables and two are dependent variables. The dependent variables can be expressed in terms of independent variables. This leads to various two port parameters out of which the following three are important:

1. Impedance parameters (z-parameters)
2. Admittance parameters (y-parameters)
3. Hybrid parameters (h-parameters)

z-parameters

A two-port network can be described by z-parameters as

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Where

$$z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0}$$

Input impedance with output port open circuited

$$z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0}$$

Reverse transfer impedance with input port open circuited

$$z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0}$$

Forward transfer impedance with output port open circuited

$$z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0}$$

Output impedance with input port open circuited

Y-parameters

A two-port network can be described by Y-parameters as

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0}$$

Input admittance with output port short circuited

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0}$$

Reverse transfer admittance with input port short circuited

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0}$$

Forward transfer admittance with output port short circuited

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$$

Output admittance with input port short circuited

Hybrid parameters (h-parameters)

If the input current I1 and output voltage V2 are taken as independent variables, the dependent variables V1 and I2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where $h_{11}, h_{12}, h_{21}, h_{22}$ are called as hybrid parameters.

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$$

Input impedance with o/p port short circuited

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$

output impedance with i/p port open circuited

THE HYBRID MODEL FOR TWO PORT NETWORK:

Based on the definition of hybrid parameters the mathematical model for two port networks known as h-parameter model can be developed. The hybrid equations can be written as:

$$V_1 = h_i I_1 + h_r V_2$$

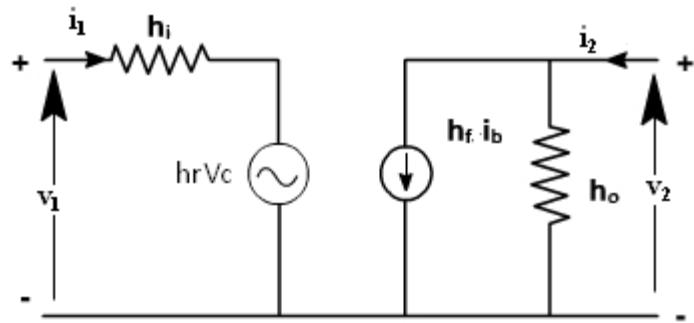
$$I_2 = h_f I_1 + h_o V_2$$

(The following convenient alternative subscript notation is recommended by the **IEEE Standards**:

i=11= input o = 22 = output

f=21 = forward transfer r = 12 = reverse transfer)

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff's voltage and current laws for input and output ports.



If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. h_{fe} , h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in fig. 2.

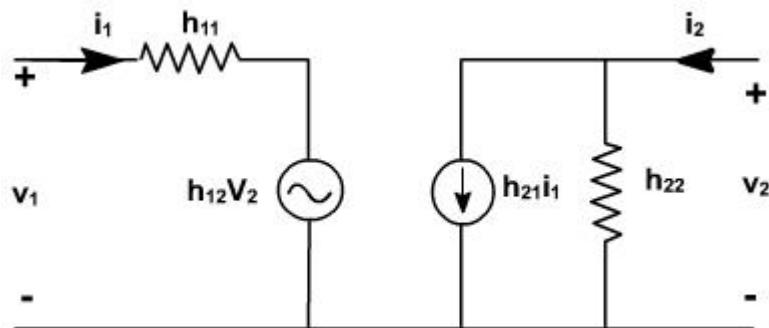


Fig. 2

TRANSISTOR HYBRID MODEL:

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in fig. 3. The variables, i_B , i_C , v_C , and v_B represent total instantaneous currents and voltages i_B and v_C can be taken as independent variables and v_B , i_C as dependent variables.

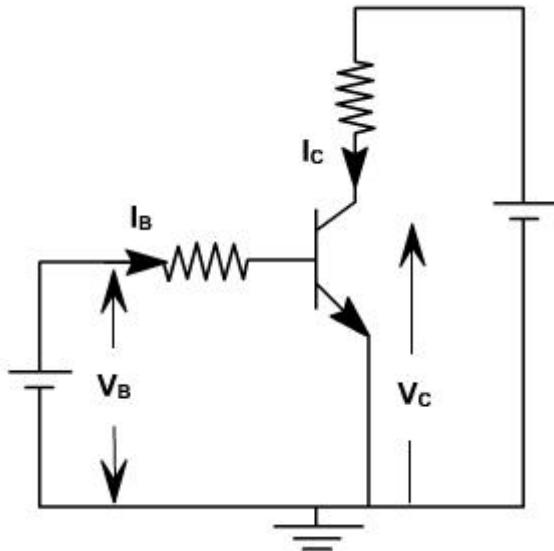


Fig. 3

$$V_B = f_1(i_B, v_C)$$

$$I_C = f_2(i_B, v_C).$$

Using Taylor's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \frac{\partial f_1}{\partial i_B} \Big|_{v_C} \Delta i_B + \frac{\partial f_1}{\partial v_C} \Big|_{i_B} \Delta v_C$$

$$\Delta i_C = \frac{\partial f_2}{\partial i_B} \Big|_{v_C} \Delta i_B + \frac{\partial f_2}{\partial v_C} \Big|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δv_B , Δv_C , Δi_B , Δi_C represent the small signal (incremental) base and collector current and voltage and can be represented as v_B , i_C , i_B , v_C

$$\therefore v_B = h_{ie} i_B + h_{re} v_C$$

$$i_C = h_{fe} i_B + h_{oe} v_B$$

where

$$h_{ie} = \frac{\partial f_1}{\partial i_B} \Big|_{v_C} = \frac{\partial v_B}{\partial i_B} \Big|_{v_C}; \quad h_{re} = \frac{\partial f_1}{\partial v_C} \Big|_{i_B} = \frac{\partial v_B}{\partial v_C} \Big|_{i_B}$$

$$h_{fe} = \frac{\partial f_2}{\partial i_B} \Big|_{v_C} = \frac{\partial i_C}{\partial i_B} \Big|_{v_C}; \quad h_{oe} = \frac{\partial f_2}{\partial v_C} \Big|_{i_B} = \frac{\partial i_C}{\partial v_C} \Big|_{i_B}$$

The model for CE configuration is shown in fig. 4.

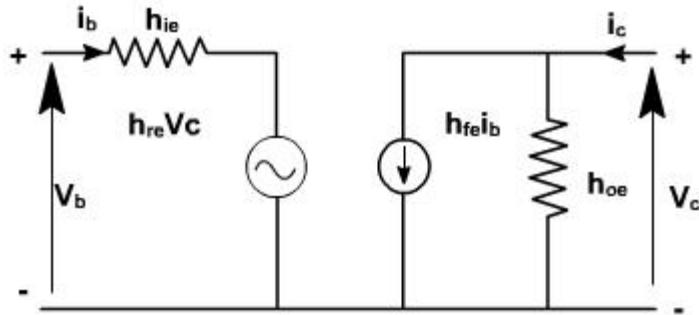


Fig. 4

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. Fig. 5, shows the output characteristics of CE amplifier.

$$h_{fe} = \left. \frac{\partial i_C}{\partial i_B} \right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}}$$

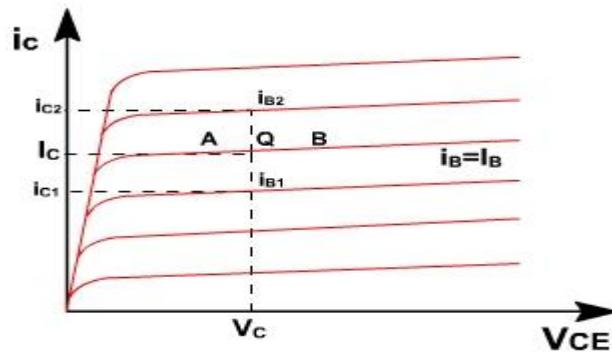


Fig. 5

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left. \frac{\partial i_C}{\partial V_C} \right|_{i_B}$$

The value of h_{oe} at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \left. \frac{\partial V_B}{\partial i_B} \right|_{V_C} \approx \left. \frac{\Delta V_B}{\Delta i_B} \right|_{V_C}$$

h_{ie} is the slope of the appropriate input on [fig. 6](#), at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left. \frac{\Delta V_B}{\Delta V_C} \right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

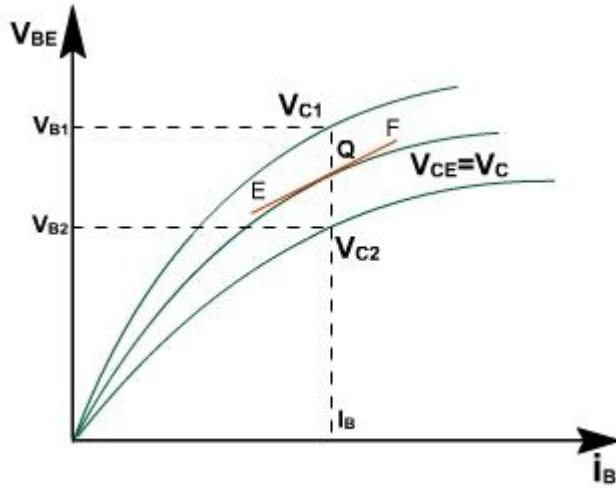


Fig. 6

A vertical line on the input characteristic represents constant base current. The parameter h_{re} can be obtained from the ratio $(V_{B2} - V_{B1})$ and $(V_{C2} - V_{C1})$ for at Q.

Typical CE h-parameters of transistor 2N1573 are given below:

$$h_{ie} = 1000 \text{ ohm.}$$

$$h_{re} = 2.5 * 10^{-4}$$

$$h_{fe} = 50$$

$$h_{oe} = 25 \text{ } \mu \text{A/V}$$

ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in [fig. 1](#) and to bias the transistor properly.

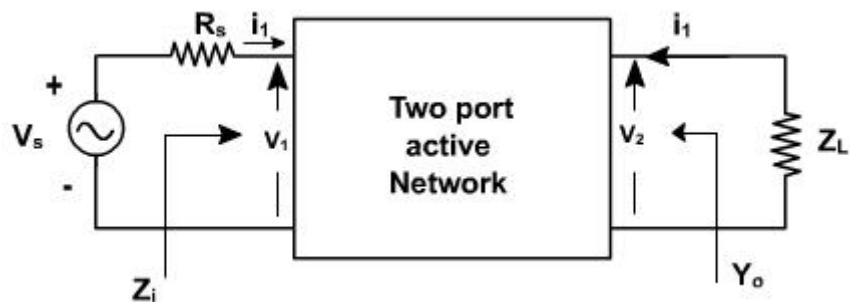
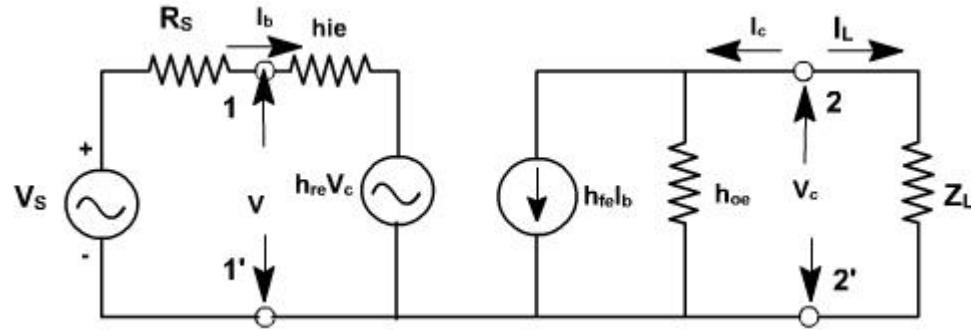


Fig. 1

Consider the two-port network of CE amplifier. R_s is the source resistance and Z_L is the load impedance. h -parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in fig. 2. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedance, voltage gain, and output impedance.



Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

Input impedance:

The impedance looking into the amplifier input terminals ($1, 1'$) is the input impedance Z_i .

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\begin{aligned} \frac{V_b}{I_b} &= h_{ie} + h_{re} \frac{V_c}{I_b} \\ &= h_{ie} - \frac{h_{re} I_c Z_L}{I_b} \end{aligned}$$

$$\therefore Z_i = h_{ie} + h_{re} A_i Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{\gamma_L + h_{oe}} \quad (\text{since } \gamma_L = \frac{1}{Z_L})$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_c}{V_b} = -\frac{I_c Z_L}{V_b}$$

$$\therefore A_v = \frac{I_b A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance:

$$Y_0 = \left. \frac{I_c}{V_c} \right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe} \frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $R_s \cdot I_b + h_{ie} \cdot I_b + h_{re} V_c = 0$.

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_s) is given by

$$A_{Vs} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_s} \quad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i \right)$$

$$= A_v \cdot \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i Z_L}{Z_i + R_s}$$

It is defined as

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source I_s in parallel with a resistance R_s as shown in fig. 3.

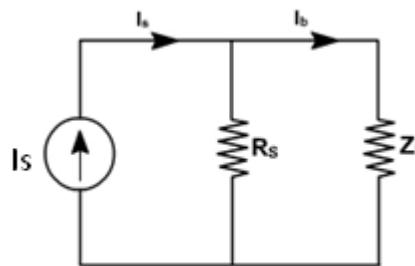


Fig. 3

In this case, overall current gain A_{IS} is defined as

$$\begin{aligned}
 A_{I_s} &= \frac{I_L}{I_s} \\
 &= -\frac{I_c}{I_s} \\
 &= -\frac{I_c * I_b}{I_b * I_s} \quad \left(I_b = \frac{I_s * R_s}{R_s + Z_i} \right) \\
 &= A_I * \frac{R_s}{R_s + Z_i}
 \end{aligned}$$

If $R_s \rightarrow \infty$, $A_{I_s} \rightarrow A_I$

h-parameters

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example [fig. 4](#) hrc in terms of CE parameter can be obtained as follows.

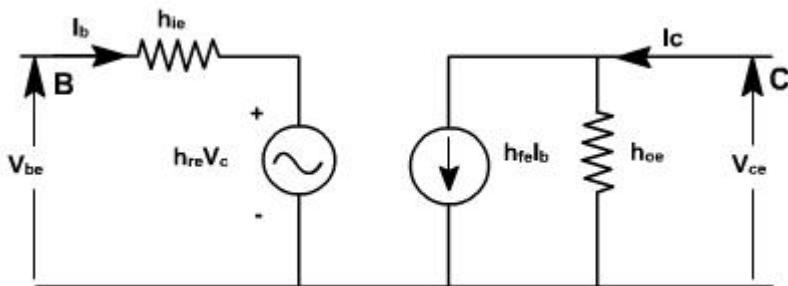


Fig. 4

For CE transistor configuration

$$V_{be} = h_{ie} I_b + h_{re} V_{ce}$$

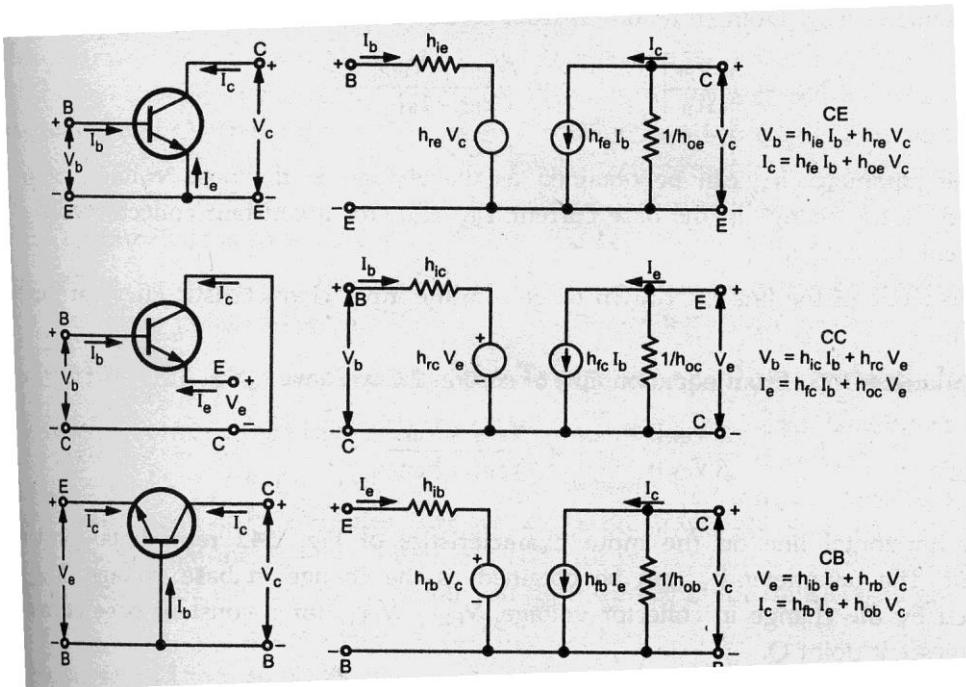
$$I_c = h_{fe} I_b + h_{oe} V_{ce}$$

The circuit can be redrawn like CC transistor configuration as shown in [fig. 5](#).

$$V_{bc} = h_{ie} I_b + h_{rc} V_{ce}$$

$$I_c = h_{fe} I_b + h_{oc} V_{ce}$$

hybrid model for transistor in three different configurations



Typical h-parameter values for a transistor

Parameter	CE	CC	CB
h_i	1100Ω	1100Ω	22Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51	-0.98
h_o	$25 \mu\text{A/V}$	$25 \mu\text{A/V}$	$0.49 \mu\text{A/V}$

Analysis of a Transistor amplifier circuit using h-parameters

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

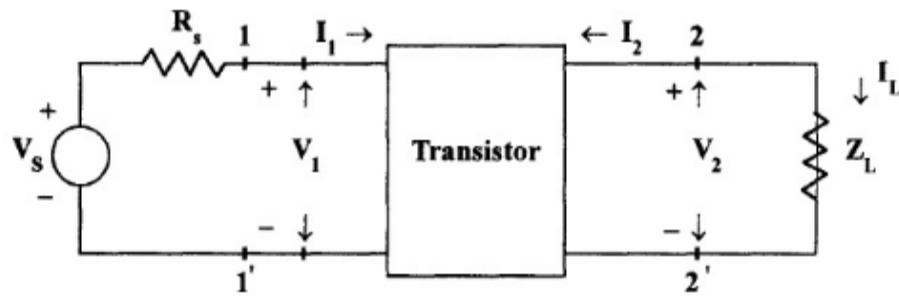


Fig.1.4 Basic Amplifier Circuit

The two port network of Fig. 1.4 represents a transistor in any one of its configuration. It is assumed that h-parameters remain constant over the operating range. The input is sinusoidal and I_1, V_1, I_2 and V_2 are phase quantities

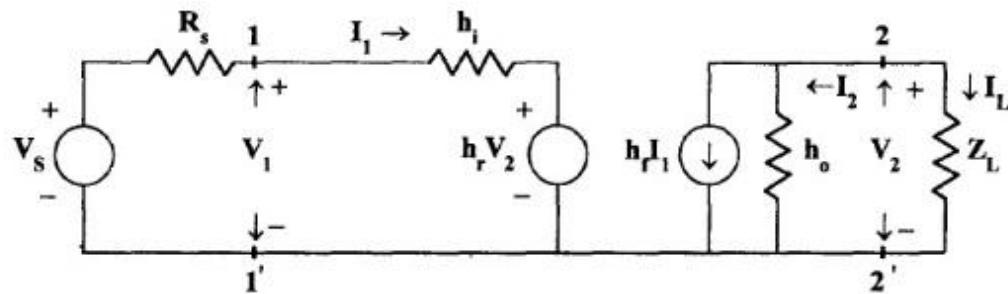


Fig. 1.5 Transistor replaced by its Hybrid Model

Current Gain or Current Amplification (A_i)

For transistor amplifier the current gain A_i is defined as the ratio of output current to input current, i.e,

$$A_i = I_L / I_1 = -I_2 / I_1$$

From the circuit of Fig

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2(1 + Z_L h_o) = h_f I_1$$

$$A_i = -I_2 / I_1 = -h_f / (1 + Z_L h_o)$$

Therefore,

$$A_i = -h_f / (1 + Z_L h_o)$$

Input Impedance (Z_i)

In the circuit of Fig , R_s is the signal source resistance .The impedance seen when looking into the amplifier terminals (1,1') is the amplifier input impedance Z_i ,

$$Z_i = V_1 / I_1$$

From the input circuit of Fig $V_1 = h_i I_1 + h_r V_2$

$$Z_i = (h_i I_1 + h_r V_2) / I_1$$

$$= h_i + h_r V_2 / I_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$Z_i = h_i + h_r A_1 I_1 Z_L / I_1$$

$$= h_i + h_r A_1 Z_L$$

Substituting for A_i

$$Z_i = h_i - h_f h_r Z_L / (1 + h_o Z_L)$$

$$= h_i - h_f h_r Z_L / Z_L (1/Z_L + h_o)$$

Taking the Load admittance as $Y_L = 1/Z_L$

$$Z_i = h_i - h_f h_r / (Y_L + h_o)$$

Voltage Gain or Voltage Gain Amplification Factor(A_v)

The ratio of output voltage V_2 to input voltage V_1 give the voltage gain of the transistor i.e,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$A_v = A_1 I_1 Z_L / V_1 = A_i Z_L / Z_i$$

Output Admittance (Y_o)

Y_o is obtained by setting V_s to zero, Z_L to infinity and by driving the output terminals from a generator V_2 . If the current V_2 is I_2 then $Y_o = I_2 / V_2$ with $V_s = 0$ and $R_L = \infty$.

From the circuit of fig

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by V_2 ,

$$I_2 / V_2 = h_f I_1 / V_2 + h_o$$

With $V_2 = 0$, by KVL in input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$(R_s + h_i) I_1 + h_r V_2 = 0$$

$$\text{Hence, } I_2 / V_2 = -h_r / (R_s + h_i)$$

$$= h_f (-h_r / (R_s + h_i)) + h_o$$

$$Y_o = h_o - h_f h_r / (R_s + h_i)$$

The output admittance is a function of source resistance. If the source impedance is resistive then Y_o is real.

Voltage Amplification Factor(A_{vs}) taking into account the resistance (R_s) of the source

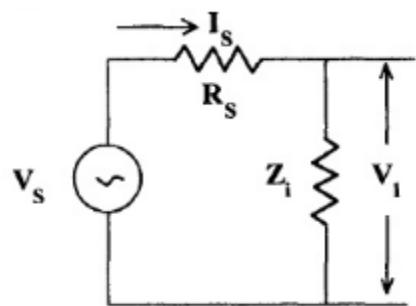


Fig. 5.6 Thevenin's Equivalent Input Circuit

This overall voltage gain A_{vs} is given by

$$A_{vs} = V_2 / V_s = V_2 V_1 / V_1 V_s = A_v V_1 / V_s$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 5.6

$$V_1 = V_s Z_i / (Z_i + R_s)$$

$$V_1 / V_s = Z_i / (Z_i + R_s)$$

$$\text{Then, } A_{vs} = A_v Z_i / (Z_i + R_s)$$

$$\text{Substituting } A_v = A_i Z_L / Z_i$$

$$A_{vs} = A_i Z_L / (Z_i + R_s)$$

$$A_{vs} = A_i Z_L R_s / (Z_i + R_s) R_s$$

$$A_{vs} = A_{is} Z_L / R_s$$

Current Amplification (A_{is}) taking into account the source Resistance(R_s)

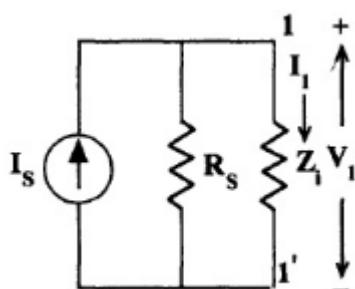


Fig. 1.7 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of A_{is} is shown in Fig. 1.7

$$\text{Overall Current Gain, } A_{is} = -I_2 / I_S = -I_2 I_1 / I_1 I_S = A_i I_1 / I_S$$

$$\text{From Fig. 1.7} \quad I_1 = I_S R_S / (R_S + Z_i)$$

$$I_1 / I_S = R_S / (R_S + Z_i)$$

$$\text{and hence, } A_{is} = A_i R_S / (R_S + Z_i)$$

Operating Power Gain (A_p)

The operating power gain A_p of the transistor is defined as

$$A_p = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i$$

$$A_p = A_i^2 (Z_L / Z_i)$$

Small Signal analysis of a transistor amplifier

$A_i = -h_f / (1 + Z_L h_o)$	$A_v = A_i Z_L / Z_i$
$Z_i = h_i + h_r A_i Z_L = h_i - h_f h_r / (Y_L + h_o)$	$A_{vs} = A_v Z_i / (Z_i + R_S) = A_i Z_L / (Z_i + R_S)$ $= A_{is} Z_L / R_S$
$Y_o = h_o - h_f h_r / (R_S + h_i) = 1 / Z_o$	$A_{is} = A_i R_S / (R_S + Z_i) = A_{vs} = A_{is} R_S / Z_L$