UNIT 5

FIELD EFFECT TRANSISTOR

5.1 INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

5.2 CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

1. Junction Field Effect Transistors

2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.

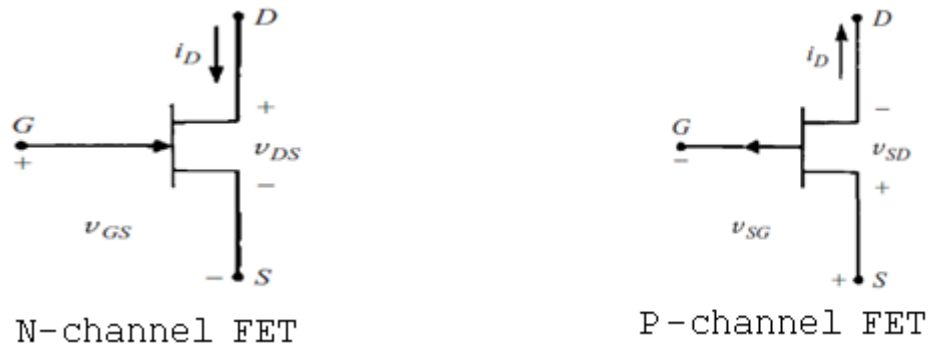


Fig 5.1 schematic symbols for the P-channel and N-channel JFET

5.3 CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET

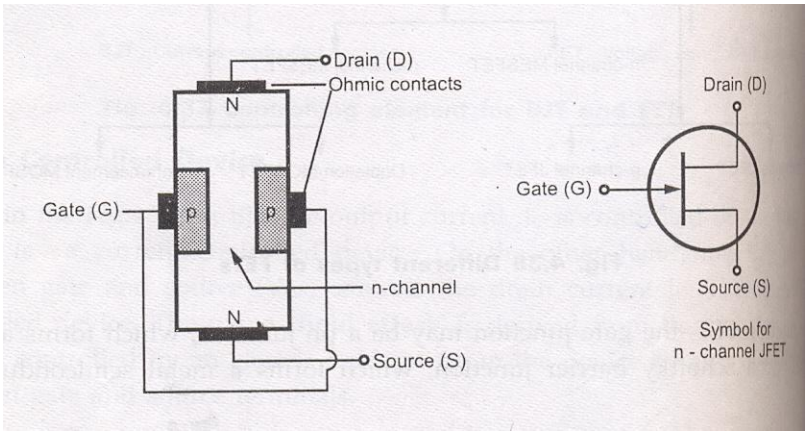


Fig 5.2 Construction of N-Channel JFET

A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source. And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

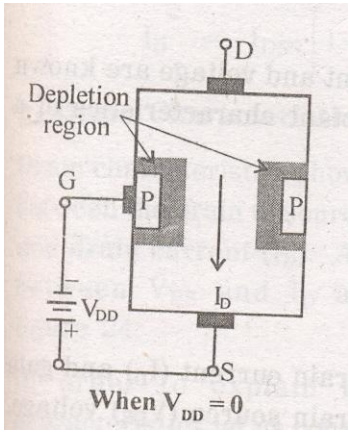
A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut off completely.

There are two ways to control the channel width

1. By varying the value of Vgs
2. And by Varying the value of Vds holding Vgs constant

1 By varying the value of Vgs :-

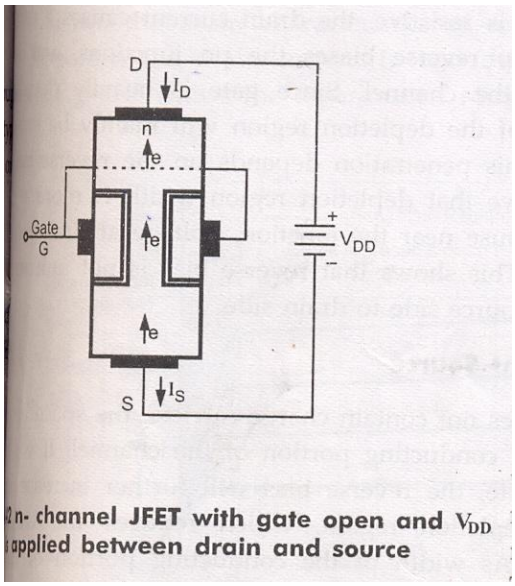
We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage Vgs connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



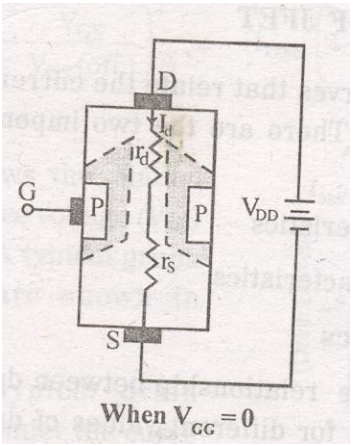
1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.
2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
6) By varying the value of Vgs we can vary the width of the channel.

2 Varying the value of Vds holding Vgs constant :-

1) When no voltage is applied to the gate i.e. Vgs=0 , Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current Id .
2) With Vgs= 0 for Id= 0 the channel between the gate junctions is entirely open .In response to a small applied voltage Vds , the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds .
3) The channel resistances are represented as rd and rs as shown in the fig.



n- channel JFET with gate open and V_{DD} applied between drain and source



4) This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction,(rd> rs) .Thus the depletion region is formed which is not symmetrical .

5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because Vrd >> Vrs. So reverse bias is higher near drain than at source.
6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off. This is the voltage where the current Id begins to level off and approach a constant value.

7) So, by varying the value of Vds we can vary the width of the channel holding Vgs constant.

When both Vgs and Vds is applied:-

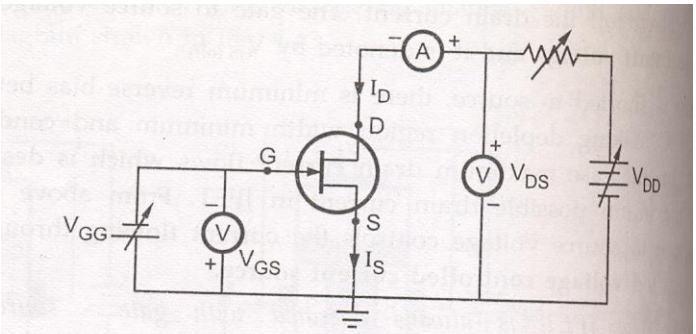
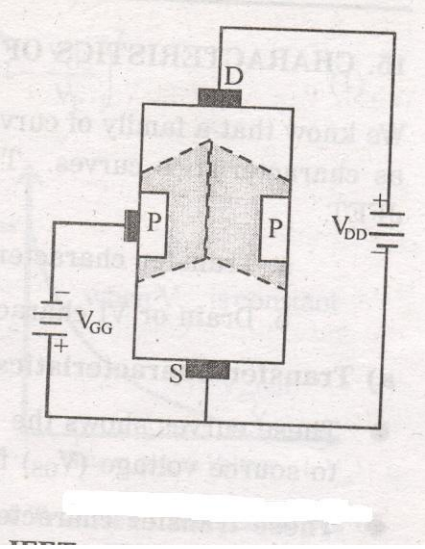


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current Id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

1) When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current Id, its conventional direction is from drain to source.
2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by Idss.



3) When Vgs is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
4) When Vgs is further increased a stage is reached at which to depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

5.4 CHARACTERISTICS OF N-CHANNEL JFET

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

1) Drain or VI Characteristics
2) Transfer characteristics

1. **Drain Characteristics:-**
2. Drain characteristics shows the relation between the drain to source voltage Vds and drain current Id. In order to explain typical drain characteristics let us consider the curve with Vgs= 0.V.

1) When Vds is applied and it is increasing the drain current ID also increases linearly up to knee point.
2) This shows that FET behaves like an ordinary resistor.This region is called as ohmic region.
3) ID increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

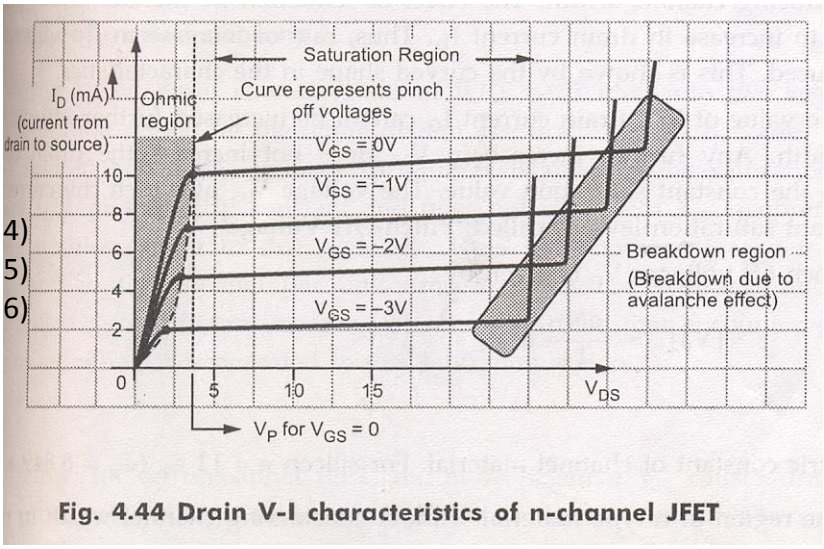


Fig. 4.44 Drain V-I characteristics of n-channel JFET

4)
5)
6)

4) It is because of the fact that there is an increase in VDS .This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of the channel.

5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.

5) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(Vp).

PINCH OFF Region:-

1) This is the region shown by the curve as saturation region.
2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region , the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
3) In this drain current remains constant at its maximum value IDSS.

4) The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{dss} [1-V_{gs/Vp}]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
2) It is because of the gate to source junction due to avalanche effect.

3) The avalanche break down occurs at progressively lower value of VDS because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction
This causes

1. The maximum saturation drain current is smaller
2. The ohmic region portion decreased.

4) It is important to note that the maximum voltage VDS which can be applied to FET is the lowest voltage which causes available break down.

3. TRANSFER CHARACTERISTICS:-

These curves shows the relationship between drain current ID and gate to source voltage VGS for different values of VDS.

1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.
2) Plot the graph between gate to source voltage along the horizontal axis and current ID on the vertical axis. We shall obtain a curve like this.

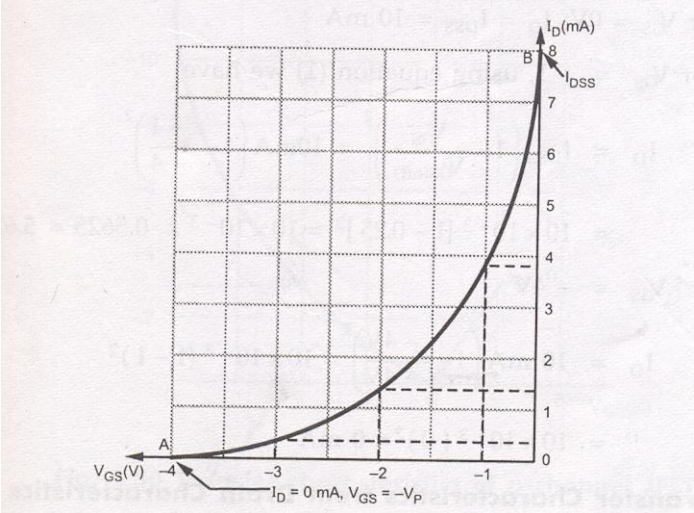


Fig. 4.48 Transfer characteristics of n-channel JFET

3) As we know that if V_{gs} is more negative curves drain current to reduce . where V_{gs} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{gs} at the cutoff point is designed as V_{gsoff}

4) The upper end of the curve as shown by the drain current value is equal to I_{dss} that is when V_{gs} = 0 the drain current is maximum.

5) While the lower end is indicated by a voltage equal to V_{gsoff}
6) If Vg_s continuously increasing , the channel width is reduced , then I_d =0
7) It may be noted that curve is part of the parabola; it may be expressed as

$I_d=I_{dss}[1-V_{gs}/V_{gsoff}]^2$

DIFFERENCE BETWEEN V_p AND V_{gsoff} –

Vp is the value of V_{gs} that causes the JFET to become constant current component, It is measured at V_{gs} =0V and has a constant drain current of I_d =I_{dss} .Where V_{gsoff} is the value of V_{gs} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET 's have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

5.5 JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region.It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage $V_{gs.}$

Mathematically it is expressed as $r_d=\Delta V_{ds}/ \Delta I_d$ where V_{gs} is held constant.

TRANCE CONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{ds})

Mathematically the transconductance can be written as

$$g_m=\Delta I_{d/}\Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu=\Delta V_{ds}/\Delta V_{gs}$ when I_d held constant

The amplification factor μ may be expressed as a product of transconductance (g_m)and ac drain resistance (r_d)

$\mu=\Delta V_{ds}/\Delta V_{gs}=g_m\, r_d$

5.5 THE FET SMALL SIGNAL MODEL

The linear small signal equivalent circuit for the FET can be obtained in a manner similar to that used to derive the corresponding model for a transistor.

We can express the drain current iD as a function f of the gate voltage and drain voltage V_{ds}.

$I_d=f(V_{gs},V_{ds})$----------(1)

The transconductance g_m and drain resistance r_d:-

If both gate voltage and drain voltage are varied, the change in the drain current is approximated by using taylors series considering only the first two terms in the expansion

$$\Delta i_d=\frac{\partial id}{\partial Vgs}|v_{ds}=\text{constant}\ .\Delta v_{gs}+\frac{\partial id}{\partial Vds}|vgs=\text{constant}\Delta v_{ds}$$

we can write $\Delta i_d=i_d$

$\Delta v_{gs}=v_{gs}$

$\Delta v_{ds}=v_{ds}$

$$I_d=g_m\, vgs\ +\frac{1}{rd}\ Vds\rightarrow(1)$$

Where $g_m=\frac{\partial id}{\partial Vgs}|Vds\cong\frac{\Delta id}{\Delta Vgs}|Vds$

$$g_m=\frac{id}{Vgs}|Vds$$

Is the mutual conductance or transconductance .It is also called as gfs or yfs common source forward conductance .

The second parameter r_d is the drain resistance or output resistance is defined as

$$r_d=\frac{\partial Vds}{\partial id}|_{Vgs} \cong \frac{\Delta vds}{\Delta ids}|_{Vgs}=\frac{Vds}{id}|_{Vgs}$$

$$r_d=\frac{Vds}{id}|_{Vgs}$$

The reciprocal of the rd is the drain conductance gd .It is also designated by Yos and Gos and called the common source output conductance . So the small signal equivalent circuit for FET can be drawn in two different ways.

1.small signal current –source model

2.small signal voltage-source model.

A small signal current –source model for FET in common source configuration can be drawn satisfying Eq→(1) as shown in the figure(a)

This low frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate-to –source voltage. The proportionality factor is the transconductance 'g_m'. The output resistance is 'r_d'. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.

The small signal voltage-source model is shown in the figure(b).

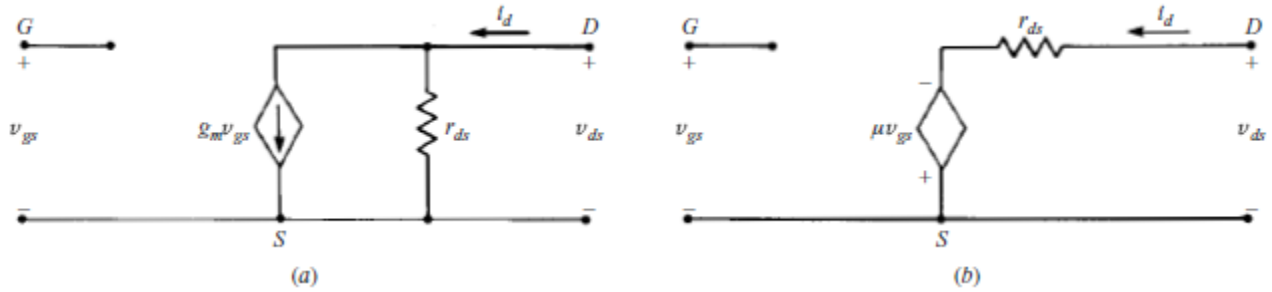
This can be derived by finding the Thevenin's equivalent for the output part of fig(a) .

These small signal models for FET can be used for analyzing the three basic FET amplifier configurations:

1.common source (CS) 2.common drain (CD) or source follower

3. common gate(CG).

(a)Small Signal Current source model for FET (b)Small Signal voltage source model for FET

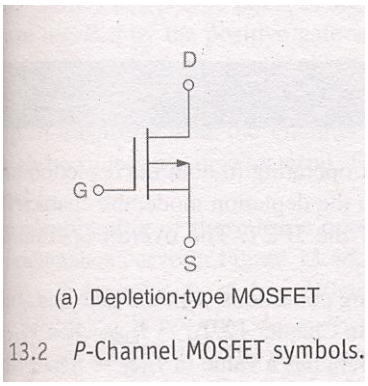


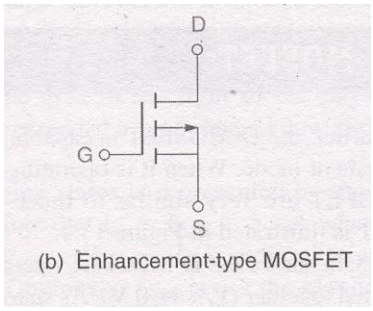
Here the input circuit is kept open because of having high input impedance and the output circuit satisfies the equation for ID

5.7 MOSFET

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.





(a) Depletion type MOSFET (b) Enhancement type MOSFET

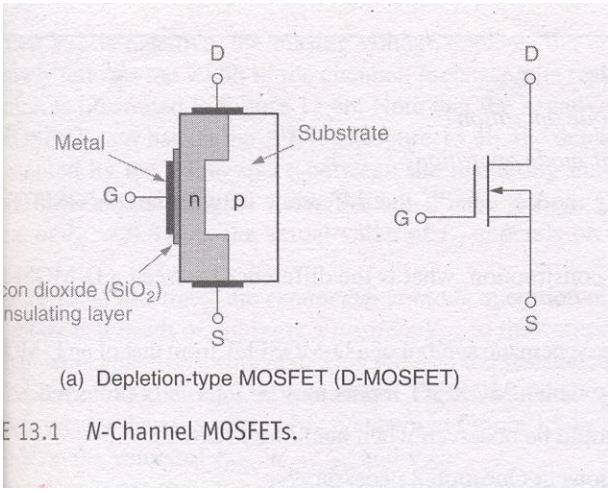
Both of them are P- channel

Here are two basic types of MOSFETS

(1) Depletion type (2) Enhancement type MOSFET.

D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

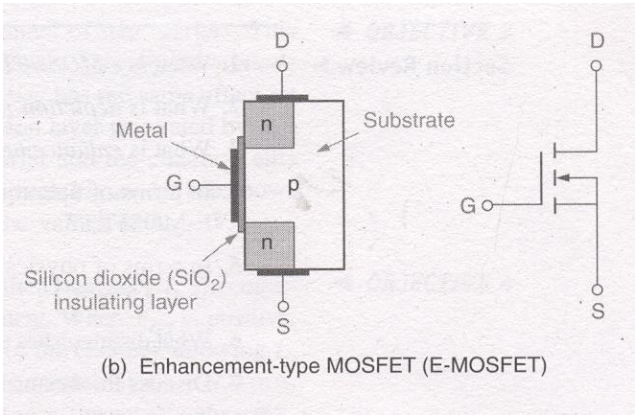
The construction difference between the two is shown in the fig given below.



(a) Depletion-type MOSFET (D-MOSFET)

E 13.1 *N*-Channel MOSFETs.

As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



(b) Enhancement-type MOSFET (E-MOSFET)

The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SIO_2 a glass like insulating material. The gate material is made up of

metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET or IGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channel device.

CONSTRUCTION OF AN N-CHANNEL MOSFET:-

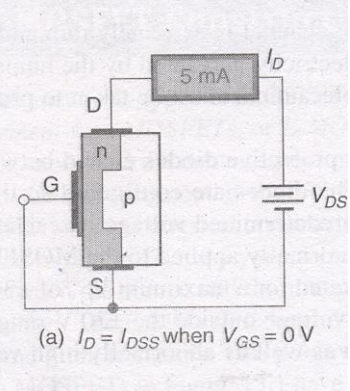
The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections , which will act as source and drain.

A thin layer of insulation silicon dioxide (SIO_2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region.Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of sio2

Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10 10 to 10power 15ohms) for MOSFET.

5.7.1 DEPLETION MOSFET

The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current IDSS flows foe zero gate to source voltage, Vgs=0.



Depletion mode operation:-

1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together(VGS=0V)

2) At this stage ID= IDSS where VGS=0V, with this voltage VDS, an appreciable drain current IDSS flows.

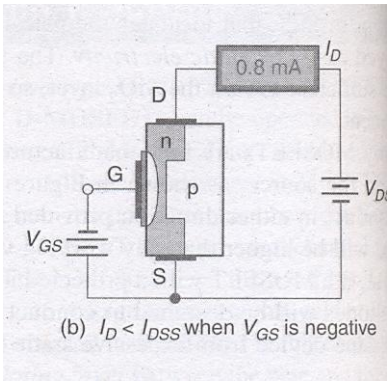
3) If the gate to source voltage is made negative i.e. VGs is negative .Positive charges are induced in the channel through the SIO2 of the gate capacitor.

4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as Vgs is made more negative.

5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.

6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.

7) Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.



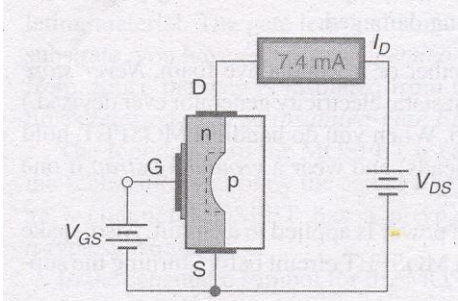
(b) $I_D < I_{DSS}$ when V_{GS} is negative

8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result ,Id<Idss.The actual value of ID depends on the value of Idss,Vgs(off) and Vgs.

Enhancement mode operation of the D-MOSFET:-

1) This operating mode is a result of applying a positive gate to source voltage Vgs to the device.
2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of IDSS
3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.

4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
5) With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N type material.
6) The extended n type channel now allows more current, Id> Idss



(c) $I_D > I_{DSS}$ when V_{GS} is positive

FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

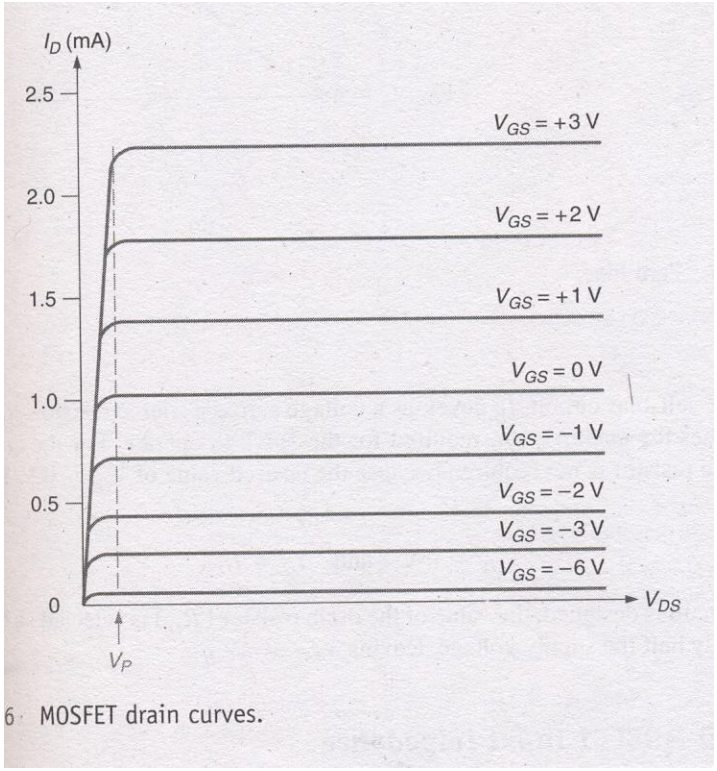
The fig. shows the drain characteristics for the N channel depletion type MOSFET

1) The curves are plotted for both Vgs positive and Vgs negative voltages
.
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive ,the MOSFET operates in the enhancement mode.
3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of Vgs.

4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increases linearly.

5) But as Vgs,0 induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. Id is constant.

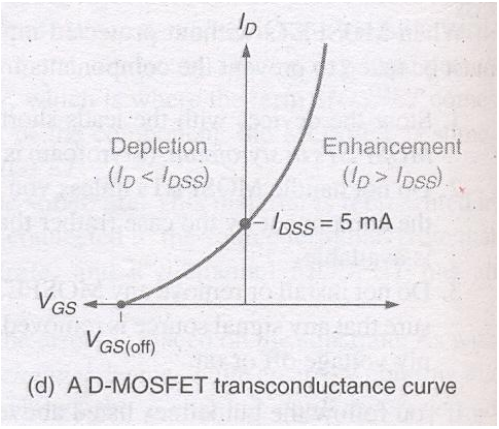
6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



6 MOSFET drain curves.

TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. Vgs=0V, VGs<0V, Vgs>0V is represented by the D MOSFET transconductance curve shown in Fig.



(d) A D-MOSFET transconductance curve

1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.

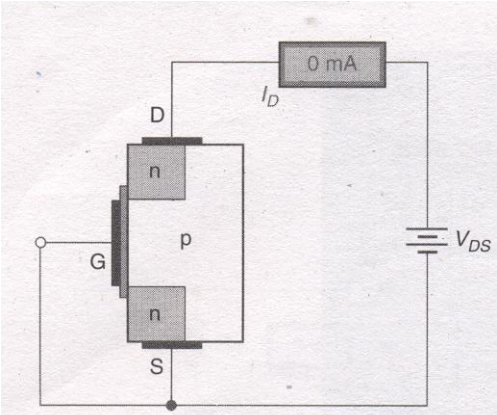
2) This curve extends for the positive values of Vgs

3) Note that Id=Idss for Vgs=0V when Vgs is negative,Id< Idss when Vgs= Vgs(off) ,Id is reduced to approximately omA.Where Vgs is positive Id>Idss.So obviously Idss is not the maximum possible value of Id for a MOSFET.

4) The curves are similar to JFET so thet the D MOSFET have the same transconductance equation.

5.7.2 E-MOSFETS

The E MOSFET is capable of operating only in the enhancement mode.The gate potential must be positive w.r.t to source.



(a) $I_D = 0$ mA when $V_{GS} = 0$ V

1) when the value of Vgs=0V, there is no channel connecting the source and drain materials.

2) As aresult , there can be no significant amount of drain current.

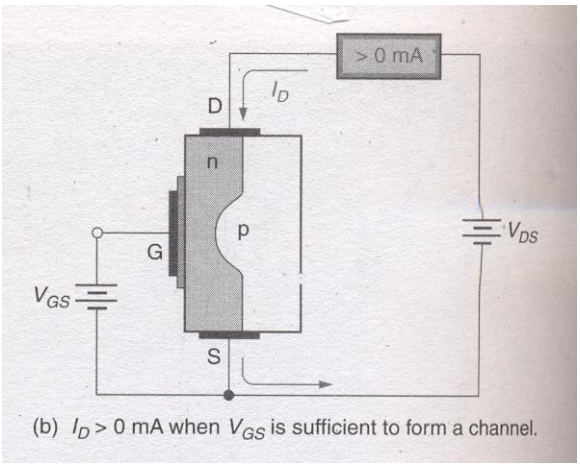
3) When Vgs=0, the Vdd supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current at Vgs=0,

4) If Vgs is positive, it induces a negative charge in the p type substrate just adjacent to the SIO2 layer.

5) As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providing a path for drain current.

6) This +ve gate voltage forma a channel between the source and drain.

7) This produces a thin layer of N type channel in the P type substarate.This layer of free electrons is called N type inversion layer.



(b) $I_D > 0$ mA when V_{GS} is sufficient to form a channel.

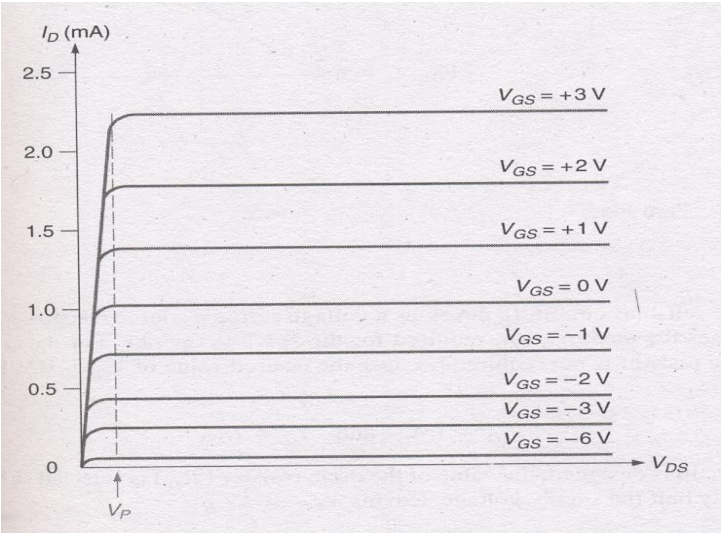
8) The minimum Vgs which produces this inversion layer is called threshold voltage and is designated by Vgs(th).This is the point at which the device turns on is called the threshold voltage Vgs(th)
9) When the voltage Vgs is <Vgs (th) no current flows from drain to source.

10) How ever when the voltage Vgs > Vgs (th) the inversion layer connects the drain to source and we get significant values of current.

CHARACTERISTICS OF E MOSFET:-

1. **DRAIN CHARACTERISTICS**

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the fig.



6 MOSFET drain curves.

2. TRANSFER CHARACTERISTICS:-

1) The current Idss at Vgs≤ 0 is very small beinf of the order of a few nano amps.
2) As Vgs is made +ve , the current Id increases slowly at forst, and then much more rapidly with an increase in Vgs.
3) The standard transconductance formula will not work for the E MOSFET.
4) To determine the value of ID at a given value of VGs we must use the following relation

$$Id = K[V_{gs} - V_{gs(Th)}]^2$$

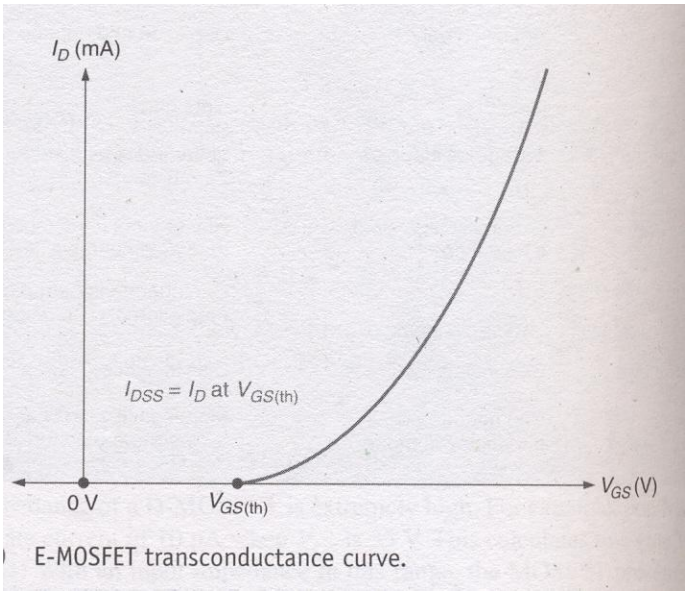
Where K is constant for the MOSFET . found as

$$K = \frac{Id(on)}{[vgs(on) - Vgs(Th)]2}$$

From the data specification sheets, the 2N7000 has the following ratings.

Id(on)= 75mA(minimum).

And Vgs(th)=0.8(minimum)



E-MOSFET transconductance curve.

5.8 APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and +5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

5.9 BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage VGS and drain current ID which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

1) Self bias
2) Voltage divider bias.

5.9.1 SELF BIAS

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate. A self bias circuit is shown in the fig. Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative VGS for an N channel JFET and a positive VGS for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig. The gate resistor RG doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V .RG is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor RS makes gate source junction reverse biased.

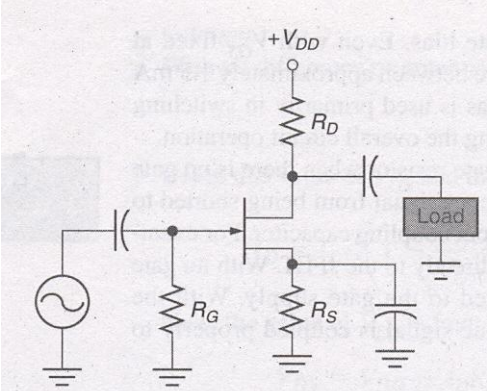


FIGURE 12.19 Self-bias.

For the dc analysis coupling capacitors are open circuits.

For the N channel FET in Fig (a)

IS produces a voltage drop across RS and makes the source positive w.r.t ground. In any JFET circuit all the source current passes through the device to the drain circuit .This is due to the fact that there is no significant gate current.

We can define source current as IS = ID

(VG =0 because there is no gate current flowing in RG So VG across RG is zero)

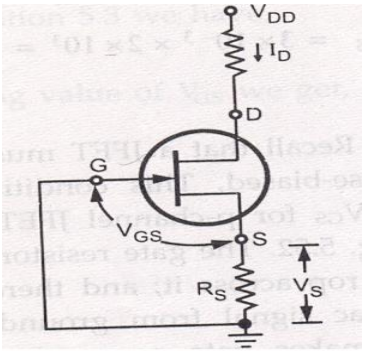
VG =0 then VS= ISRS =ID RS

VGS = VG-VS =0-ID RS=- ID RS

DC analysis of self Bias:-

In the following DC analysis, the N channel J FET shown in the fig. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor RG by a short circuit equivalent.:. IG = 0.The relation between ID and VGS is given by



$$Id=Idss[1-\frac{Vgs}{Vp}]^2$$

VGS for N channel JFET is =-id Rs

Substuting this value in the above equation

$$Id=Idss[1-\frac{(-IdRs)}{Vp}]^2$$

$$Id=Idss[1+\frac{(IdRs)}{Vp}]^2$$

For the N-chanel FET in the above figure

Is produces a voltage drop across Rs and makes the source positive w.r.t ground in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current. Therefore we can define source current as Is=Id and Vg=0 then

Vs= Is Rs =IdRs

Vgs=Vg-Vs=0-IdRs=-IdRs

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig.

The maximum drain current is 5mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

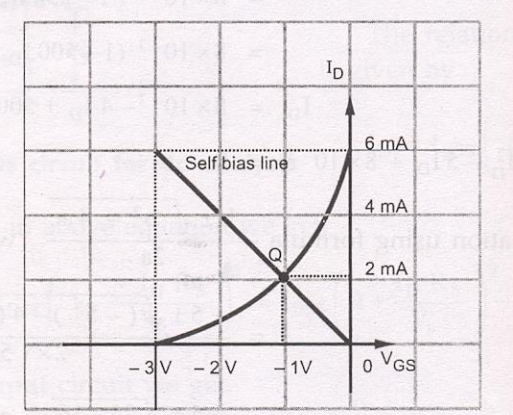


Fig. 5.55 Transfer characteristics

Now using the equation VGS = -IDRS and assuming RS of any suitable value we can draw the self bias line.

Let us assume RS = 500Ω

With this Rs , we can plot two points corresponding to ID = 0 and Id = IDSS

for ID = 0

VGS = -ID RS

VGS = 0X (500.Ω) = 0V

So the first point is (0 ,0)

(I_d, VGS)

For ID= IDSS=5mA

VGS = (-5mA) (500 Ω) = -3V

So the 2nd Point will be (5mA,-3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line.The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point , the ID is slightly > than 2mA and VGS is slightly > -1V. The Q point for the self bias JFET depends on the value of Rs.If Rs is large, Q point far down on the transconductance curve ,ID is small, when Rs is small Q point is far up on the curve , ID is large.

5.9.2 VOLTAGE DIVIDER BIAS:-

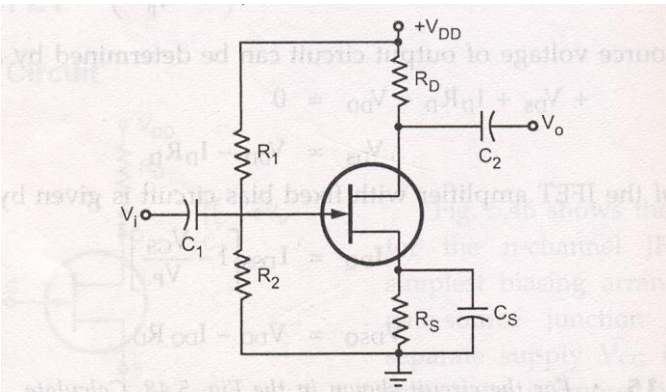


Fig. 5.49 Voltage divider bias for n-channel JFET

The fig. shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

VS = IDRS

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage divider formula.

$$Vg=\left(\frac{R2}{(R1+R2)}\right)Vdd$$

For dc analysis

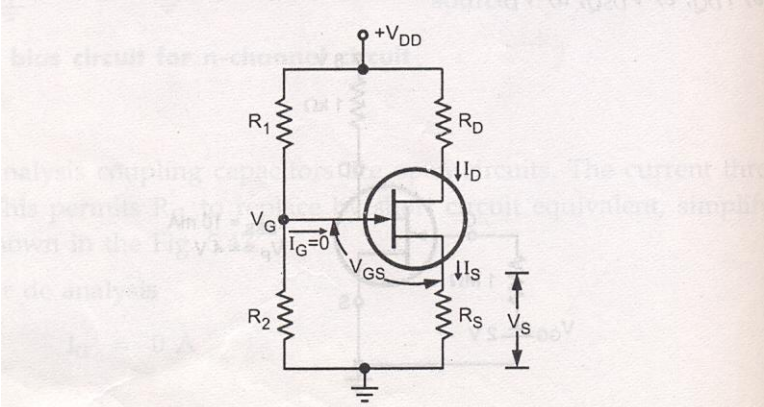


Fig. 5.50 Simplified voltage divider circuit for dc analysis

Applying KVL to the input circuit

VG-VGS-VS =0

:: VGS = VG-Vs=VG-ISRS

VGS = VG-IDRS :: IS = ID

Applying KVL to the input circuit we get

VDS+IDRD+VS-VDD =0

::VDS = VDD-IDRD-IDRS

VDS = VDD-ID (RD +RS)

The Q point of a JFET amplifier , using the voltage divider bias is

IDQ = IDSS [1-VGS/VP]2

VDSQ = VDD-ID (RD+RS)

COMPARISON OF MOSFET WITH JFET

a. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel.

b. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.

c. The gate leakage current in a MOSFET is of the order of 10^{-12}A. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω. The gate leakage current of a JFET is of the order of 10^{-9}A., and its input resistance is of the order of 10^{8}Ω.

d. The output characteristics of the JFET are flatter than those of the MOSFET, and hence the drain resistance of a JFET (0.1 to 1MΩ) is much higher than that of a MOSFET (1 to 50kΩ).

e. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.

f. Comparing to JFET, MOSFETs are easier to fabricate.

g. Special digital CMOS circuits are available which involve near zero power dissipation and very low voltage and current requirements. This makes them suitable for portable systems.

FET AMPLIFIERS

5.10 INTRODUCTION

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input impedence. Because of high input impedence and other characteristics of JFETs they are preferred over BJTs for certain types of applications.

There are 3 basic FET circuit configurations:

i)Common Source

ii)Common Drain

iii)Common Gain

Similar to BJT CE,CC and CB circuits, only difference is in BJT large output collector current is controlled by small input base current whereas FET controls output current by means of small input voltage. In both the cases output current is controlled variable.

FET amplifier circuits use voltage controlled nature of the JFET. In Pinch off region, I_D depends only on V_{GS}.

5.11 Common Source (CS) Amplifier

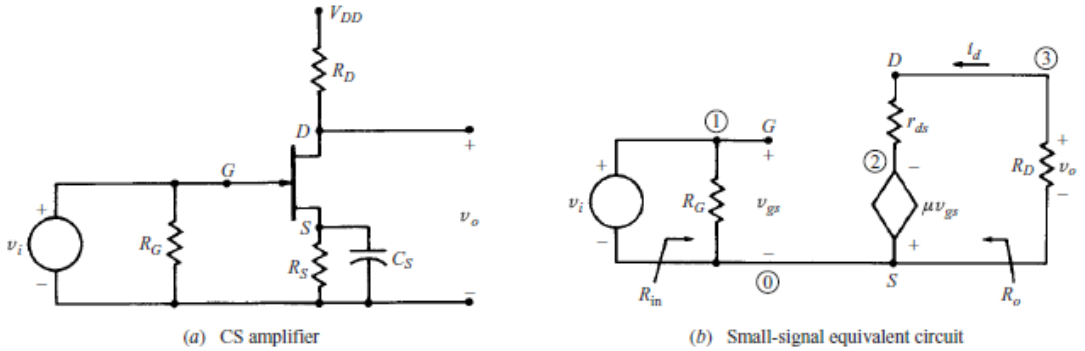


Fig. 5.1 (a) CS Amplifier (b) Small-signal equivalent circuit

A simple Common Source amplifier is shown in Fig. 5.1(a) and associated small signal equivalent circuit using voltage-source model of FET is shown in Fig. 5.1(b)

Voltage Gain

Source resistance (R_S) is used to set the Q-Point but is bypassed by C_S for mid-frequency operation.

From the small signal equivalent circuit ,the output voltage

$$V_O = -R_D \mu V_{gs}(R_D + r_d)$$

Where $V_{gs} = V_i$, the input voltage,

Hence, the voltage gain,

$$A_V = V_O / V_i = -R_D \mu (R_D + r_d)$$

Input Impedence

From Fig. 5.1(b) Input Impedence is

$$Z_i = R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

Output Impedance

Output impedance is the impedance measured at the output terminals with the input voltage $V_I = 0$

From the Fig. 5.1(b) when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence

$$\mu V_{gs} = 0$$

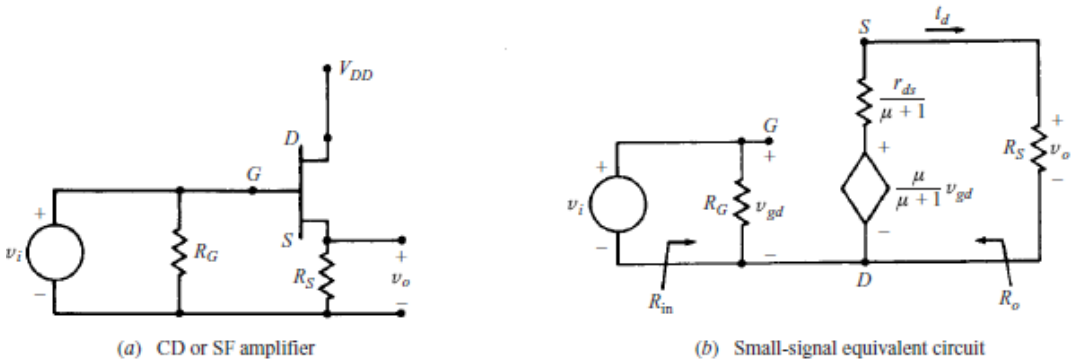
The equivalent circuit for calculating output impedence is given in Fig. 5.2.

Output impedence $Z_o = r_d \parallel R_D$

Normally r_d will be far greater than R_D . Hence $Z_o \approx R_D$

5.12 Common Drain Amplifier

A simple common drain amplifier is shown in Fig. 5.2(a) and associated small signal equivalent circuit using the voltage source model of FET is shown in Fig. 5.2(b).Since voltage V_{gd} is more easily determined than $V_{gs,}$ the voltage source in the output circuit is expressed in terms of V_{gs} and Thevenin's theorem.



(a) CD or SF amplifier (b) Small-signal equivalent circuit

Fig. 5.2 (a)CD Amplifier (b)Small-signal equivalent circuit

Voltage Gain

The output voltage,

$$V_O = R_S \mu V_{gd} / (\mu + 1) R_S + r_d$$

Where $V_{gd} = V_i$ the input voltage.

Hence, the voltage gain,

$$A_v = V_O / V_i = R_S \mu / (\mu + 1) R_S + r_d$$

Input Impedence

From Fig. 5.2(b), Input Impedence $Z_i = R_G$

Output Impedence

From Fig. 5.2(b), Output impedence measured at the output terminals with input voltage $V_i = 0$ can be calculated from the following equivalent circuit.

As $V_i = 0$: $V_{gd} = 0$: $\mu v_{gd} / (\mu + 1) = 0$

Output Impedence

$$Z_O = r_d / (\mu + 1) \parallel R_S$$

When $\mu \gg 1$

$$Z_O = (r_d / \mu) \parallel R_S = (1/g_m) \parallel R_S$$

5.13 BIASING FET

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage VGS and drain current ID which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

1. Self bias
2. Voltage divider bias.

5.13.1. SELF BIAS:-

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate.

A self bias circuit is shown in the fig 5.3

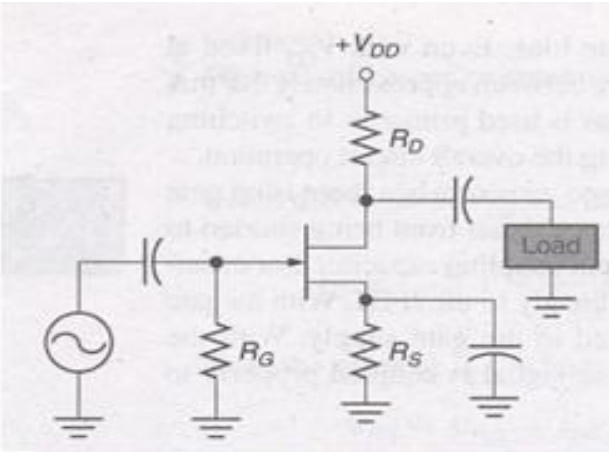


fig 7.3

Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative VGS for an N channel JFET and a positive VGS for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig 5.3. The gate resistor RG doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V .RG is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor RS makes gate source junction reverse biased.

DC analysis of self Bias:-

In the following DC analysis , the N channel J FET shown in the fig5.4. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor RG by a short circuit equivalent.

:. IG = 0

The relation between ID and VGS is given by

$$Id=Idss[1-\frac{Vgs}{Vp}]^2$$

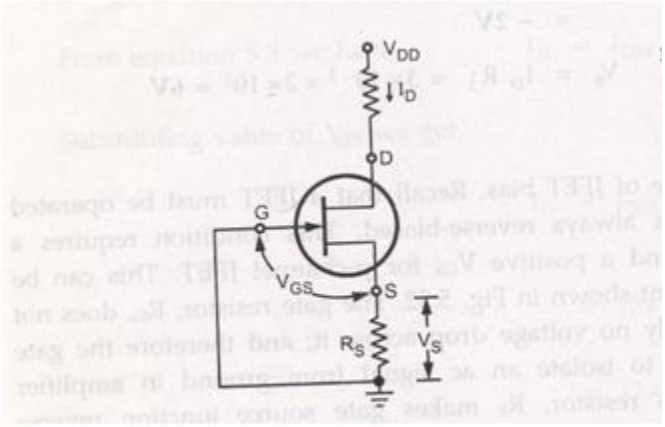


fig 7.4

VGS for N channel JFET is =-id Rs

Substuting this value in the above equation

$$Id=Idss[1-\frac{(-IdRs)}{Vp}]^2$$

$$Id=Idss[1+\frac{(IdRs)}{Vp}]^2$$

For the N-chanel FET in the above figure

Is produces a voltage drop across Rs and makes the source positive w.r.t ground

in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current

therefore we can define source current as Is=Id and Vg=0 then

Vs= Is Rs =IdRs

Vgs=Vg-Vs=0-IdRs=-IdRs

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig5.5.

The maximum drain current is 6mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

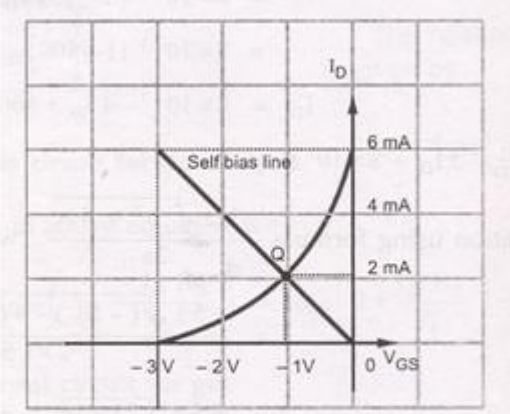


fig 7.5 Transfer characteristics

Now using the equation VGS = -IDRS and assuming RS of any suitable value we can draw the self bias line.

Let us assume RS = 500Ω

With this Rs , we can plot two points corresponding to ID = 0 and Id = IDSS

for ID = 0

VGS = -ID RS

VGS = 0X (500.Ω) = 0V

So the first point is (0 ,0)

(I_d, VGS)

For ID= IDSS=6mA

VGS = (-6mA) (500 Ω) = -3V

So the 2nd Point will be (6mA,-3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point , the ID is slightly > than 2mA and VGS is slightly > -1V. The Q point for the self bias JFET depends on the value of Rs.If Rs is large, Q point far down on the transconductance curve ,ID is small, when Rs is small Q point is far up on the curve , ID is large.

5.13.2 VOLTAGE DIVIDER BIAS:-

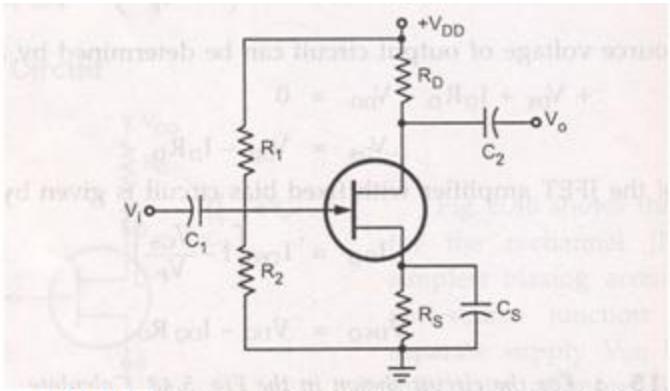


fig 7.6 **Voltage divider bias for n-channel JFET**

The fig5.6 shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

VS = IDRS

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage divider formula.

$$Vg=\left(\frac{R2}{(R1+R2)}\right)Vdd$$

For dc analysis fig 5.5

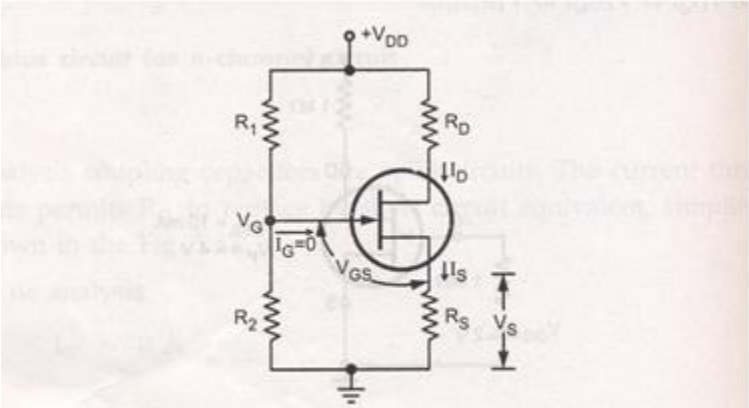


fig 7.7 **Simplified voltage divider circuit for dc analysis**

Applying KVL to the input circuit

VG-VGS-VS =0

:: VGS = VG-Vs=VG-ISRS

VGS = VG-IDRS :: IS = ID

Applying KVL to the input circuit we get

VDS+IDRD+VS-VDD =0

::VDS = VDD-IDRD-IDRS

VDS = VDD-ID (RD +RS)

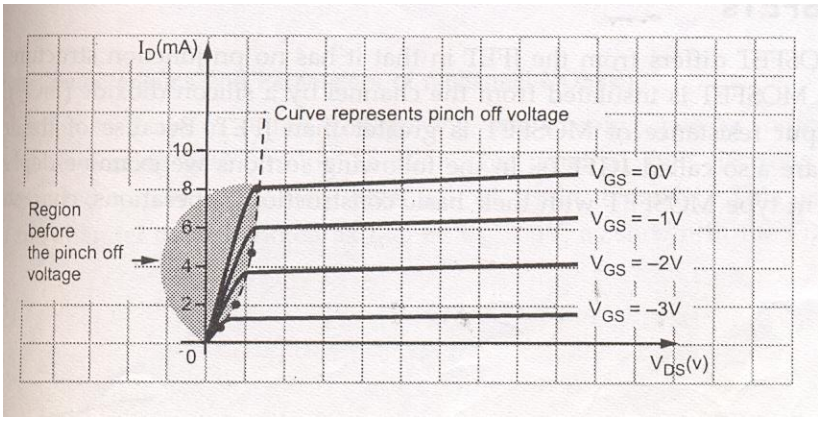
The Q point of a JFET amplifier , using the voltage divider bias is

IDQ = IDSS [1-VGS/VP]2

VDSQ = VDD-ID (RD+RS)

5.14 JFET AS A VVR OR VDR

Let us consider the drain characteristics of FET as shown in the fig.



In this characteristics we can see that in the region before pinch off voltage, drain characteristics are linear, i.e. FET operation is linear. In this region the FET is useful as a voltage controlled resistor,i.e. the drain to source resistance is controlled by the bias voltage VGS.(In this region only FET behaves like an ordinary resistor This resistances can be varied by VGS) .The operation of FET in the region is useful in most linear applications of FET.In such an application the FET is also referred to as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

The drain to source conductance (rd)

$g_d=\frac{Id}{Vds}$ for small values of VDS which may also be expressed as

$g_d=g_{d0}(1-(\frac{Vgs}{Vp})^{1/2})$

Where g_{d0} is the value of drain conductance

When the variation of the rd with VGS can be closely approximated by the expression

$rd=(\frac{r0}{1-KVgs})$ Where ro = drain resistance at zero gate bias.K = a constant, dependent upon FET type.

5.14.1 APPLICATION OF VVR

The VVR property of FET can be used to vary the voltage gain of a multistage amplifier A, as the signal level is increased. This action is called AGC automatic gain control. A typical arrangement is shown in the fig.

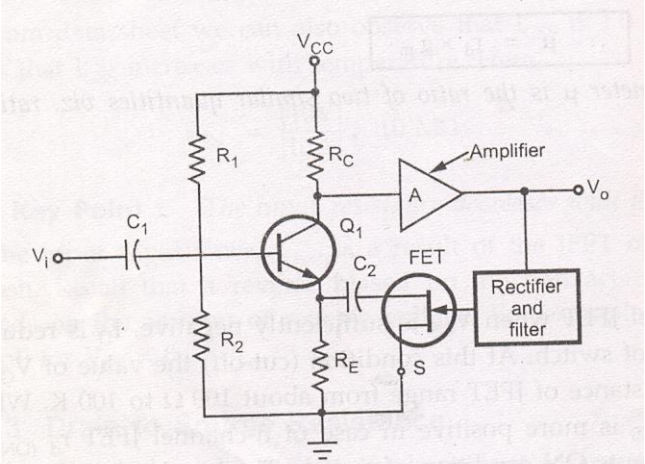


Fig. 4.54 AGC amplifier using FET as a voltage variable resistor

Here maximum value of signal is taken rectified; filter to produce a DC voltage proportional to the output signal level. This voltage is applied to the gate of JFET, this causing the resistance between drain and source to change. As this resistance is connected across RE, so effective RE also changes according to change in the drain to source resistance. When output signal level increases, the drain to source resistance rd increases, increasing effective RE. Increase in RE causes the gain of transistor Q1 to decrease, reducing the output signal. Exactly reverse process takes place when output signal level decreased.

:: The output signal level is maintained constant. It is to be noted that the DC bias conditions of Q1 are not affected by JFET since FET is isolated from Q1 by capacitor C2

EDC Model Papers

MALLAREDDY COLLEGE OF ENGINEERING AND TECHNOLOGY, HYDERABAD

B.Tech II Year I Semester Examinations, Model Paper I -2014

Electronic Devices and Circuits

(Common to EEE, ECE, CSE, EIE, BME, IT, MCT, ETM, ECOMPE)

Time: 3 hours **Max. Marks: 75**

PART-A

1.Answer all the following questions:

(a)What is a pn junction? How is it formed? (2M)

(b) Sketch the energy-band picture for (3M)

i} an intrinsic ii}n-type iii} a p-type semiconductor

Indicates the positions of the fermi, the donor &the acceptor levels.

(c) What is meant by rectifier? (2M)

(d) Compare the performance measure of different filters. (3M)

(e) Why Transistor is called Current Controlled Device? (2M)

(f)What is early effect? How does it modify the V-I characteristics of a BJT? (3M)

(g) What is meant by operating point? Explain its significance (2M)

(h)What is the condition for thermal stability and thermal resistance? (3M)

(i) Explain when a FET acts as a voltage variable resistor. (2M)

(j) Explain the drain and transfer characteristics of a JFET in details (3M)

Answer all the following questions **10x5=50**

2.a) Derive an expression for total diode current starting from Boltzmann relationship in terms of the applied voltage.

b) The reverse saturation current of a silicon p – n function diode at an operating temperature of 270C is 50 nA. Compute the dynamic forward and reverse resistances of the diode for applied voltages of 0.8 V and -0.4 V respectively.

OR

3.a) Explain the operation of silicon p – n junction diode and obtain the forward bias and reverse bias Volt – Ampere characteristics.

b) Obtain the transition capacitance C_T of a junction diode at a reverse bias voltage of 12 V if C_T of the diode is given as 15 PF at a reverse bias of 8 V. Differentiate between transition and diffusion capacitances.

4.a) Define the following terms of a rectifier and filter:

i) Ripple Factor

ii) Regulation

iii) Rectification Efficiency

iv) Form Factor

b) What is the ripple factor if a power supply of 220 V, 50 Hz is to be Full Wave rectified and filtered with a 220μF capacitor before delivering to a resistive load of 120Ω? Compute the value of the capacitor for the ripple factor to be less than 15%.

OR

5.a) Derive expressions for ripple factor of a Full Wave Rectifier with and without a capacitive filter.

b) Compute the average and RMS load currents, TUF of an unfiltered centre tapped Full Wave Rectifier specified below.

Input voltage to transformer = 220 V/50 Hz.

Step down ratio of centre tapped transformer = 4:1(Primary to each section secondary).

Sum of transformer secondary winding in each secondary segment and diode forward resistance = 100Ω. Load resistance, RL= 220Ω.

6.a) With the help of input & output characteristics, explain the operation of a BJT in Common Emitter Configuration.

b) For an NPN transistor with α_N= 0.98, I_{CO}= 2μA and I_{EO}= 1.6μA connected in Common Emitter Configuration, calculate the minimum base current for which the transistor enters into saturation region. V_{CC} and load resistance are given as 12 V and 4.0 KΩ respectively.

OR

7.a) Compare the characteristics of a BJT in CB, CE and CC configurations.

b) A Silicon BJT is connected in common Emitter configuration with collector – to –Base bias. Calculate the base resistance R_b for the quiescent collector – to – Emitter voltage, V_{CE} has to be 4 V. V_{CC} and R_C are given as 2 V and 1 KΩ respectively. Assume β= 100, V_{BE} to be zero volts. Also find the stability factor of the circuit.

8.a) Explain how self biasing can be done in a BJT with relevant sketches and waveforms.

b) Design a self bias circuit for the following specifications: V_{CC} = 12 V; V_{CE} = 2V; I_C = 4mA; h_{fe} = 80. Assume any other design parameters required. Draw the designed circuit.

OR

9.a) Explain how biasing is provided to a transistor through potential divider bias. List the assumptions made. List the need of bias compensation methods.

b) An NPN transistor with β= 50 is used in common Emitter configuration with V_{CC} = 10V and R_C = 2.2 KΩ. Biasing is done through a 100 KΩ resistance from collector – to – Base. Assuming V_{BE} to be zero volts, Find i) The quiescent point ii) The stability factor, 'S'.

10.a) Detail the construction of an n-channel MOSFET of depletion type. Draw and explain its characteristics.

b) A self biased p – channel JFET has a pinch – off voltage of VP = 5 V and IDSS = 12 mA. The supply voltage is 12 V. Determine the values of RD and RS so that ID = 5 mA and VDS = 6V.

OR

11.a) Explain the significance of threshold voltage of a MOSFET. Discuss the methods to reduce threshold voltage, V_T.

b) A FET follows the relation $I_D = I_{DSS}[1 - V_{GS}/V_p]^2$. What are the values of ID and gm for VGS = -1.5 V if IDSS and VP are given as 8.4 mA and -3V respectively.

MALLAREDDY COLLEGE OF ENGINEERING AND TECHNOLOGY, HYDERABAD

B.Tech II Year I Semester Examinations, Model Paper II -2014

Electronic Devices and Circuits

(Common to EEE, ECE, CSE, EIE, BME, IT, MCT, ETM, ECOMPE)

Time: 3 hours **Max. Marks: 75**

PART-A

1.Answer all the following questions:

(a)What do you mean by potential barrier for a p-n junction? (2M)

(b)What is the significance of negative resistance of a tunnel diode (3M)

(c) Define peak inverse voltage (PIV). (2M)

(d) Explain FWR working principle with circuit and waveforms. (3M)

(e)What are the three regions of a Transistor? (2M)

(f) What is thermal runway ? how can it avoided? (3M)

(g)What is faithful amplification? (2M)

(h) How α,β and γ are related to each other? (3M)

(i)Define the pinch off voltage (Vp) sketch the depletion region before and after pinchoff? (2M)

(j) Derive Expression for saturation drain current (3M)

Answer all the following questions: **5x10= 50 marks**

2. Difference between

i) Static and dynamic resistances of a p – n diode.

ii) Transition and Diffusion capacitances of a p – n diode.

iii)Volt – Ampere characteristics of a single silicon p – n diode and two identical silicon p- n diodes connected in parallel.

iv) Avalanche and zener break down mechanisms

OR

3.a) Define the following terms for a PN diode

i) Dynamic resistance

ii) Load line

iii) Difference capacitance

iv) Reverse saturation current

b) A reverse bias voltage of 90V is applied to a Germanium diode through a resistance R. The reverse saturation current of the diode is 50 μA at an operating temperature of 250C. Compute the diode current and voltage for

i) R = 10 MΩ

ii) R = 100 KΩ

4.a) Define Ripple factor and form factor. Establish a relation between them.

b) Explain the necessity of a bleeder resistor in an L – section filter used with a Full Wave filter.

c) Compute ripple factor of an L – section choke input filter used at the output of a Full wave rectifier and capacitor values of the filter are given as 10 H and 8.2 μF respectively.

OR

5.a) List out the merits and demerits of Bridge type Full Wave rectifiers over centre tapped type Full Wave rectifiers.

b) The secondary voltages of a centre tapped transformer are given as 60V-0V-60V the total resistance of secondary coil and forward diode resistance of each section of transformer secondary is 62 Ω. Compute the following for a load resistance of 1 KΩ.

i) Average load current

ii) Percentage load regulation

iii) Rectification efficiency

iv) Ripple factor for 240 V/50Hz supply to primary of transformer.

c) What is bleeder resistance in L – section filters?

6.a) Describe the significance of the terms, 'α' and 'β'. Establish a relation between them.

b) A transistor is operated at a forward emitter current of 2 mA and with the collector open – circuited. Assuming $\alpha_N = 0.98$, $I_{EO} = 1.6$ μA and $I_{CO} = 2$ μA, determine

i) The junction voltages V_C and V_E

ii) The collector to Emitter voltage V_{CE}

iii) The region of transistor operation (Saturation/Active/Cut-off).

Assume any other values necessary.

OR

7.a) Describe the functioning of a BJT in common base configuration.

b) Determine the collector current of a BJT with both of its junctions reverse biased. Assume $I_{CO} = 5$μA, $I_{EO} = 3.58$ μA, $\alpha_N = 0.98$ and any other parameter values as required.

c) How do you identify the region of operation of a BJT to be saturation region from the values of various circuit currents?

8.a) Justify statement "Potential divider bias is the most commonly used biasing method" for BJT circuits. Explain how bias compensation can be done in such biasing through diodes.

b) An NPN transistor with $\beta = 100$ is used in common Emitter configuration with Collector – to – Base bias. If VCC = 10 V, RC = 1 K and VBE = 0 V, determine i)Rb such that quiescent Collector – to – Emitter Voltage is 4V.

ii) The stability factor, 'S'.

OR

9.a) Define all the four hybrid parameters of a BJT in CE configuration. Draw the circuit and its equivalent circuit.

b) The source and load resistances connected to a BJT amplifier in

CE configuration are 680Ω and 1 KΩ respectively. Calculate the voltage gain AV and the input resistance R_i if the h-parameters are listed as h_{ie} = 1.1 kΩ ; $h_{re} = 2\times10^{-4}$; h_{fe}= 50 and h_{oe}= 20 μmhas. Compute A_V and R_i using both approximate and exact analysis.

10.a) With the help of a neat schematic, explain the functioning of a common source amplifier.

b) Bring out the differences between BJT and FET. Compare the three configurations of JFET amplifiers.

OR

11.a) Differentiate between enhancement and depletion modes of a MOSFET with the help of its characteristics and construction.

b) Determine the pinch off voltage for an N – channel silicon. JFET if the thickness of its gate region is given as 3.2×10^{-4}cm and the donor density in n-type region is $1.2\text{x}10^{-5}/\text{cm}^3$.

c) Establish a relation between the three JFET parameters, μ, r_d and g_m.

MALLAREDDY COLLEGE OF ENGINEERING AND TECHNOLOGY, HYDERABAD

B.Tech II Year I Semester Examinations, Model Paper III -2014

Electronic Devices and Circuits

(Common to EEE, ECE, CSE, EIE, BME, IT, MCT, ETM, ECOMPE)

Time: 3 hours **Max. Marks: 75**

PART-A

Answer all the following questions:

(a)What is mean by zener breakdown (2M)

(b)Explain the effect of temperature on the V-I characteristics of pn junction diode (3M)

(c)What is meant by filter (2M)

(d)Bridge rectifier is becoming more and more popular, why? (3M)

(e)Write B.J.T specifications (2M)

(f) Explain how transistor acts as an Amplifier? (3M)

(g)What is meant by stabilization (2M)

(h)What is thermal runway? How can it avoid? (3M)

(i)State the application of JFET (2M)

(j) When FET acts as a voltage variable resistor (vvr)? (3M)

Answer all the following questions: **5x10= 50 marks**

2.a) Explain the concept of diode capacitance. Derive expression for transition capacitance?

b) Find the value of D.C. resistance and A.C resistance of a Germanium junction diode at 25^0C with reverse saturation current, I_o= 25μA and at an applied voltage of 0.2V across the diode.

OR

3.a) What do you understand by depletion region at p-n junction? What is the effect of forward and reverse biasing of p-n junction on the depletion region? Explain with necessary diagrams.

b) Explain Zener and avalanche breakdown mechanisms in detail.

4. Define the following terms and derive the equations with respect to half-wave rectifier: i) Ripple factor ii) Peak inverse voltage iii) Rectification efficiency iv) % Regulation.

OR

5.a) Draw the circuit diagram of full-wave rectifier with inductor filter. Explain its operation with necessary equations.

b) A HWR circuit supplies 100mA DC current to a 250Ω load. Find the DC output voltage, PIV rating of a diode and the r.m.s. voltage for the transformer supplying the rectifier

6.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CB configuration. Also derive expression for output current.

b) Derive the relation among α, β and γ.

OR

7.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.

b) Calculate the collector current and emitter current for a transistor with α= 0.99 and ICBO= 50μA when the base current is 20μA.

8.a) Explain the basic requirements of transistor biasing. Verify these requirements in collector to base bias circuit.

b) Design a fixed bias circuit using silicon transistor, with the following specifications: VCC = 16V, VBE = 0.7V, VCEQ= 8V, ICQ = 4 mA & β= 50.

OR

9.a) What is thermal runaway in transistors? Obtain the condition for thermal stability in transistors.

b) Draw the circuit diagram, AC equivalent & small signal equivalent of Emitter Follower amplifier using accurate h-parameter model. Derive expressions for AVs , AIs, RI & RO.

10.a) Explain the construction & operation of an N-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.

b) Define pinch-off voltage and transconductance in field effect transistors.

OR

11(a) Write short notes on applications of FET as a voltage variable resistor.

b) Explain the principle of CS amplifier with the help of circuit diagram. Derive the expressions for A_V, input impedance and output impedance.

MALLAREDDY COLLEGE OF ENGINEERING AND TECHNOLOGY, HYDERABAD

B.Tech II Year I Semester Examinations, Model Paper IV -2014

Electronic Devices and Circuits

(Common to EEE, ECE, CSE, EIE, BME, IT, MCT, ETM, ECOMPE)

Time: 3 hours **Max. Marks: 75**

PART-A

1. Answer all the following questions:

a) What is diode equation? (2M)

b) Draw the v-I characteristics of SCR & define all related terms. (3M)

c) What is the purpose of bleeder resistance in a rectifier circuit using LC filter? (2M)

d) Write short note on Full wave rectifier (FWR) along with input output waveforms. (3M)

e) Why hybrid parameters are called so? Define those (2M)

f) What factors are to be considered for selecting the operating point Q for an amplifier? (3M)

g) Why does potential divider method of biasing become universal? (2M)

h) What is the major difference between a BJT and FET? (3M)

i) Draw the symbols of JFET (N Channel/P channel) MOSFET (Depletion MOSFET (n-channel/p-channel)and Enhancement MOSFET (n-channel/p-channel) (2M)

j) Draw the low frequency hybrid equivalent circuit for C.E .C.B and CC (3M)

Answer all the following questions: **5x10= 50 marks**

2.a) Explain about various current components in a forward biased p-n junction diode.

b) With neat sketches and necessary waveforms explain about the regulation characteristics

OR

3.a) With neat sketches and necessary waveforms explain the volt ampere characteristics of PN diode.

b) Explain the temperature dependence of VI characteristics of PN diode.

c) Compare ideal and practical diodes.

4.a) Draw the circuit of full-wave rectifier with capacitor filter. Explain its operation with necessary equations.

b) A full wave rectifier circuit uses two silicon diodes with a forward resistance of 20Ω each. A DC voltmeter connected across the load of 1K

Ω reads 55.4 volts. Calculate

i) Irms

ii) Average voltage across each diode

iii) ripple factor iv) Transformer secondary voltage rating.

OR

5.a) Draw the circuit of full-wave rectifier with L-section filter and derive expression for its ripple factor.

b) A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together has a resistance of 100Ω, determine

i) dc voltage across the load.

ii) dc current flowing through the load.

iii) dc power delivered to the load.

iv) PIV across each diode.

6.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.

b) The reverse leakage current of the transistor when connected in CB configuration is 0.2 μA while it is 18 μA when the same transistor is connected in CE configuration. Calculate α and β of the transistor.

OR

7.a) With the help of a neat diagram explain different current components in an NPN bipolar junction transistor.

b) With reference to bipolar junction transistors, define the following terms and explain.

i) Emitter efficiency.

ii) Base Transportation factor.

iii) Large signal

8.a) Explain how ICO variations are compensated with the help of diode and thermistor in transistor biasing circuits?

b) Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: VCC = 16V, VBE = 0.7V, VCEQ= 8V, ICQ= 4 mA & β= 50.

OR

9.a) Explain the basic requirements of transistor biasing. Verify these requirements in Emitter feedback bias circuit.

b) An NPN Silicon transistor with $\beta=50$ is used in a common emitter circuit with VCC=10V, RC=2K. The bias is obtained by connecting a 100K resistance from collector to base. Find i) Q-Point ii) Stability factor, S

10.a) Explain the construction & operation of an P-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.

b) Explain why field effect transistor is called as unipolar and voltage controlled device

OR

11.a) With neat sketches, necessary equations explain the drain & transfer characteristics of MOSFET in enhancement mode.

b) Why is a Field Effect Transistor called unipolar & voltage controlled device? Explain the drain & transfer characteristics of a JFET in detail.

MALLAREDDY COLLEGE OF ENGINEERING AND TECHNOLOGY, HYDERABAD

B.Tech II Year I Semester Examinations, Model Paper V -2014

Electronic Devices and Circuits

(Common to EEE, ECE, CSE, EIE, BME, IT, MCT, ETM, ECOMPE)

Time: 3 hours **Max. Marks: 75**

1.Answer all the following questions: **5x2= 10 marks**

a) What is "dark current" of a photo diode? (2M)

b) Which type of diode capacitance is used in the varactor diode, explain. (3M)

c) What is Diffusion and Drift Currents? (2M)

d) Derive ripple factor of FWR. (3M)

e) What is a dc power supply (Regulated power supply)? (2M)

f) Draw the characteristics of Photo Diode. (3M)

g) Define reverse leakage current in C.E configuration (2M)

h) Compare CB, CE and CC configurations. (3M)

i) Define the four- h parameters (2M)

j) Explain the JFET small signal model (3M)

Answer all the following questions: **5x10= 50 marks**

1 a) Explain the formation of depletion region in an open circuited pn junction with neat Sketches.

b) The voltage across a silicon diode at room temperature of 300oK is 0.7V when 2mA Current flows through it. If the voltage increases to 0.75V, calculate the diode current.

(OR)

3. Discuss the constructional details of SCR and Schotky barrier diode.

2. A HWR circuit supplies 100mA DC current to a 250Ω load. Find the DC output voltage, PIV rating of a diode and the r.m.s. voltage for the transformer supplying the rectifier

(OR)

Draw the circuit of full-wave rectifier with capacitor filter. Explain its operation with necessary equations.

3. The reverse leakage current of the transistor, when connected in CB configuration is 0.2mA, while it is 18 m A when the same transistor is connected in CE configuration.

Calculate α and β of the transistor

(OR)

a) Compare the three transistor amplifier configurations with related to A_I, A_V, R_i and R_O.

b) For the emitter follower with R_S = 0.5K, R_L = 50K, h_{fe} = -50, h_{ie} = 1K, h_{oe} = 25μA/V, h_{re} = 1. Calculate A_V, A_I, Z_i and Z_O.

4. Draw a fixed bias circuit and explain its operation. Calculate the Stability factor

(OR)

(a)What is thermal runaway in transistors? Obtain the condition for thermal stability in transistors.

b) Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β = 50.

5. a) Write the expressions for mid-frequency gain of a FET Common Source Amplifier.

b) Discuss the high frequency response of CD Configuration.

(OR)

Explain the working of MOSFET in i) Enhancement mode ii) Depletion mode.

Draw the necessary diagrams and graphs.