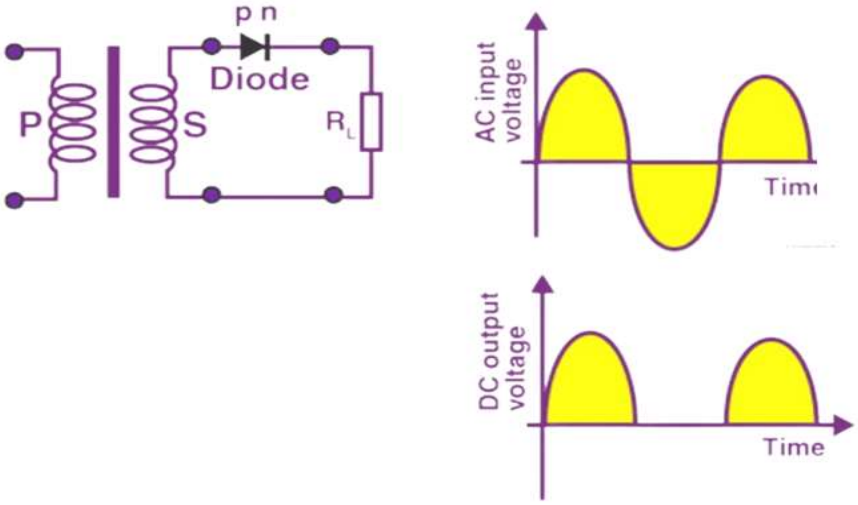
one complete cycle, the diode is forward-biased for half of the time, while it is reverse-biased for the other half. Optimal outcomes are achieved by the use of alternating half-cycles.

Working: in the rectifier circuit has input of alternating cycles positively and negatively. Since the current flows from positive to negative during the positive half of the input, the a.c. supply only produces a positive half cycle. When the transformer receives a.c., the diode's secondary winding voltage lowers. Pulsating D.C. voltage will reach the load resistor, reducing A.C. supply variations.



The half-wave rectifier cycles positively and negatively. Since the current flows from positive to negative during the positive half of the input, the a.c. supply only produces a positive half cycle. When the transformer receives a.c., the diode's secondary winding voltage lowers. Pulsating d.c. voltage will reach the load resistor, reducing a.c. supply variations.

Characteristics:

Ripple Factor

Filters like inductors and capacitors correct DC oscillations to reduce ripples. To quantify waves, utilize the ripple factor (γ). Ripple factor indicates output DC ripples. A lower ripple factor means a less oscillating output DC.

Ripple factor is the ratio of RMS value of the AC component of the output voltage to the DC component of the output voltage.

$$\gamma = \sqrt{(\frac{V_{rms}}{V_{DC}})^2 - 1}$$

DC Current

DC current is given as:

$$I_{DC} = \frac{I_{max}}{\pi}$$

Where, I_{max} is the maximum DC load current

DC Output Voltage

The DC voltage at the load resistor RL is determined by multiplying the output DC voltage with the load resistor RL. The provided value represents the direct current (DC) voltage output:

$$V_{DC} = \frac{V_{Smax}}{\pi}$$

Where, V_{Smax} is the maximum secondary voltage

Form Factor

The form factor is RMS/DC= 1.57.

Rectifier Efficiency

The ratio of output DC power to input AC power is rectifier efficiency. Its efficiency 40.6%

Advantages of Half Wave Rectifier

- Inexpensive
- Simple in construction and operation

Disadvantages:

- Maximum in Ripple production
- It produce distorted harmonics
- The performances is moderate

Applications:

• **Power rectification:** Half wave rectifier and transformer are used to power equipment.

. **Signal demodulation:** Half wave rectifiers are used to demodulate AM signals.

• **Signal peak detector:** Half wave rectifier detects incoming waveform peak.

Full wave Rectifier:

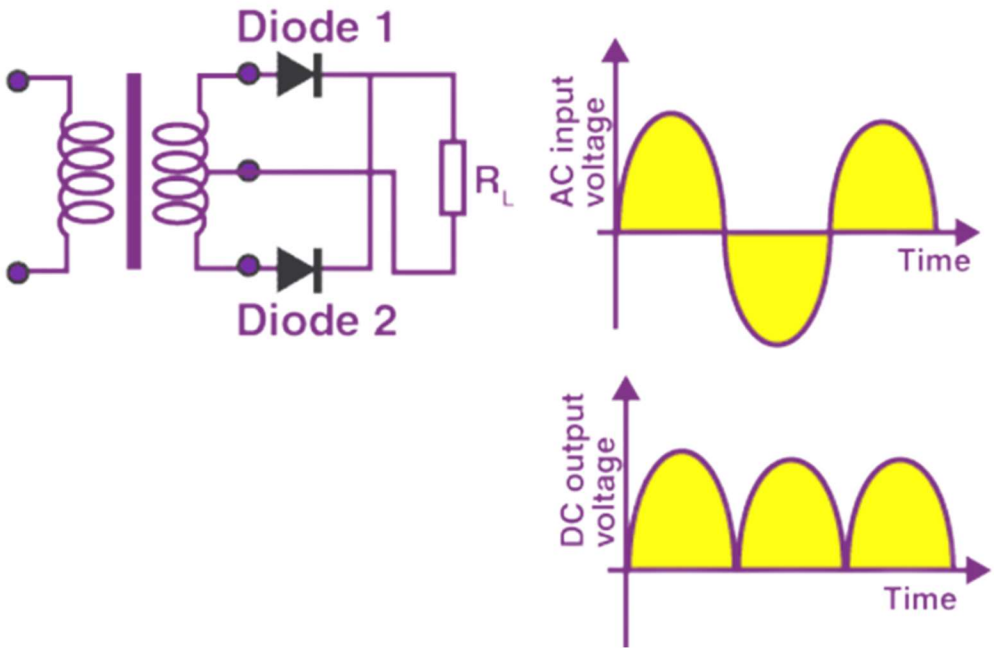
What Is Full Wave Rectifier?

Full-wave rectifier circuits are capable of producing direct current (DC) voltage or current. Full-wave rectifiers have superior performance in

terms of average output voltage and ripple reduction compared to half-wave rectifiers.

Working:

Full-wave rectifiers use both sides of the alternating current (a.c.) input. The p-n junction diode exhibits low resistance when it is in a forward biased state, while it demonstrates high resistance when it is in a reverse biased state. The purpose of the circuit is to provide a forward bias for the diode during the first half cycle, followed by a reverse bias during the second half cycle, and so on.



Characteristics

Ripple Factor

$$\gamma = \sqrt{(\frac{V_{rms}}{V_{DC}})^2 - 1}$$

DC Current

The currents originating from diodes D1 and D2 are directed towards the load resistor RL in a concurrent manner. The direct current (DC) may be determined by evaluating the ratio of the maximum current (Imax) to the mathematical constant π, since the current produced by both diodes is equivalent to this ratio.

$$I_{DC} = \frac{2I_{max}}{\pi}$$

Where, I_{max} is the maximum DC load current

DC Output Voltage

The constant output voltage is obtained at R_L and is given as:

$$V_{DC} = \frac{2V_{max}}{\pi}$$

Where, V_{max} is the maximum secondary voltage

Form Factor

The form factor refers to the ratio of the root mean square (RMS) current to the output direct current (DC) voltage. Full-wave rectifiers have a form factor of 1.11.

Rectifier Efficiency

The form factor refers to the ratio between the root mean square (RMS) current and the output direct current (DC) voltage. Full-wave rectifiers have a form factor of 1.11

Advantages of Full Wave Rectifier

- The rectifier efficiency of a full-wave rectifier is high
- The power loss is very low
- Number of ripples generated are less

Disadvantages of Full Wave Rectifier

- Very expensive

Applications of Full Wave Rectifier

Following are the uses of full-wave rectifier:

- Full-wave rectifiers are used for supplying polarized voltage in welding and for this bridge rectifiers are used.
- Full-wave rectifiers are used for detecting the amplitude of modulated radio signals.

Difference between Half Wave Rectifier and Full Wave Rectifier

Parameter	Half Wave Rectifier	Full Wave Rectifier
Definition	The half-wave rectifier is a rectifier which is used for converting the one-half cycle of AC input to DC output	A full-wave rectifier is a rectifier which is used for converting both the half cycles of AC input into DC output
No. of diodes used	1	2 or 4 depending on the type of circuit
Form factor	1.57	1.11
Rectifier efficiency	40.6%	81.2%
Ripple factor	Ripple factor of a half-wave rectifier is more	Ripple factor of a full-wave rectifier is less

Zener Diode

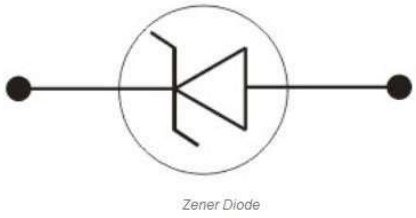
Zener diodes are semiconductors that are engineered to work in reverse direction and are extensively doped. To rephrase, the Zener diode is a type of semiconductor circuit intended to maximize performance in the breakdown area.

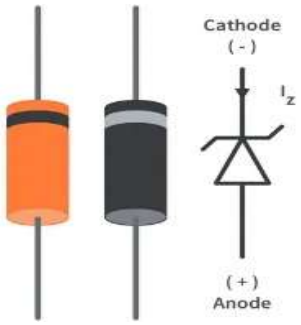
The diode is named after the inventor, Clearance Zener, because he is remembered for inventing this feature. Zener diodes are similar to regular PN junction diodes, with the exception that they are often operated in a reverse biased condition. It is not practicable to utilize a regular PN junction diode as a Zener diode when coupled in a reverse biased position. An very doped PN junction diode with a unique design is known as a Zener diode.

•During manufacturing, the quantity of doping is adjusted to manage the actual breakdown voltage. In this method, breakdown voltages may be controlled to occur at exact predetermined values ranging from around 3V to 300V.

• Zener diodes come in a range of power ratings, usually from 500mW to 50W, and they can handle larger reverse current flow than similar PN diodes.

Under ideal conditions, a zener diode's principal role is to sustain a dc voltage that is very close to constant.





Operation:

Forward Biasing:

When Zener diodes are subjected to forward biasing, where the anode voltage exceeds that of the cathode, their behavior closely resembles that of a conventional silicon diode.

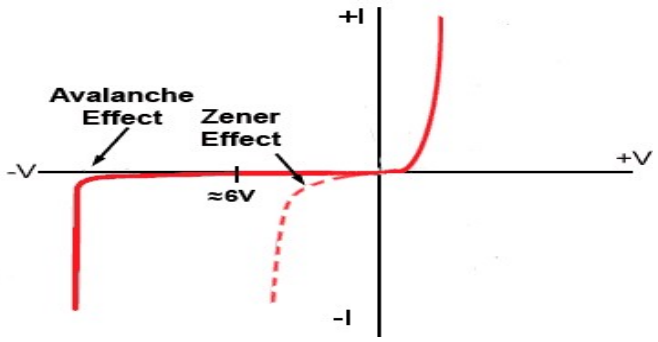
Reverse Biasing:

When subjected to reverse bias, these devices show a significant increase in resistance, resulting in a decrease

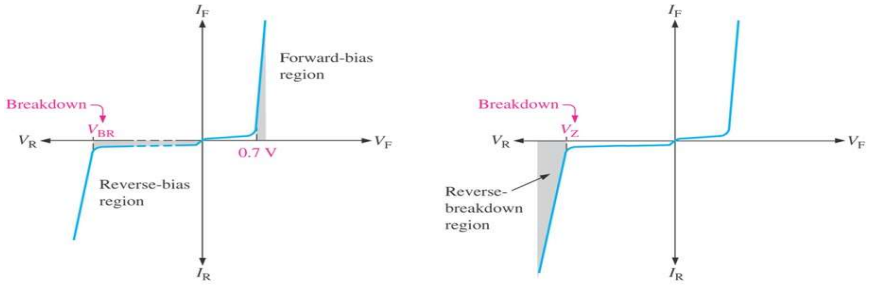
in reverse leakage current. Nevertheless, when a reverse bias attains the magnitude of the reverse breakdown voltage of the diode (also known as the Zener voltage), a prompt decline in resistance and simultaneous surge in current transpire In order to mitigate the risk of surpassing the power rating of the diode and causing its destruction, the Zener diode employs a resistor that is linked in series with the diode. This resistor serves the purpose of constraining the reverse current to a level that is deemed safe.

V – I Characteristics

- The Zener breakdown occurs when the high electric field is applied across the PN junction diode. This results in the flow of electrons across the PN-junction. It is heavily doped P-N junction diode where depletion region is very narrow.
- The Avalanche breakdown happens when a high reverse bias voltage increases the electric field, which further expands up the depletion region.



- **Zener knee:** The characteristic curve of a Zener diode has a pronounced inflection point, sometimes referred to as a sharp curve, at which the diode experiences breakdown upon reaching the breakdown voltage.
- **Zener region:** The region on the characteristic curve of a Zener diode in which breakdown occurs due to the reverse voltage exceeding a certain threshold value.

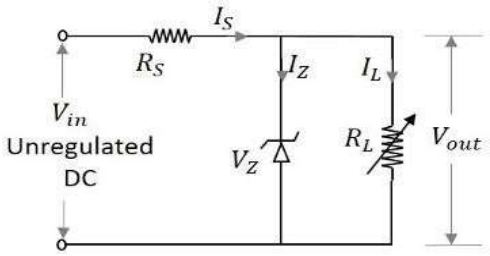


(a) The normal operating regions for a rectifier diode are shown as shaded areas.

(b) The normal operating region for a zener diode is shaded.

Zener Voltage Regulator

- The Zener diode's breakdown or Zener region voltage is almost constant for a big current variation. This makes Zener diode a useful voltage regulator.



Transistor

Sandwiching p- or n-type semiconductors between opposing kinds creates two pn junctions in a transistor. There are two kinds of transistors: (i) n-p-n transistor and (ii) PNP transistor

Fig. (i) shows an n-p-n transistor with two n-type semiconductors separated by a thin p-type portion. However, two p-sections produce a p-n-p transistor.

Note the following for each transistor type:

(i) Two pn junctions. The transistor is just two diodes linked back-to-back.

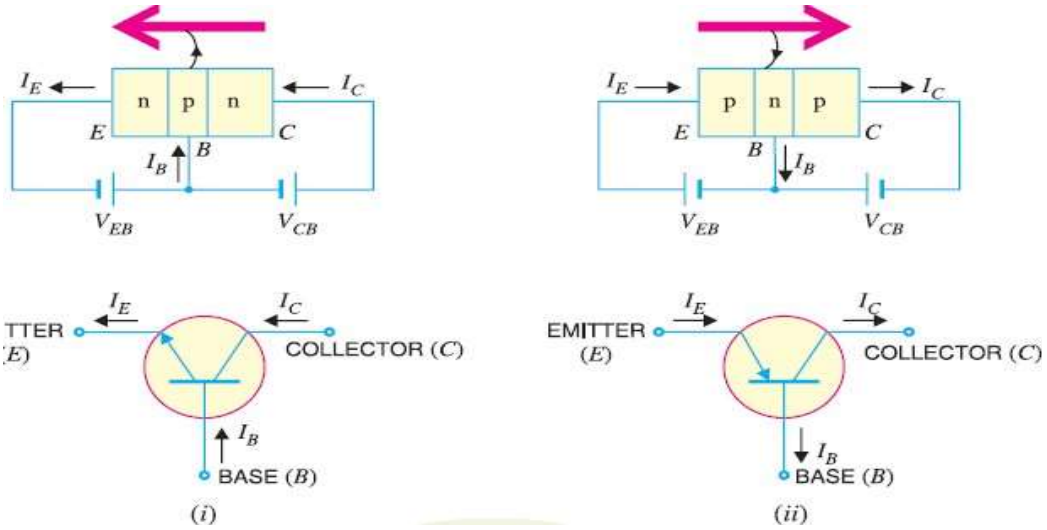
(ii) Three terminals, one from each semiconductor type.

(iii) The middle layer is thin. Transistor function depends most on

this.

Transistor Symbols

Previous diagrams showed transistors diagrammatically. Schematic diagrams illustrate transistors for convenience. See Fig. for npn and pnp transistor symbols.



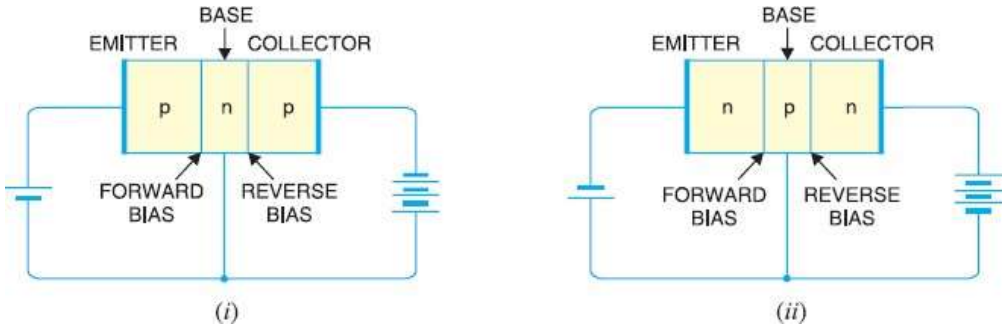
Naming the Transistor Terminals

Pnp and npn transistors have three doped semiconductor regions. One portion is the emitter and the other is the collection. Base, the central part, creates two connections between emitter and collector.

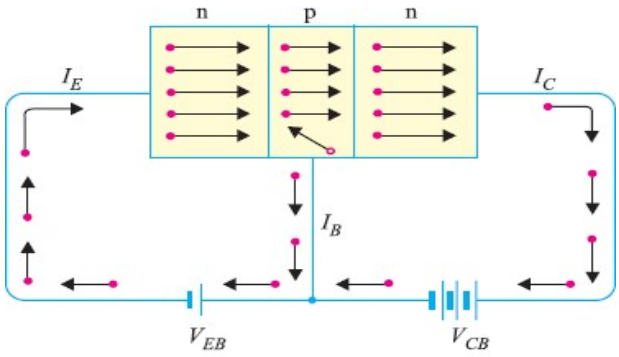
(i) **Emitter.** Electrons or one-way openings are transmitted by emitters. The base-forward biased emitter ensures the presence of a majority carrier count. Forward biased P-type transistor emitters transporting hole charges to base junctions are illustrated in Figure 8.2 (i). When biased forward, the base junction of the npn transistor receives free electrons from its n-type emitter (see Fig. 8.2 (ii)).

(ii) **Collector.** Opposing collectors collect fees. Always reverse-biased collector. Charges are extracted at the base connection. Fig. 8.2 (i) shows hole charges from the output circuit to a pnp transistor's reverse-biased collector (p-type). Under reverse bias, the npn transistor collector (n-type) is accessible to electrons (Figure 8.2 (ii)).

III. **Base.** Base with two pn-junctions between emitter and collector is central. Forward biased base-emitter connections lower emitter circuit resistance. Reverse biasing the base-collector connection increases collector circuit resistance.



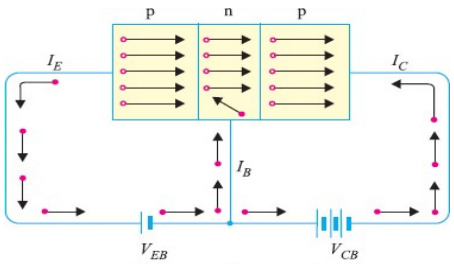
Working of npn transistor. Image of NPN transistor with forward and reverse biases. Forward bias pulls n-type emitter electrons to base. Current-emitting. Holes and electrons mix in p-type bases. Lower than 5% of electrons mix with holes to form base** current IB because to the thin, weakly doped base. To develop collector current IC, over 95% cross collector area. Nearly all emitter current flows in collecting circuit. Add collector and base currents for emitter current.. *i.e.* $I_E=I_C+I_B$



Basic connection of *npn* transistor

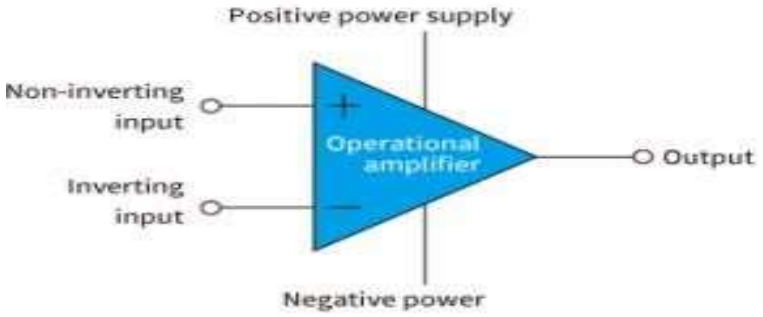
Working of pnp transistor. Fig. depicts the basic pnp transistor connection. BFB pushes p-type emitter holes. IE emitter. In n-type base, holes join electrons. Due to the narrow, poorly doped base, less than 5% of holes couple with electrons. Over 95% produces collector current IC. Collectors carry most emitter current. Pnp transistors use holes to conduct current. Current on external lines needs electrons.

Operational Amplifier (Op – Amps)



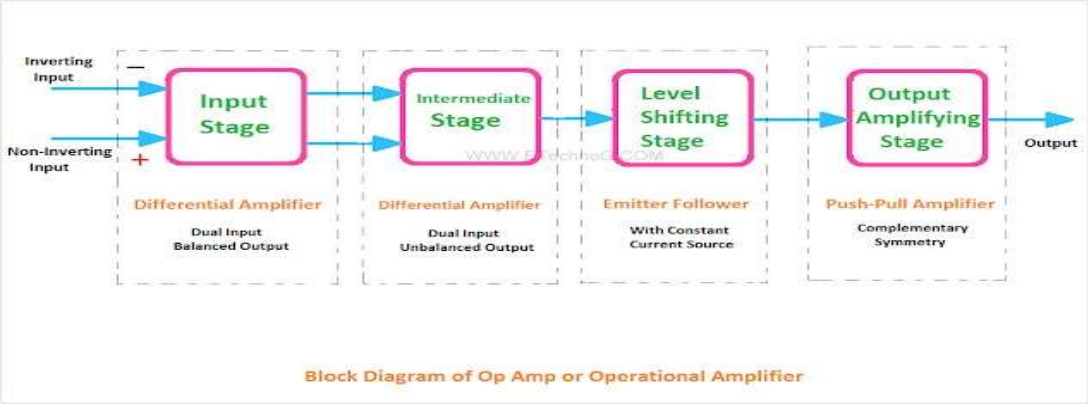
Basic connection of *pnp* transistor

Operational amplifiers, often referred to as ICs, serve the purpose of amplifying weak electrical impulses. Operational amplifiers (op-amps) are electronic devices that are equipped with two input pins and one output pin. The fundamental function of this



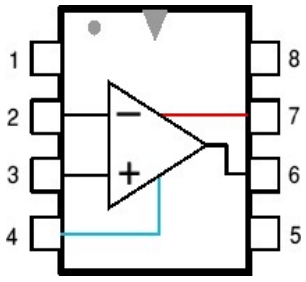
operation is to increase the amplitude of the input signal and subsequently produce an output voltage that represents the difference between the voltages at the input pins.

Basic Block Diagram



Block Diagram of Op Amp or Operational Amplifier

OP-AMP Pin Identification



Pin 1 and Pin 5 : **Offset null input, are used to remove the Offset voltage.**

Pin 2: **Inverting input ($-V_{in}$), signals at this pin will be inverted at output Pin 6.**

Pin 3: **Non-inverting input ($+V_{in}$), signals at pin 3 will be processed without inversion.**

Pin 4: **Negative power supply terminal ($-V_{EE}$).**

Pin 6: **Output (V_{out}) of the Op-Amp**

Pin 7: **Positive power supply terminal ($+V_{CC}$)**

Pin 8: **No connection (N\C), it is just there to make it a standard 8-pin.**

Characteristics of Operational Amplifier

The important characteristics or parameters of an operational amplifier are as follows :

- Open loop voltage gain
- Output offset voltage
- Common Mode Rejection Ratio
- Slew Rate

Common Mode Rejection Ratio (CMRR):

Ability of an Op-Amp to reject a signal applied to both inputs simultaneously. Common Mode Rejection Ratio (CMRR) of an op-amp is defined as the ratio of the closed loop differential gain, Ad and the common mode gain, Ac.

$$CMRR = \frac{A_d}{A_c}$$

Slew Rate (V/μs):

Slew rate of an op-amp is defined as the maximum rate of change of the output voltage due to a step input voltage.

$$SR = Maximum\ of\ \frac{dV_0}{dt}$$

Ideal Op-amp characteristics

- An infinite open loop voltage gain.
- Infinite input impedance.
- Zero output impedance.
- Infinite common mode rejection ratio.
- Infinite bandwidth.
- Zero offset voltage.

Practical op-amp Characteristics

- Input impedance, *Zi* in the order of **Mega ohms**.
- Output impedance, *Z*0

- in the order of **few ohms.**
- Open loop voltage gain, *Av* will be **high**.
- Input impedance, *Zi* should be as high as possible.
- Output impedance, *Z*0 should be as low as possible.
- Open loop voltage gain, *Av* should be as high as possible.
- Output offset voltage should be as low as possible.
- The operating Bandwidth should be as high as possible.
- CMRR should be as high as possible.
- Slew rate should be as high as possible.

Typical OP-AMP Parameters

Parameter	Variable	Typical Ranges	Ideal Values
Open-Loop Voltage Gain	A	10^5 to 10^8	∞
Input Resistance	R_i	10^5 to 10^{13} Ω	∞ Ω
Output Resistance	R_o	10 to 100 Ω	0 Ω
Supply Voltage	Vcc/V^+ $-Vcc/V^-$	5 to 30 V -30V to 0V	N/A N/A

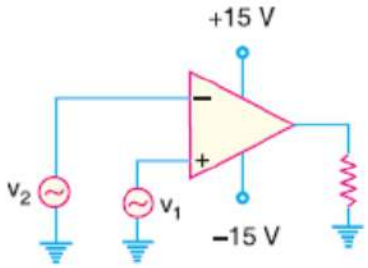
Linear Applications of OP-AMP

There are many applications of an OP-AMP.

1. Voltage Adder (Summing Amplifier)
2. Difference Amplifier
3. Integrator
4. Differentiator
5. Comparator
6. Voltage Follower & etc…

Comparators

Often we want to compare one voltage to another to see which is larger. In this situation, a *comparator* may be used. *A comparator is an OP-amp circuit without negative feedback* and takes advantage of very high open-loop voltage gain of OP-amp. A comparator has two input voltages (noninverting and inverting) and one output voltage. Because of the high open-loop voltage gain of an *OP*-amp, a very small difference voltage between the two inputs drives the amplifier to saturation. For example, consider an *OP*-amp having *AOL* = 100,000. A voltage difference of only 0.25 mV between the inputs will produce an output voltage of (0.25 mV) (100,000) = 25V. However, most of OP-amps have output voltages of less than ± 15V because of their d.c. supply voltages. Therefore, a very small differential input voltage will drive the OP-amp to saturation. This is the key point in the working of comparator. Fig. 25.93 illustrates the action of a comparator. The input voltages are *v*1 (signal) and *v*2 (*reference voltage). If the differential input is positive, the circuit is driven to saturation and output goes to maximum positive value (**+*Vsat* = + 13V). Reverse happens when the differential input goes negative *i.e.* now output is maximum negative (– *Vsat* = – 13V). This circuit is called comparator because it compares *v*1 to *v*2 to produce a saturated positive or negative output voltage. Note that output voltage rapidly changes from – 13V to + 13V and *vice-versa*.



Comparator Circuits

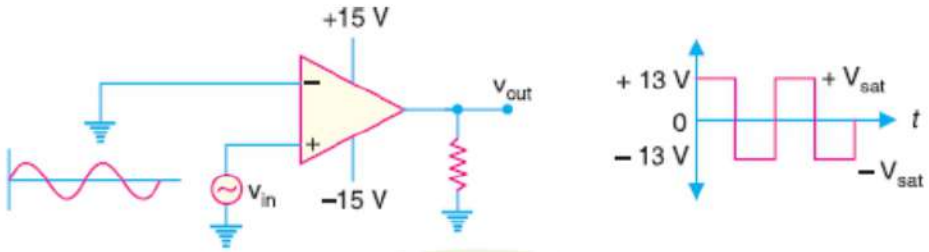
A comparator circuit has the following two characteristics :

(i) It uses no feedback so that the voltage gain is equal to the open-loop voltage gain (*AOL*) of *OP*-amp.

(ii) It is operated in a non-linear mode.

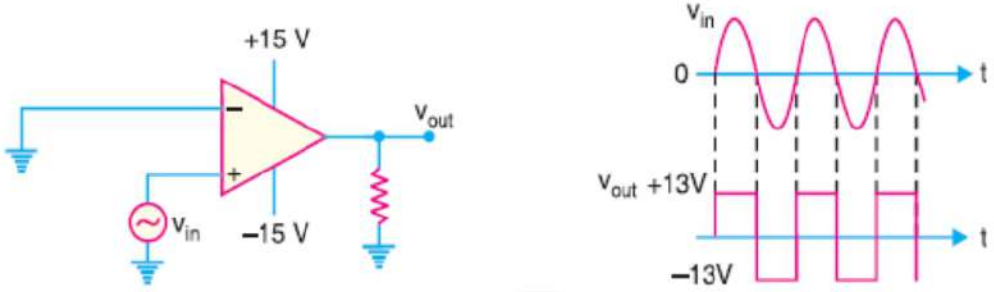
These properties of a comparator permit it to perform many useful functions.

1. As a square wave generator. A comparator can be used to produce a square wave output from a sine wave input. Fig. 25.94 shows the circuit of a comparator to produce square wave output. Note that inverting terminal (–) is grounded and signal (*vin*) is applied to the noninverting terminal (+). Since the gain of a comparator is equal to *AOL*, virtually any difference voltage at the inputs will cause the output to go to one of the voltage extremes (+ *Vsat* or – *Vsat*) and stay there until the voltage difference is removed. The polarity of the input difference voltage will determine to which extreme (+*Vsat* or – *Vsat*) the output of the comparator goes.



When the input signal goes positive, the output jumps to about + 13 V. When the input goes negative, the output jumps to about – 13 V. The output changes rapidly from – 13 V to + 13 V and *vice-versa*. This change is so rapid that we get a square wave output for a sine wave input.

2. As a zero-crossing detector. When one input of a comparator is connected to ground, it is known as zero-crossing detector because the output changes when the input crosses 0 V. The zerocrossing circuit is shown in Fig. 25.95. The input and output waveforms are also shown. When the input signal is positive-going, the output is driven to positive maximum value (*i.e.* + *Vsat* = + 13 V). When the input crosses the zero axis and begins to go negative, the output is driven to negative maximum value (*i.e.* – *Vsat* = – 13 V).

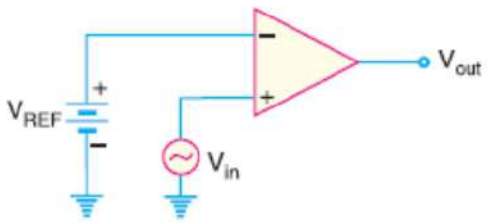


From the input/output waveforms, you can see that every time the input crosses 0 V going positive, the output jumps to + 13 V. Similarly, every time the input crosses 0 V going negative, the output jumps to – 13 V. Since the change (+ 13 V or – 13 V) occurs every time the input crosses 0 V, we can tell when the input signal has crossed 0 V. Hence the name zero-crossing detector.

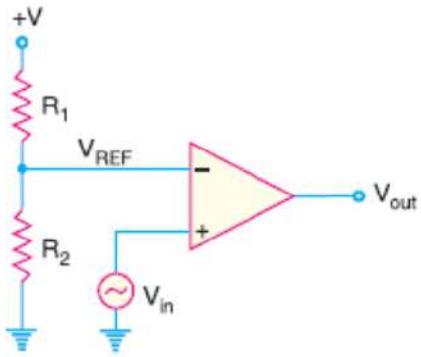
3. As a level detector. When a comparator is used to compare a signal amplitude to a fixed d.c. level (reference voltage), the circuit is referred to as a level detector. We can modify zerocrossing detector circuit to construct level detector. This can be done by connecting a fixed reference voltage V_{REF} to the inverting input as shown in Fig. 25.96 (*i*). A more practical arrangement is shown in Fig. 25.96 (*ii*) using a voltage divider to set the reference voltage as follows :

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V)$$

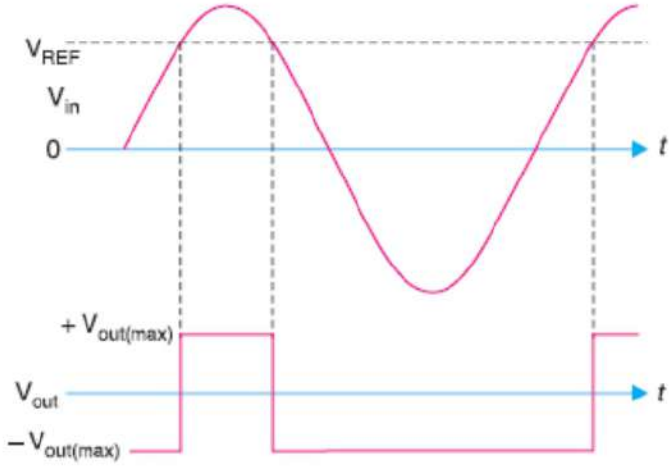
where + V is the positive OP-amp d.c. supply voltage.



(*i*) Battery reference



(*ii*) Voltage-divider reference



(*iii*) Waveforms

The circuit action is as follows. Suppose the input signal *vin* is a sine wave. When the input voltage is less than the reference voltage (*i.e. Vin < VREF*), the output goes to maximum negative level. It remains here until *Vin* increases above *VREF*. When the input voltage exceeds the reference voltage (*i.e. Vin > VREF*), the output goes to its maximum positive state. It remains here until *Vin* decreases below *VREF*. Fig. 25.96 (*iii*) shows the input/output waveforms. Note that this circuit is used for non zero-level detection.

ANALOG TO DIGITAL CONVERTOR

Definition:

An electronic integrated circuit which converts a signal from analog (continuous and can take an inifinity of values) to digital (discrete digital data) form. Provides a link between the analog world of transducers and the digital world of signal processing and data handling.

FLASH TYPE ADC

Flash type ADC produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest ADC. The circuit diagram of a 3-bit flash type ADC is shown in the following figure

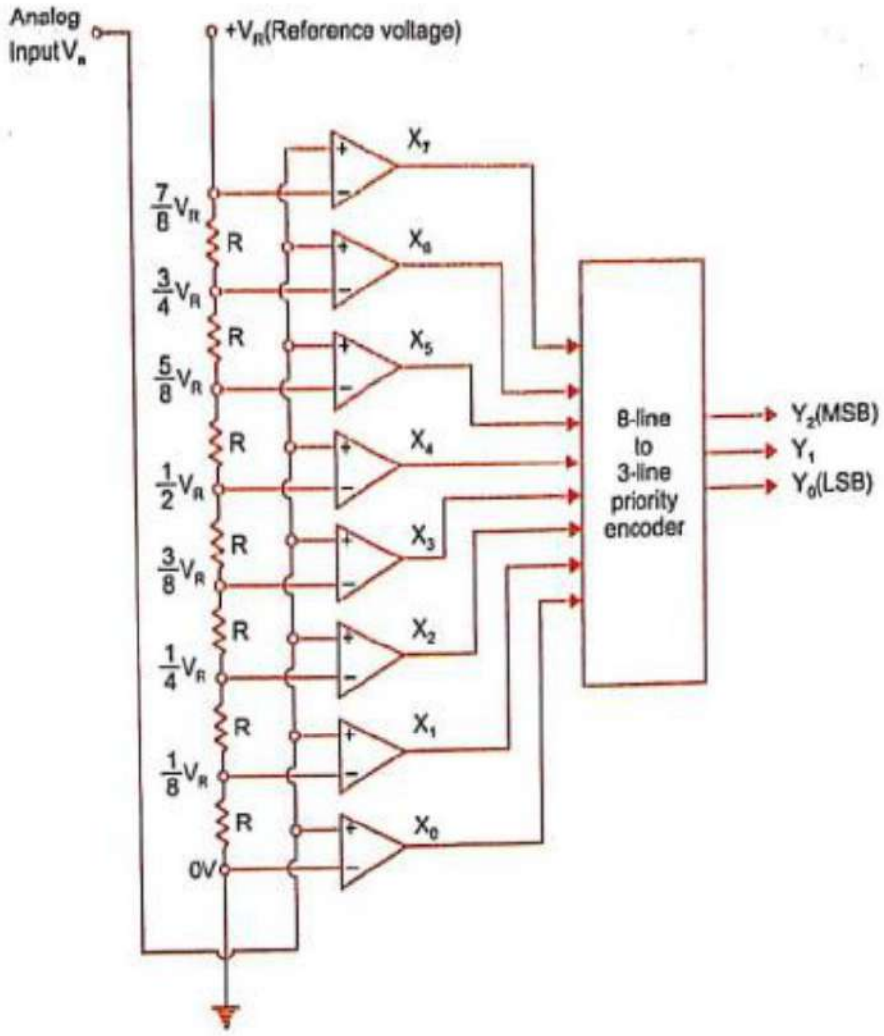


Figure 4.6.1.Basic circuit for flash type A/D converter

The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

The working of a 3-bit flash type ADC is as follows.

• The voltage divider network contains 8 equal resistors. A reference voltage VR is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of VR8VR8.

• The external input voltage Vi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.

• At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator parallelly.

• The output of the comparator will be '1' as long as Vi is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, Vi is less than or equal to the voltage drop present at the respective other input terminal.

• All the outputs of comparators are connected as the inputs of priority encoder.This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.

• Therefore, the output of priority encoder is nothing but the binary equivalent (digital output) of external analog input voltage, Vi

The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

Advantages

- Simplest in terms of operational theory
- Most efficient in terms of speed, very fast
- limited only in terms of comparator and gate propagation delays

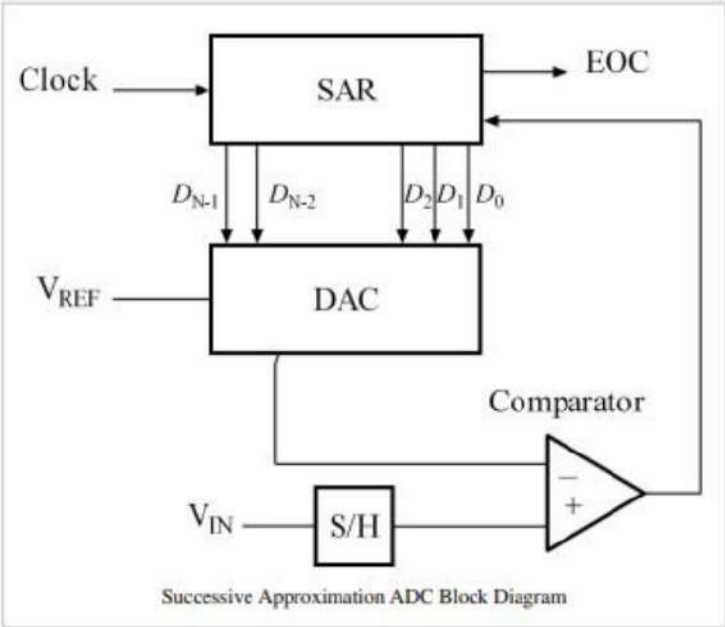
Disadvantages

- Lower resolution
- Expensive
- Large Power Consumption
- For each additional output bit, the number of comparators is doubled
  i.e. for 8 bits, 256 comparators needed

Successive Approximation type ADC

A successive approximation ADC is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

Successive Approximation ADC Circuit



Successive Approximation ADC Block Diagram

Elements:

- DAC = Digital to Analog Converter
- EOC = End of Conversion
- SAR = Successive Approximation Register
- S/H = Sample and Hold Circuit
- V_{in} = Input Voltage
- Comparator
- V_{ref} = Reference Voltage

Algorithm

The successive-approximation analog-to-digital converter circuit typically consists of four chief subcircuits:

1. A sample-and-hold circuit to acquire the input voltage V_{in}.
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive-approximation register (SAR).

3. A successive-approximation register subcircuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that, for comparison with V_{ref}, supplies the comparator with an analog voltage equal to the digital code output of the SAR_{in}.

Operation -

- The output of SAR is converted to analog out by the DAC and this analog output is compared with the input analog sampled value in the Op-Amp comparator.
- This Op-Amp provides a high or low clock pulse based on the difference through the logic circuit.
- In very first case the 3-bit SAR enables its MSB bit as high i.e. '1' and the result will be "100".
- This digital output is converted to analog value and compared with input sampled voltage (Vin).
- If the deference is positive i.e. if the sampled input is high, then the SAR enables the next bit from MSB and result will be "110".
- Now if the output is negative i.e. if the input sampled voltage is less than the SAR resets the last set bit and sets the next bit and resultant output in this case will be "101" which will definitely approximately equal to the input analog value.
- The counting sequence is explained by the following counter flow chat as shown in below.

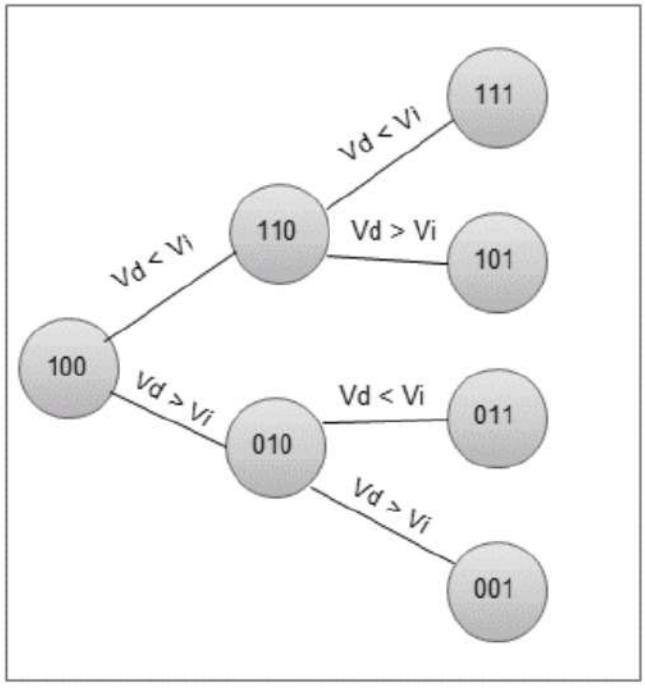


Figure- Successive Approximation ADC Counter Flow Chart

Conversion time of Successive Approximation ADC -

By observing above 3-bit example, it is illustrated for a 3-bit ADC the conversion time will be 3 clock pulses.

Then, N bit Successive Approximation ADC conversion time = 3T (T- clock pulse). So to avoid aliasing effect the next sample of input signal should be taken after 3 clock pulses.

Advantages

- Capable of high speed and reliable
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost
- Capable of output the binary number in serial (one bit at a time) format.
- High resolution
- No precision external components needed

Disadvantages -

- Cost is high because of SAR
- Complexity in design
- Applications

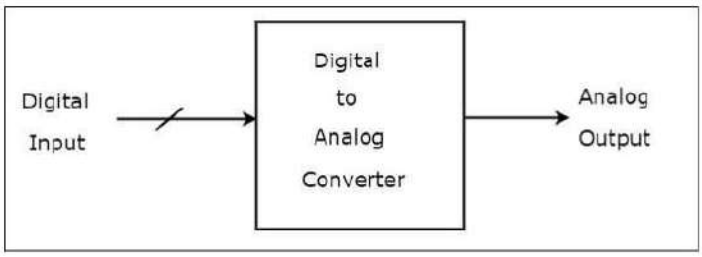
Applications -

- The SAR ADC is used widely data acquisition techniques at the sampling rates higher than 10KHz.

Digital to Analog Converters

A **Digital to Analog Converter (DAC)** converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. This chapter deals with Digital to Analog Converters in detail.

The **block diagram** of DAC is shown in the following figure –



A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output. In general, the **number of binary inputs** of a DAC will be a power of two.

Types of DACs

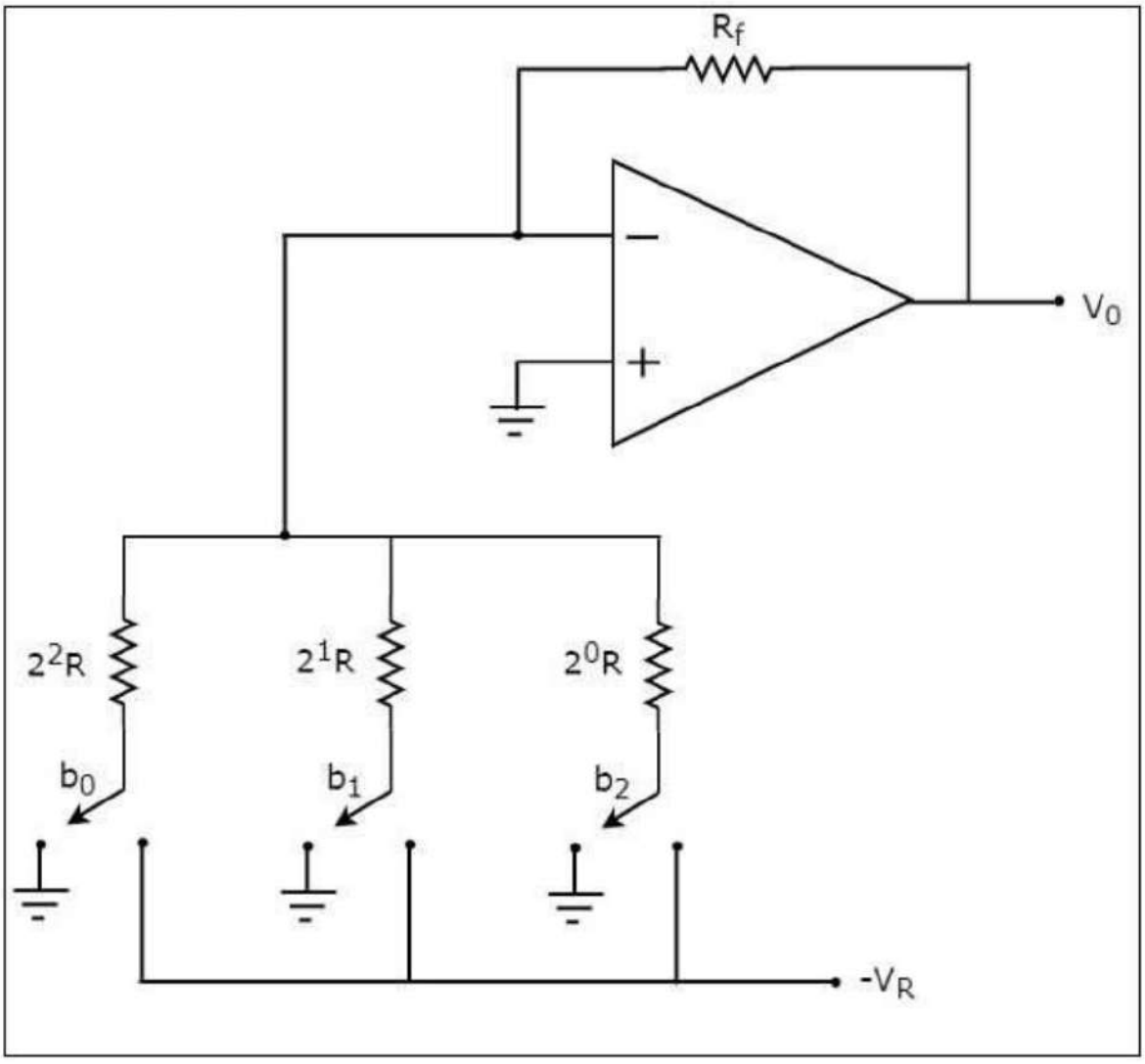
There are **two types** of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC

Weighted Resistor DAC

A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using **binary weighted resistors** in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC.

The **circuit diagram** of a 3-bit binary weighted resistor DAC is shown in the following figure –



Recall that the bits of a binary number can have only one of the two values. i.e., either 0 or 1. Let the 3-bit binary input is b2b1b0. Here, the bits b2 and b0 denote the Most Significant Bit (MSB) and Least Significant Bit (LSB) respectively.

The digital switches shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in the above figure will be connected to the negative reference voltage, −VR when the corresponding input bits are equal to '1'.

In the above circuit, the non-inverting input terminal of an op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of op-amp.

According to the virtual short concept, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal's node will be zero volts.

The nodal equation at the inverting input terminal's node is:

$$\frac{0+V_R b_2}{2^0 R}+\frac{0+V_R b_1}{2^1 R}+\frac{0+V_R b_0}{2^2 R}+\frac{0-V_0}{R_f}=0$$

$$=>\frac{V_0}{R_f}=\frac{V_R b_2}{2^0 R}+\frac{V_R b_1}{2^1 R}+\frac{V_R b_0}{2^2 R}$$

$$=> V_0=\frac{V_R R_f}{R}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

Substituting, $R=2R_f$ f in above equation.

$$=> V_0=\frac{V_R R_f}{2R_f}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

$$=> V_0=\frac{V_R}{2}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

The above equation represents the output voltage equation of a 3-bit binary weighted resistor DAC. Since the number of bits are three in the binary (digital) input, we will get seven possible values of output voltage by varying the binary input from 000 to 111 for a fixed reference voltage, VR.

We can write the generalized output voltage equation of an N-bit binary weighted resistor DAC as shown below based on the output voltage equation of a 3-bit binary weighted resistor DAC.

$$=> V_0 = \frac{V_R}{2}\left\{\frac{b_{N-1}}{2^0} + \frac{b_{N-2}}{2^1} + \ldots + \frac{b_0}{2^{N-1}}\right\}$$

Advantages:

- Easy principle/construction
- Fast conversion

Disadvantages

- The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.
- It is difficult to design more accurate resistors as the number of bits present in the digital input increases.

R-2R Ladder DAC

The R-2R Ladder DAC overcomes the disadvantages of a binary weighted resistor DAC. As the name suggests, R-2R Ladder DAC produces an analog output, which is almost equal to the digital (binary) input by using a **R-2R ladder network** in the inverting adder circuit.

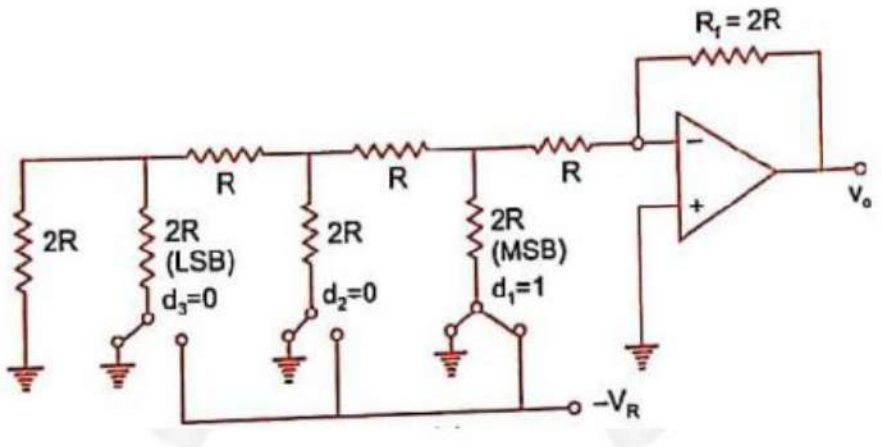


Figure 4.3.2. R-2R Ladder DAC

R-2R Ladder DAC is shown in figure 4.3.2.Wide range of resistors are required in binary weighted resistor. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. The values of R ranges from 2.5kΩ to 10kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 5.1.2(a), where the switch position $d1$ $d2$ $d3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 5.1.2(b) and finally to Fig. 5.1.2(c). then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R \frac{2}{3}R}{2R + \frac{2R}{3}} = \frac{-V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{4} = \frac{V_{FS}}{2}$$

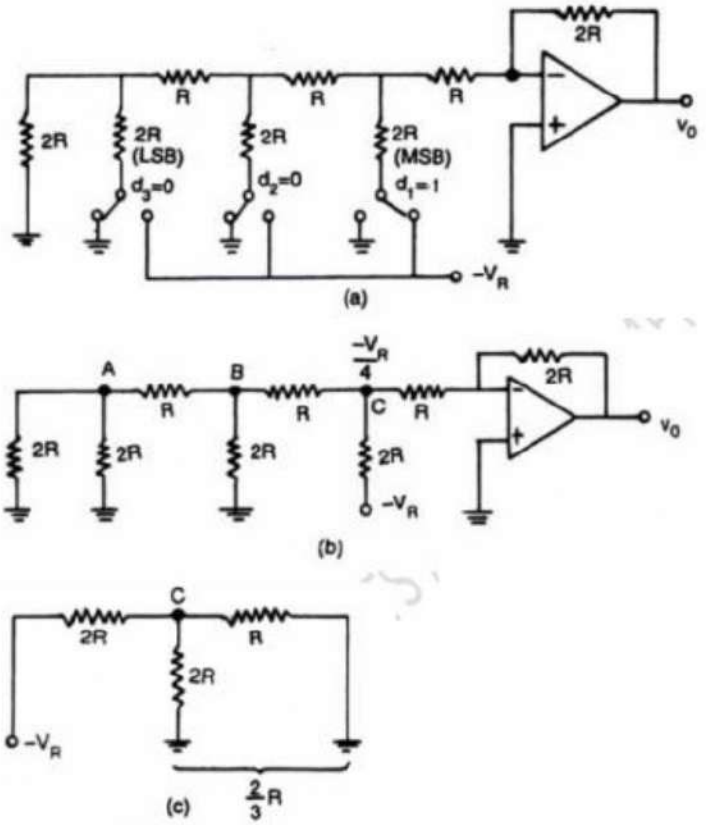


Fig. 5.1.2(a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 5.1.3(a). The circuit can be simplified to the equivalent form of Fig. 5.1.3(b). The voltages at the nodes (A,B,C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_o = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

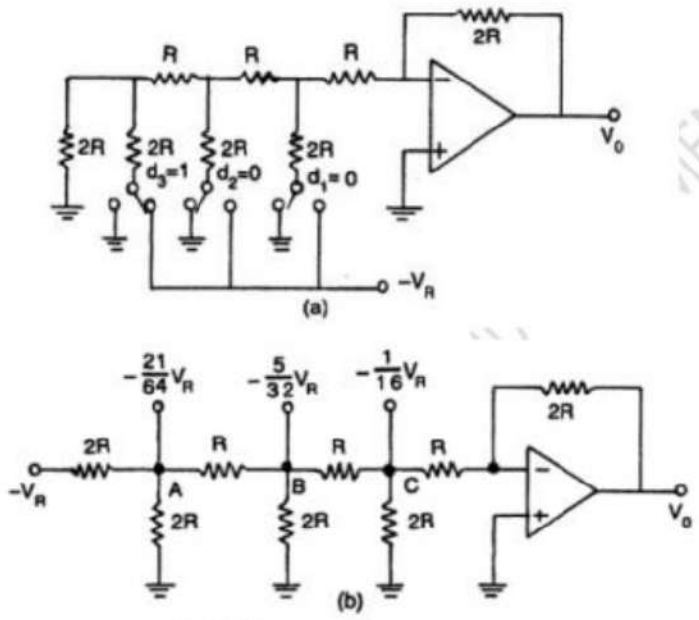


Fig. 5.1.3(a) R-2R ladder DAC for switch positons 001 (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

Advantages:

- Only two resistor values
- Does not need as precision resistors as Binary weighted DACs
- Cheap and Easy to manufacture

Disadvantages:

- Slower conversion rate