EE517: ANALOG VLSI LAB
Experiment 8

Design a fully differential folded cascode single-stage opamp

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EEE - VLSI & Nanoelectronics

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1 OBJECTIVE

To find W/L, gain bandwidth product, output swing, ICMR, and compare the practical and theoretical results.

1.1 Design Specification:

Maximum output swing, maximum gain, higher bandwidth and lower power consumption with a suitable aspect ratio

1. Target gain is =2000
2. Differential output swing =1.8v
3. Power dissipation <= 0.12 µW
4. CL = 10pF
5. Technology=180 nm
6. VDD= 1.8V

1.2 Observations

1.2.1 DC Analysis

• Report the schematic of the diff pair with DC OP point annotated: Id, Vgs, Vds, Vth, Vdsat, gm, gds, gmb, region.
• Check that all transistors operate in saturation

1.2.2 AC Analysis

• Observe pole-zero analysis of your circuit.
• Frequency response of your circuit.
• Find Av, PM, Bandwidth, CMRR, PSRR.
• Give a proper reason for selecting any value of any parameter.

1.2.3 Transient Analysis

• Slew rate.
• ICMR, OCMR.

2 Theory

2.1 Fully differential folded cascode single-stage opamp

To eliminate the disadvantages of earlier topologies, folded cascade op-amps are used. The folded structure offers greater flexibility in voltage levels as it eliminates the need to stack the cascode transistor on top of the input device. Folded cascode op-amps exhibit single-pole settling behavior at high unity gain frequencies.Basically two-stage cascode op-amp circuits are mostly used in designing of circuits where there is a requirement of high gain and high output impedance. But the performance can be even better if folded cascode is used.

Furthermore we know that the input signal of a common-gate(CG) stage is current and transistor in common-source(CS) stage converts voltage into current. Thus, the topology in which the CS stage is cascaded with CG stage, it is referred as "cascode" topology

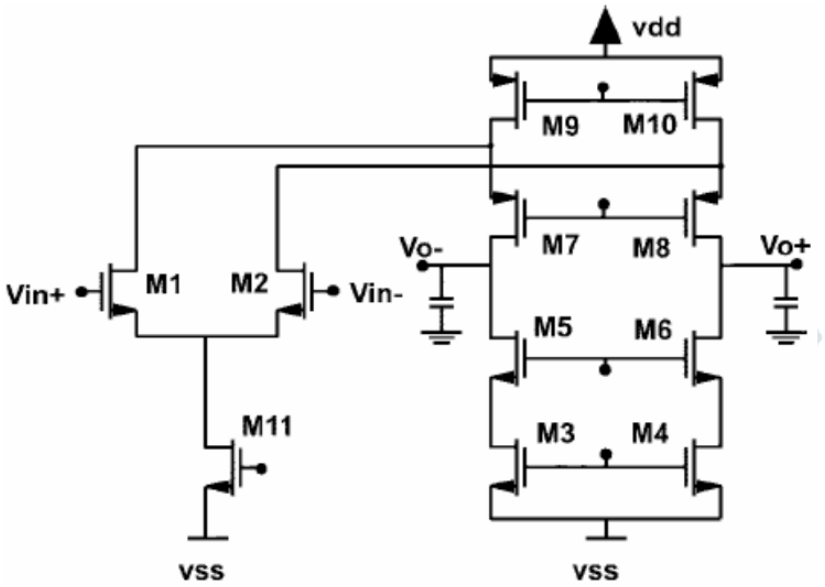

Figure 1: 2 stage OP AMP

$$Gain = gm_1 * [(gm_5 * r_o5 * r_o3)||(gm_7 * (r_o7 * (r_o||r_o1))] \quad (1)$$

2.2 Operation

- Here transistor M1 generates small signal drain current proportional to Vin and transistor M2 links or routes this current to resistance RD. The transistor M1 is known as input device and both of them carry equal current[11].

- Folded cascode op-amp provides improves the ICMR and PSRR to a decent level. The FCOA uses cascading at the output stage combined with differential amplifier ,that results in achieving good ICMR. Folded cascode op-amp provides larger output swing than the ordinary conventional telescopic amplifier but it consumes twice the current than the telescopic. Because of large output swing, the input and output are shorted so that it becomes much convenient and easier for selection of input common-mode level.

- Folded cascode op-amp possess a very important property i.e. it allows the input common-mode level close or nearer to supply voltage. With PMOS input, the input common-mode level can be lower to 0V while one with NMOS input it can reach to supply voltage VDD. As compared to ordinary op-amp, folded cascode provides high gain with large output swing and is a single-pole op-amp. The major advantage of single-pole op-amp is that it provides great stability and large phase margin [16].

3 Parameters to be measured

3.1 Slew Rate

For a large input step voltage, some transistors in the op-amp may be driven out of their saturation regions or completely cut-off. As a result the output will follow the input at a slower finite rate. The maximum rate of change dVo/dt is called slew rate.
General formula for slew rate is

$$slewrate = (\frac{dV_{out}}{dt})_{max} \tag{2}$$

3.2 ICMR

ICMR means nothing but Input the common mode range.In general, it is defined as the range of common mode inputs that can be applied to that circuit while keeping all transistors saturated.Maximum ICMR refers to the maximum common mode input values that can be applied.

3.3 GBWP

Gain Band Width Product ,of an amplifier ,product of Open Loop gain times frequency range at which amplifier gain attenuated to -20dB.

3.4 CMRR

The Common-Mode Rejection Ratio (CMRR) indicates the ability of a differential amplifier to suppress signals common to the two inputs. Desired signals should appear on only one input or with opposite polarities on both inputs. These desired signals are amplified and appear on the outputs.

3.5 PSRR

The power supply rejection ratio (PSRR) describes the ability of a circuit to suppress any power supply variations from passing to its output signal and is typically measured in dB.

4 CIRCUIT DIAGRAM

4.1 DC ANALYSIS

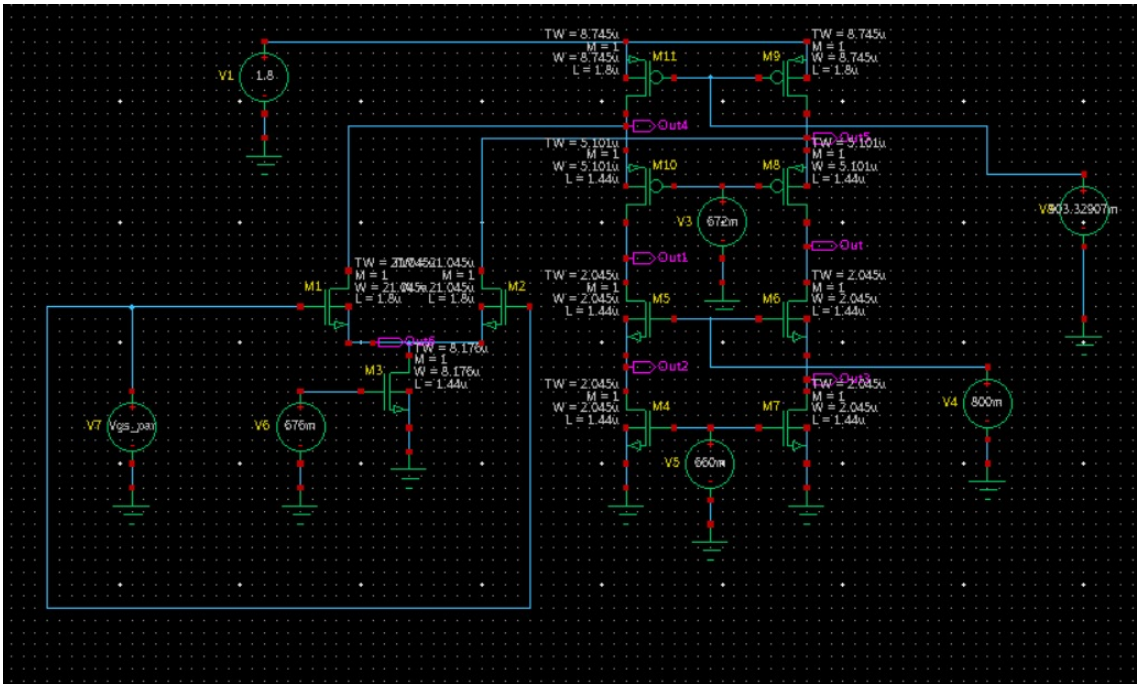

Figure 2: DC analysis schematic

4.2 AC ANALYSIS

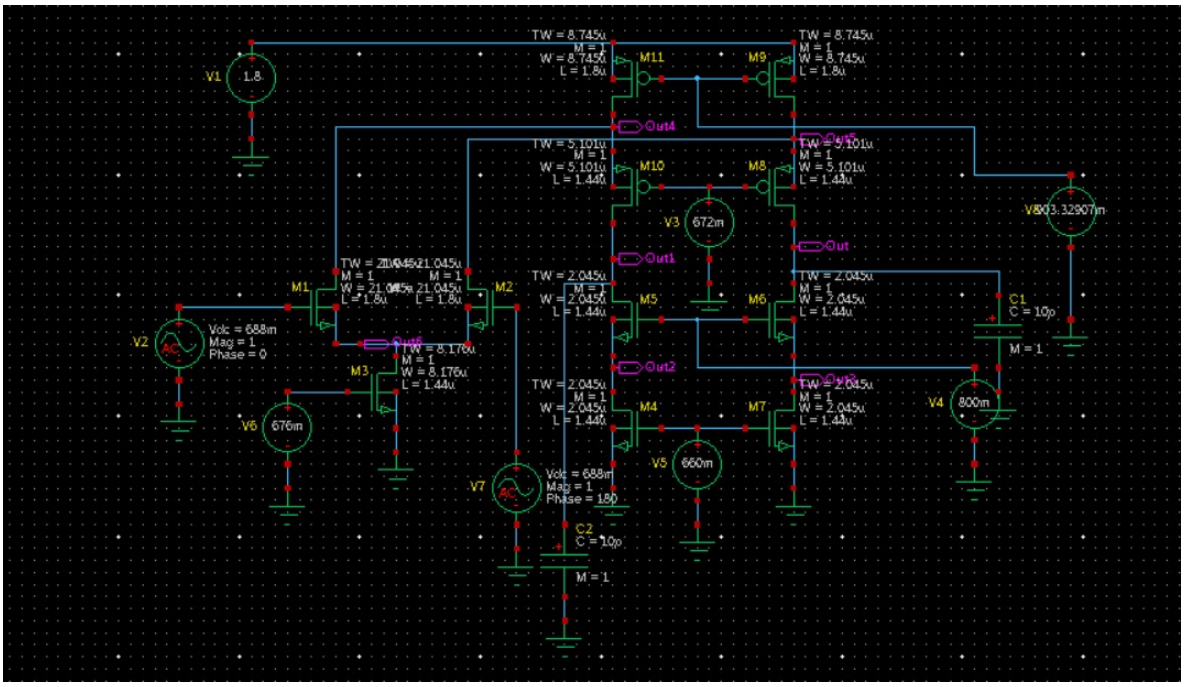

Figure 3: AC analysis schematic

5 SIMULATION RESULTS

5.0.1 DC Analysis

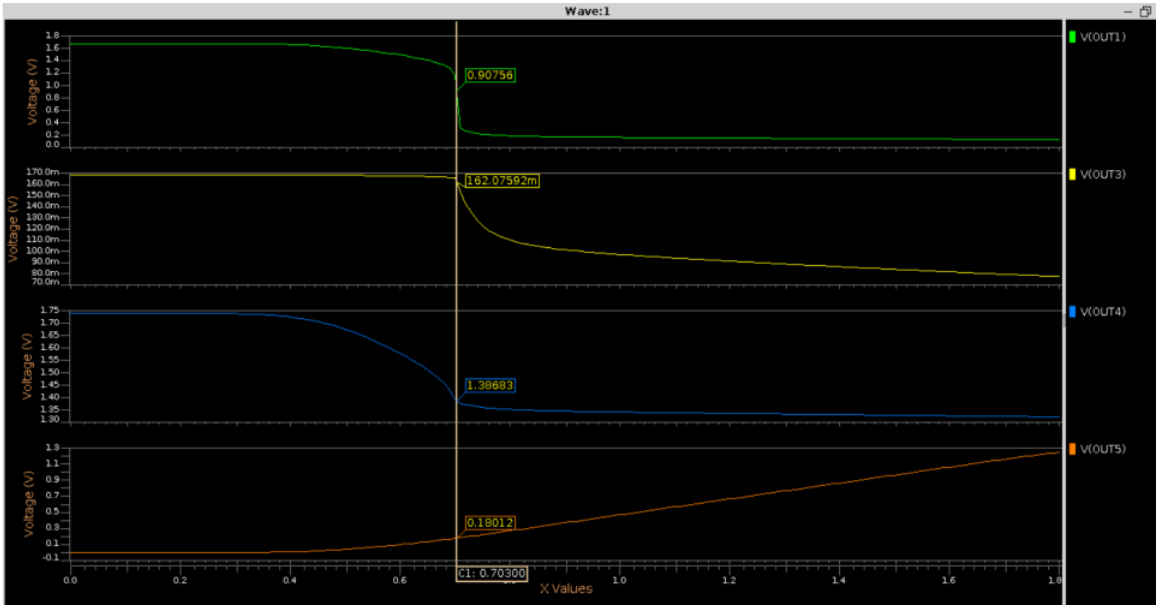

Figure 4: graph of dc analysis of 2-stage op-amp

5.0.2 AC analysis

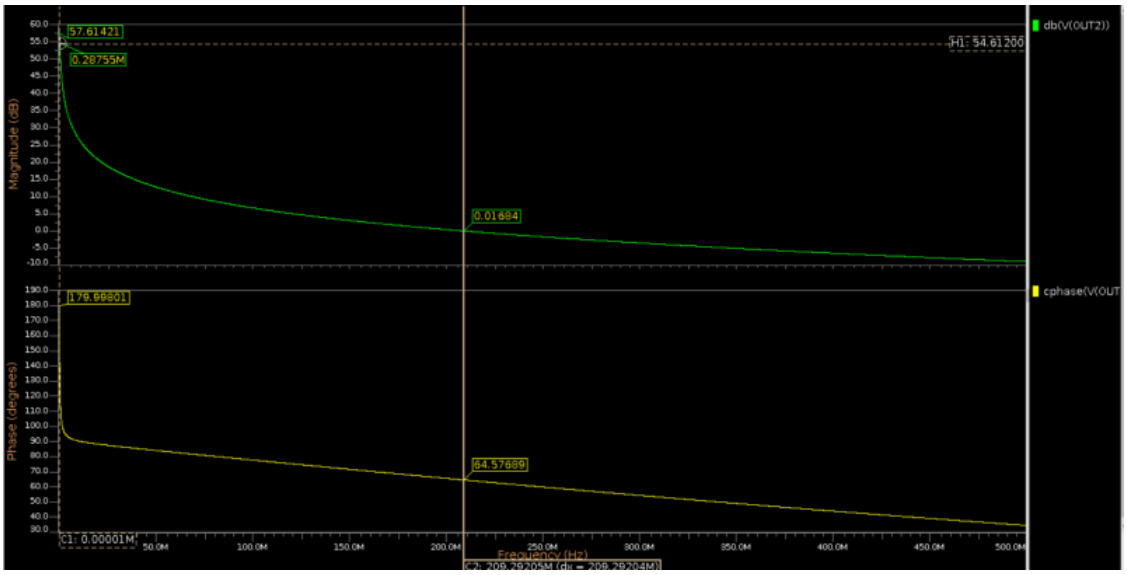

Figure 5: AC analysis gain

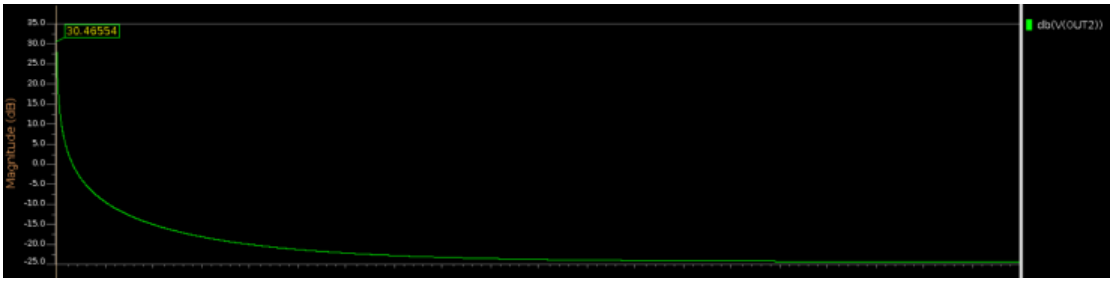

Figure 6: Common Mode gain

5.0.3 PSRR

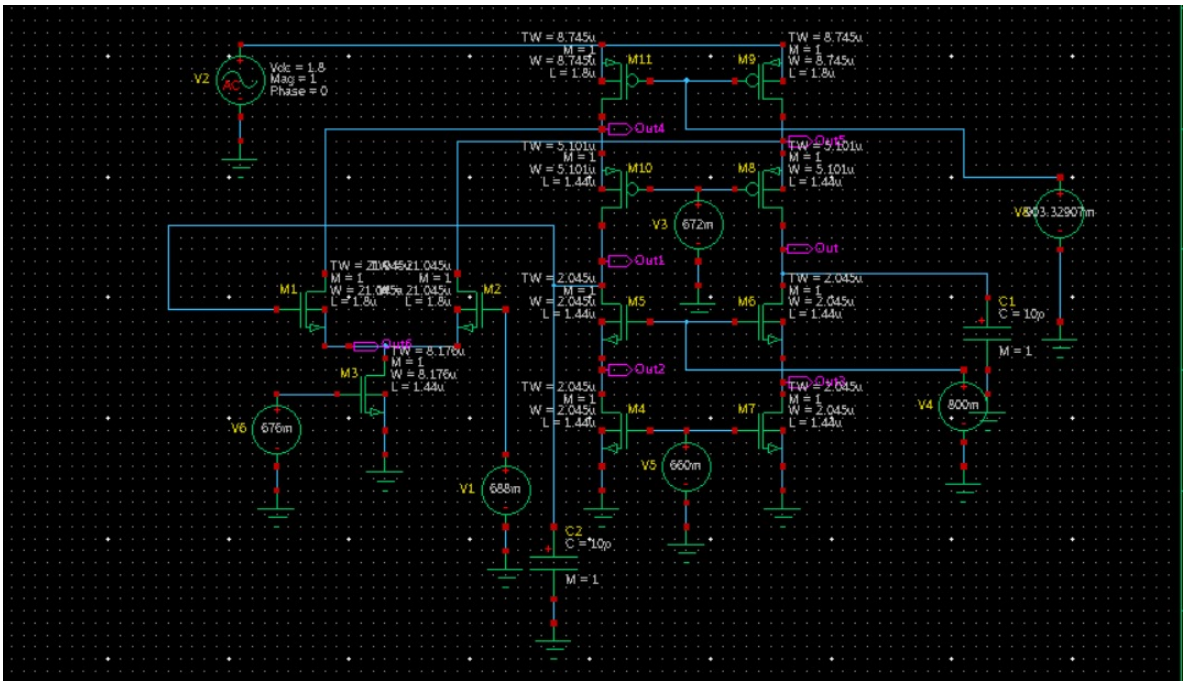

Figure 7: schematic of PSRR analysis

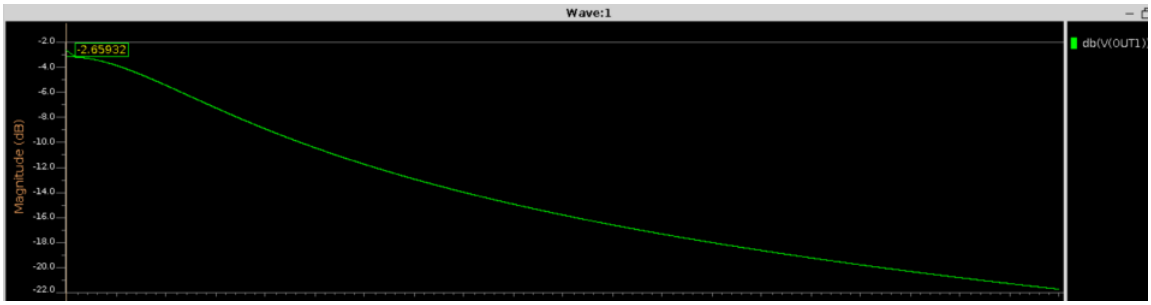

Figure 8: PSRR

5.0.4 Transient Analysis

5.0.5 Slew Rate

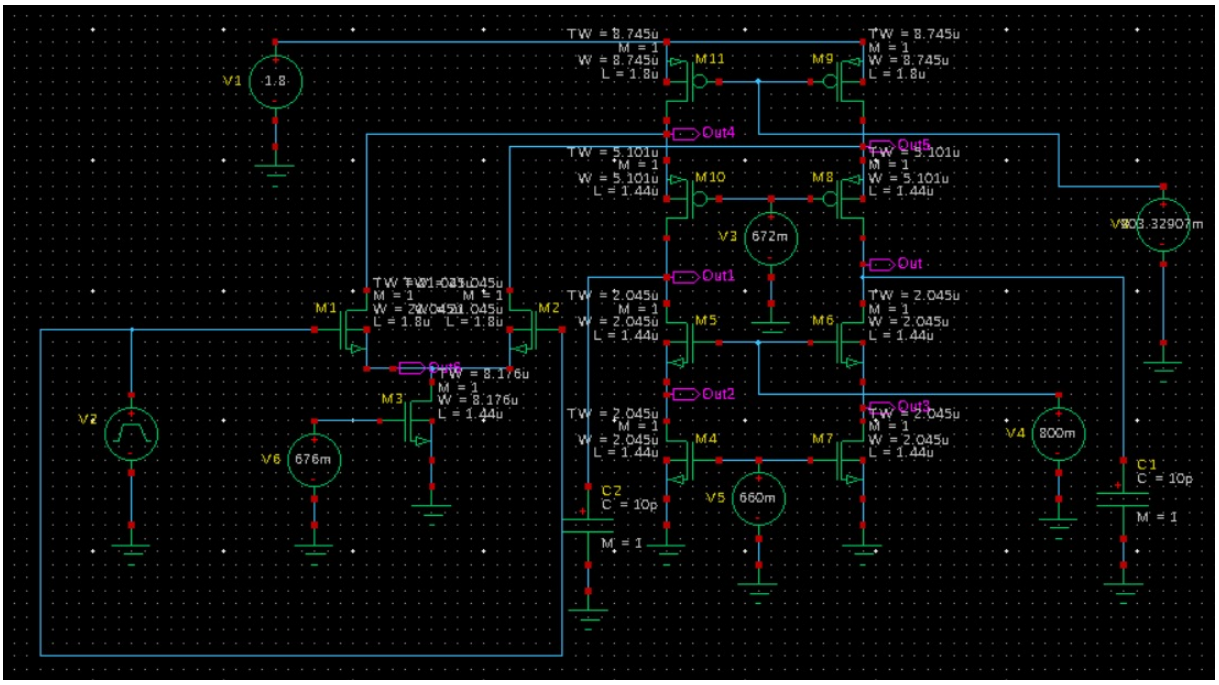

Figure 9: schematic for slew rate

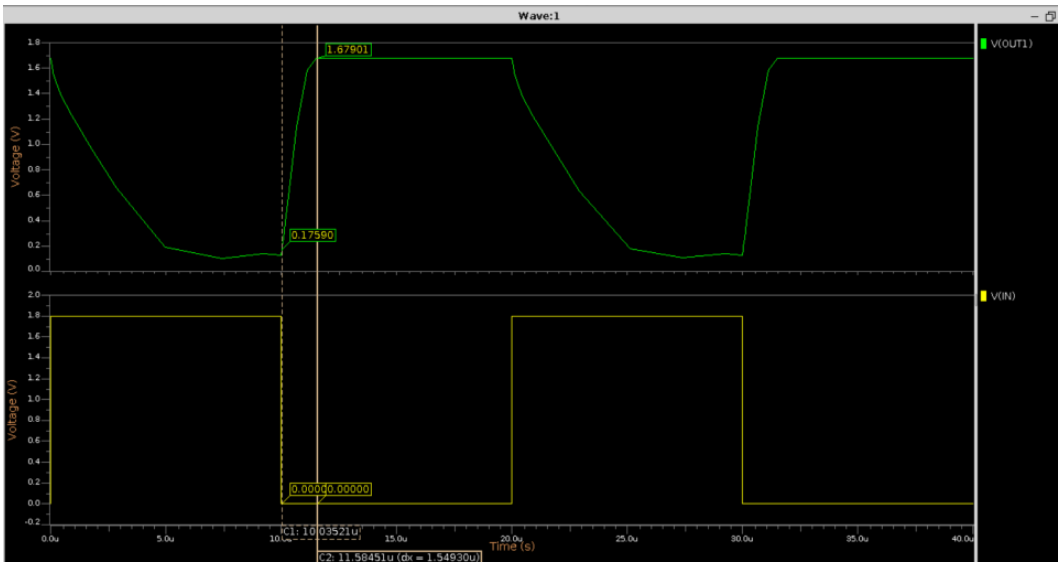

Figure 10: slew rate

5.0.6 ICMR and OCMR

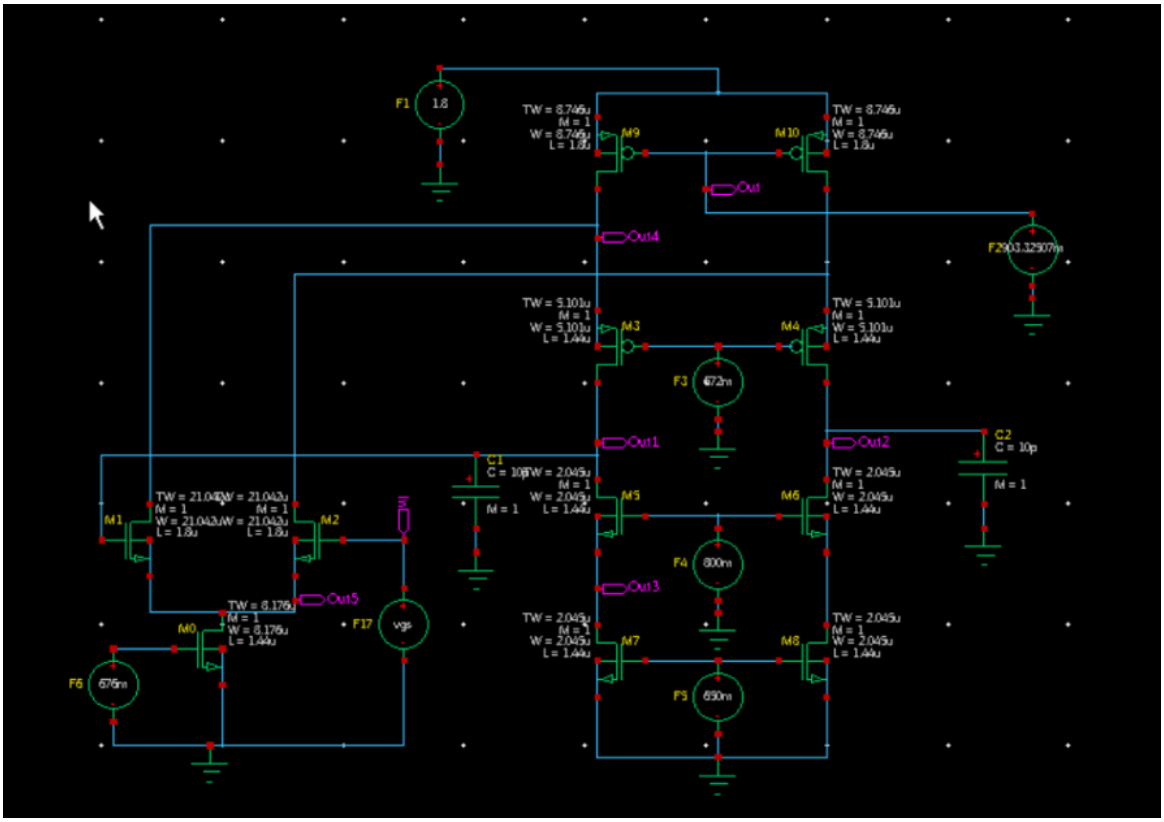

Figure 11: schematic for ICMR/OCMR

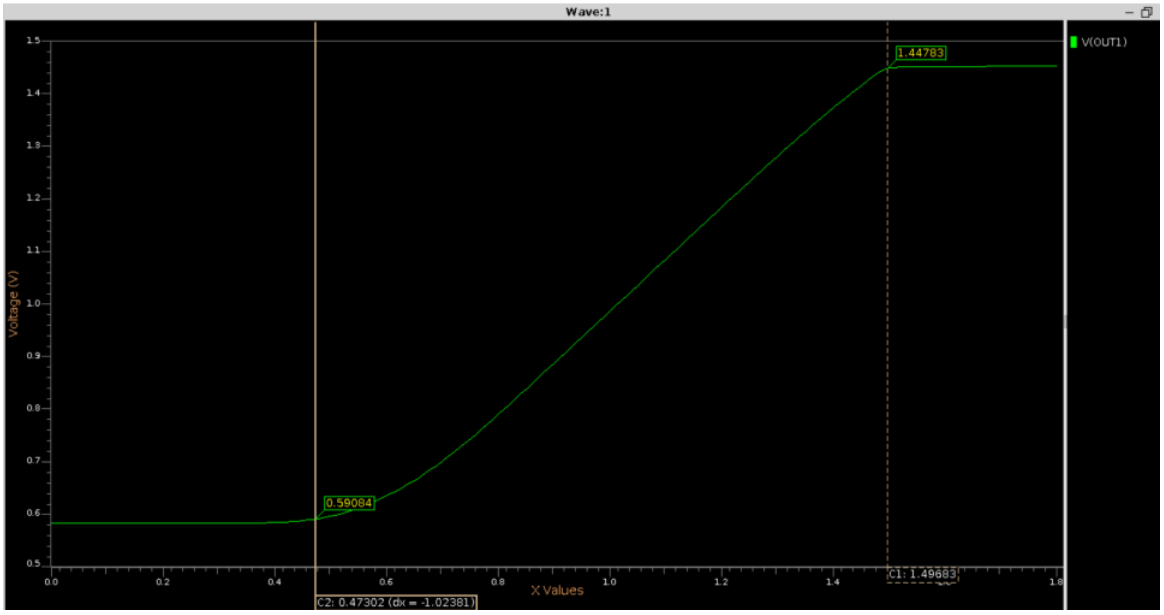

Figure 12: ICMR/OCMR

6 RESULTS

6.1 (W/l) of all transistors

Transistor	aspect ratio	width	length
M1	5.82	1440 nm	8176 nm
M2	11.65	1800 nm	21042 nm
M3	11.65	1800 nm	21042 nm
M4	3.64	1440 nm	5241 nm
M5	3.64	1440 nm	5241 nm
M6	1.456	1440um	2104 nm
M7	1.456	1440um	2104 nm
M8	1.456	1440um	2104 nm
M9	1.456	1440um	2104 nm
M10	4.865	1800 nm	8737 nm
M11	4.865	1800 nm	8737 nm

6.2 Bias voltages of transistors

transistor	Theoretical VG	practical VG	VGS	VDS	ID
M1	0.75	0.676v	0.676	0.18	41.502 µA
M2	0.85v	0.703v	0.523v	1.206	20.752 µA
M3	0.85v	0.703v	0.523v	1.206	20.752 µA
M4	0.75v	0.672v	-0.714v	-0.479	-8.463 µA
M5	0.75v	0.672v	-0.714v	-0.479	-8.463 µA
M6	0.95	0.8	0.638	0.745	8.463 µA
M7	0.95	0.8	0.638	0.745	8.463 µA
M8	0.75	0.65	0.65	0.162	8.463 µA
M9	0.75	0.65	0.65	0.162	8.463 µA
M10	0.95	0.903	-0.897	-0.414	-29.215µA
M11	0.95	0.903	-0.897	-0.414	-29.215µA

6.3 AC Results

variable	value
Gain	59.6dB
Bandwidth	0.00278Mhz
GBW	4.276Mhz
PM	84.31
CMRR	20dB
PSRR	-2.66db

6.4 Transient analysis

	theoretical value	practical value
Slew rate	1	0.97
ICMR max	-	1.488
ICMR min	-	0.463
OCMR max	-	1.44
OCMR min	-	0.56

7 Conclusion

- From the theoretical study of folded cascode , it is concluded that the overall voltage swing of a folded-cascode op-amp is only slightly higher than that of a telescope configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain and higher noise.
- Folded cascode op-amps are used widely, even more than telescopic topologies, because the input and outputs can be shorted together and the choice of the input common-mode level is easier.
- Because In telescopic op-amp, three voltage must be defined carefully, the input CM level and the gate bias voltage of the PMOS and NMOS cascode transistors, whereas in folded-cascode configurations only the latter two are critical.
- In folded-cascode op-amp, the capability of handling input CM levels are close to one of the supply rails.