
STM32
CubeMX

1. Description

1.1. Project

Project Name	NUCLEO-G474RET6-Inverter_Pinout
Board Name	NUCLEO-G474RE
Generated with:	STM32CubeMX 6.9.1
Date	10/10/2023

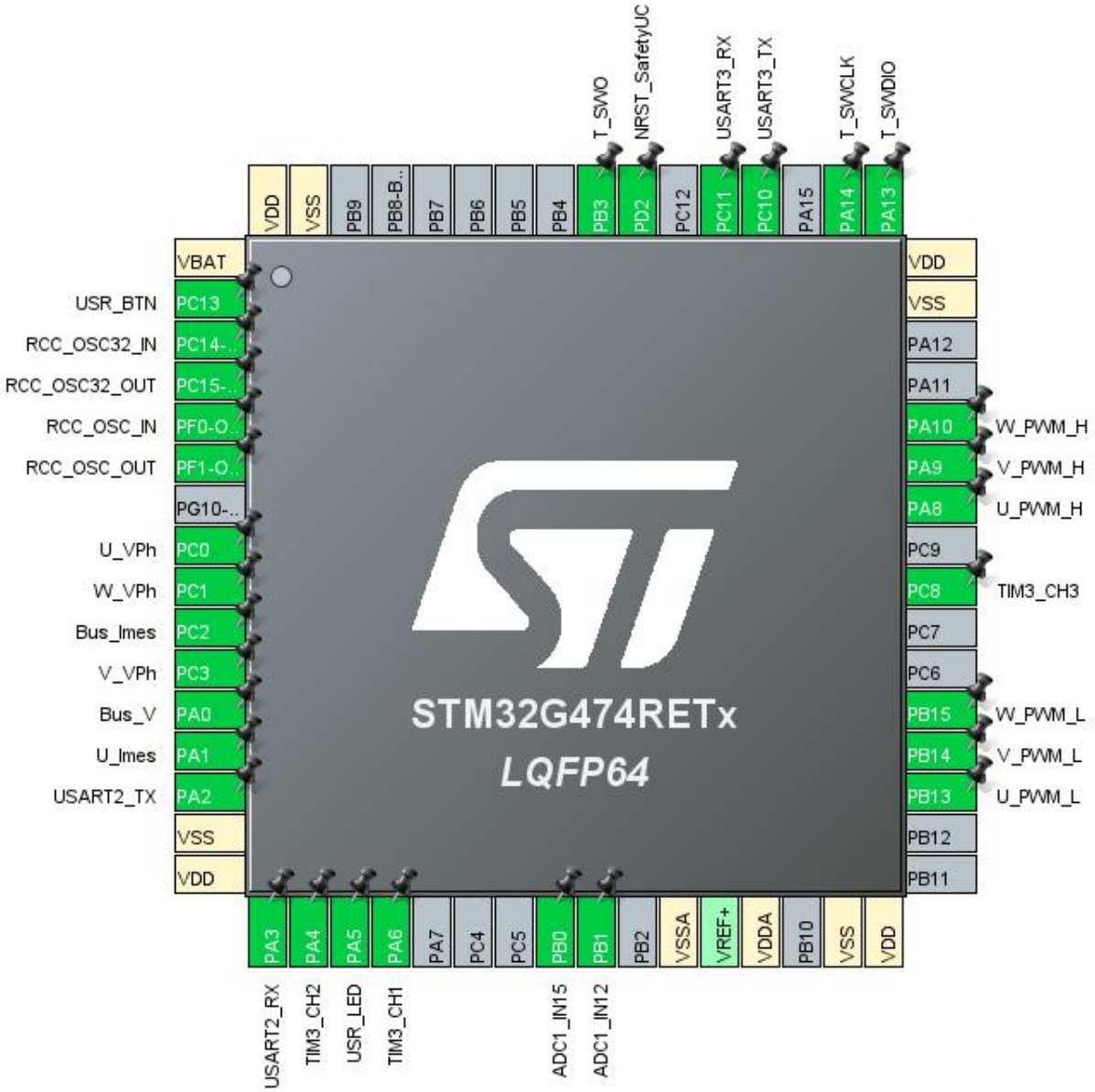
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration



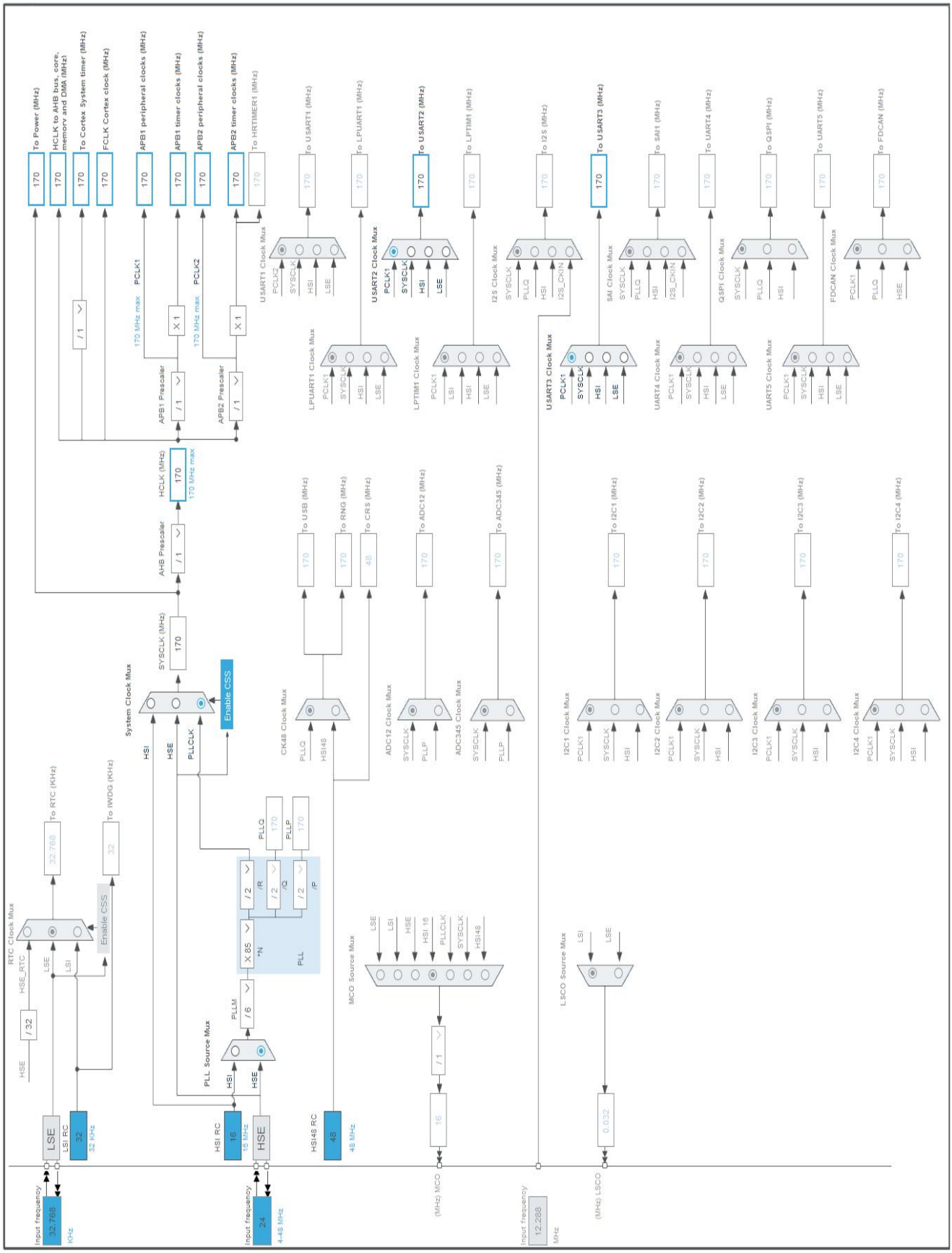
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	USR_BTN
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
8	PC0	I/O	ADC2_IN6	U_VPh
9	PC1	I/O	ADC2_IN7	W_VPh
10	PC2	I/O	ADC1_IN8	Bus_Imes
11	PC3	I/O	ADC2_IN9	V_VPh
12	PA0	I/O	ADC2_IN1	Bus_V
13	PA1	I/O	ADC1_IN2	U_Imes
14	PA2	I/O	USART2_TX	
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	USART2_RX	
18	PA4	I/O	TIM3_CH2	
19	PA5 *	I/O	GPIO_Output	USR_LED
20	PA6	I/O	TIM3_CH1	
24	PB0	I/O	ADC1_IN15	
25	PB1	I/O	ADC1_IN12	
27	VSSA	Power		
29	VDDA	Power		
31	VSS	Power		
32	VDD	Power		
35	PB13	I/O	TIM1_CH1N	U_PWM_L
36	PB14	I/O	TIM1_CH2N	V_PWM_L
37	PB15	I/O	TIM1_CH3N	W_PWM_L
40	PC8	I/O	TIM3_CH3	
42	PA8	I/O	TIM1_CH1	U_PWM_H
43	PA9	I/O	TIM1_CH2	V_PWM_H
44	PA10	I/O	TIM1_CH3	W_PWM_H
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
50	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
52	PC10	I/O	USART3_TX	
53	PC11	I/O	USART3_RX	
55	PD2 *	I/O	GPIO_Output	NRST_SafetyUC
56	PB3	I/O	SYS_JTDO-SWO	T_SWO
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	NUCLEO-G474RET6-Inverter_Pinout
Project Folder	C:\Users\Erika\OneDrive - Politecnico di
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC2_Init	ADC2
4	MX_ADC1_Init	ADC1
5	MX_TIM1_Init	TIM1
6	MX_TIM3_Init	TIM3
7	MX_USART2_UART_Init	USART2
8	MX_USART3_UART_Init	USART3

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
MCU	STM32G474RETx
Datasheet	DS12288_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

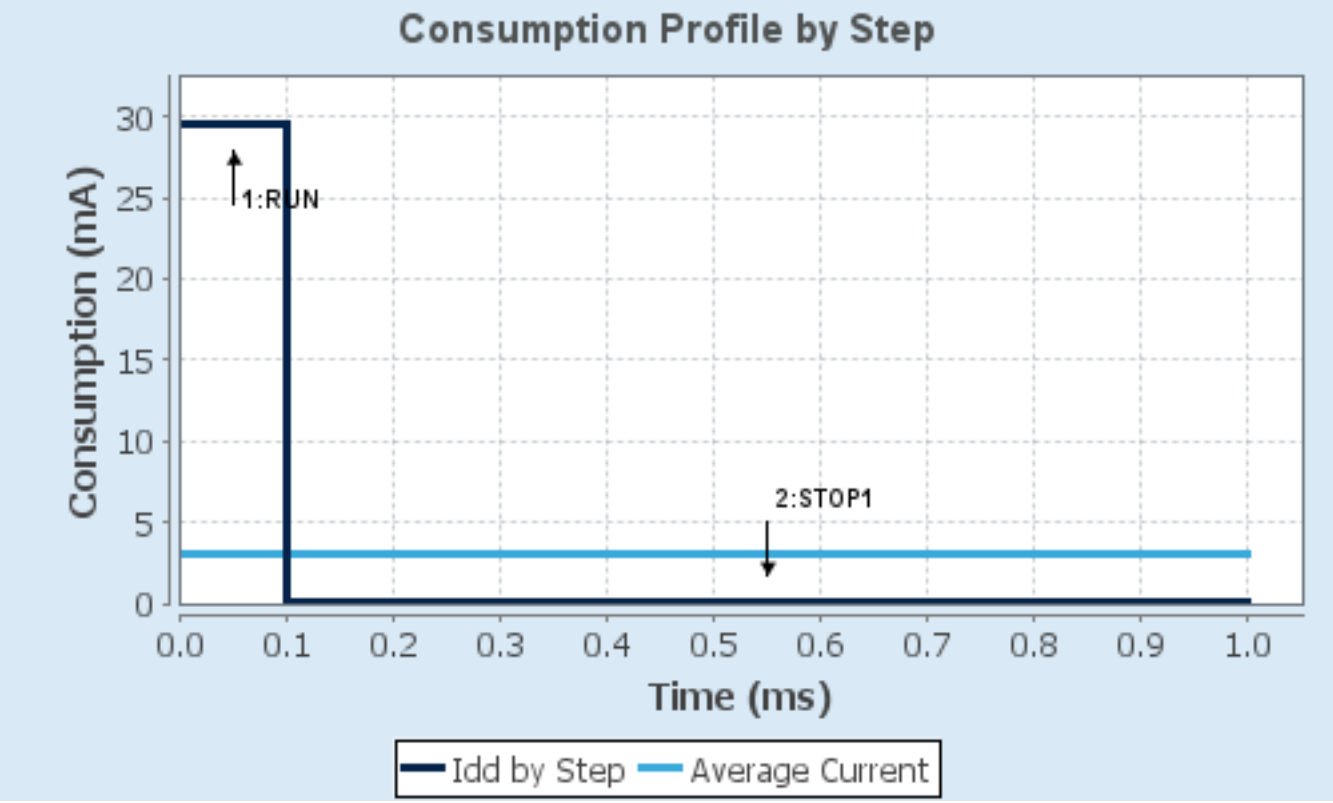
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/DualBank/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	29.5 mA	80.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	124.25	129.98
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days, 9 hours	Average DMIPS	212.5 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC1

IN2: IN2 Single-ended

IN8: IN8 Single-ended

mode: IN12

mode: IN15

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 4
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 8 ***
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.2. ADC2

IN1: IN1 Single-ended

IN6: IN6 Single-ended

IN7: IN7 Single-ended

IN9: IN9 Single-ended

2.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 4
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 6 ***
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

2.4. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM6

mode: save power of non-active UCPD - deactive Dead Battery pull-up

2.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel3: PWM Generation CH3 CH3N

2.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**127 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**65 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

DeadTime Preload	Disable
Dead Time	**25 ***
Asymmetrical DeadTime	Disable
Falling Dead Time	0

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	**39 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	**39 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	**39 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

2.6. TIM3

Combined Channels: XOR ON / Hall Sensor Mode

2.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection TRGO	Output Compare (OC2REF)

Hall Sensor:

Prescaler Division Ratio	No division
Polarity	Rising Edge
Input Filter	0
Commutation Delay	0

2.7. USART2

Mode: Asynchronous

2.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.8. USART3

Mode: Asynchronous

2.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC2	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	Bus_Imes
	PA1	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	U_Imes
	PB0	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC0	ADC2_IN6	Analog mode	No pull-up and no pull-down	n/a	U_VPh
	PC1	ADC2_IN7	Analog mode	No pull-up and no pull-down	n/a	W_VPh
	PC3	ADC2_IN9	Analog mode	No pull-up and no pull-down	n/a	V_VPh
	PA0	ADC2_IN1	Analog mode	No pull-up and no pull-down	n/a	Bus_V
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	T_SWCLK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	T_SWO
TIM1	PB13	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	U_PWM_L
	PB14	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	V_PWM_L
	PB15	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	W_PWM_L
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	U_PWM_H
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	V_PWM_H
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	W_PWM_H
TIM3	PA4	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USR_BTN
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USR_LED

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NRST_SafetyUC

3.2. DMA configuration

nothing configured in DMA service

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	true	0	0
EXTI line[15:10] interrupts	true	0	0
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	true	15	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupt	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	unused		
FPU global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

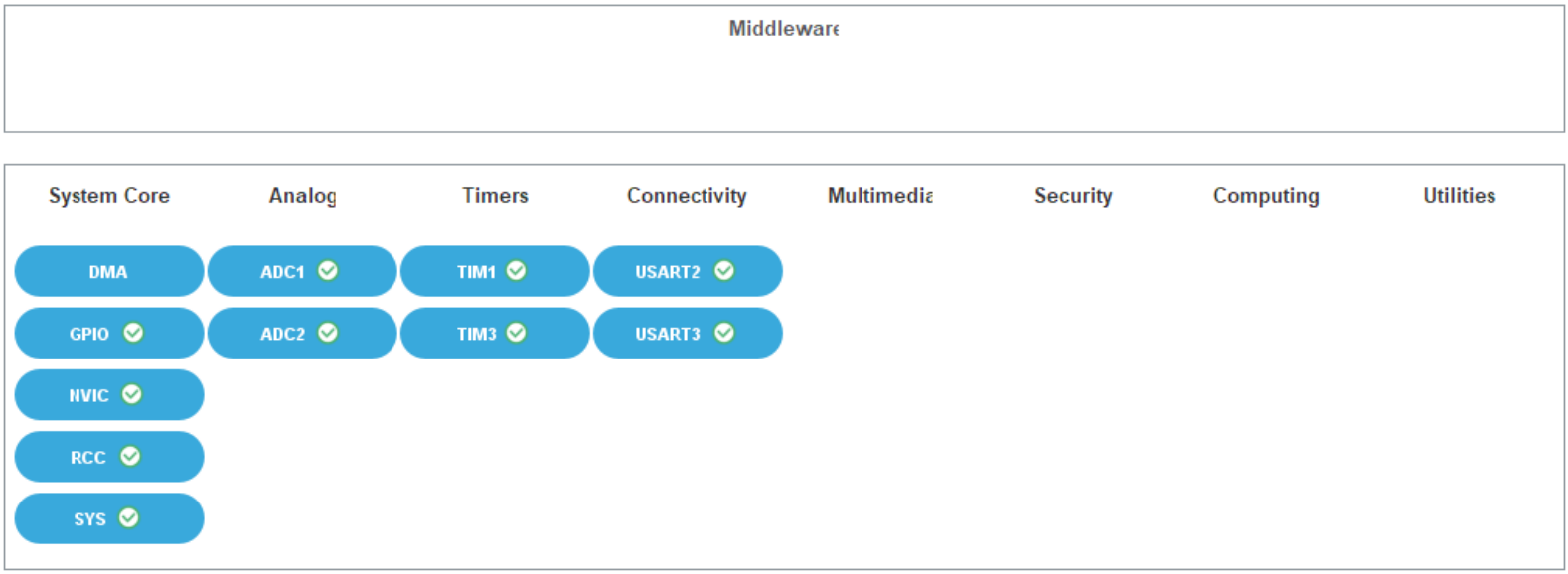
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	false	true	true

*** User modified value**

4. System Views

4.1. Category view

4.1.1. Current



5. Docs & Resources

Type	Link