Experiment 03: Study of Boolean Algebra

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1 Aim

To study the basic laws of Boolean Algebra and verify them using implementation of logic gates using Integrated Circuits.

2 Theory

3 Verification of Truth Tables and Observations

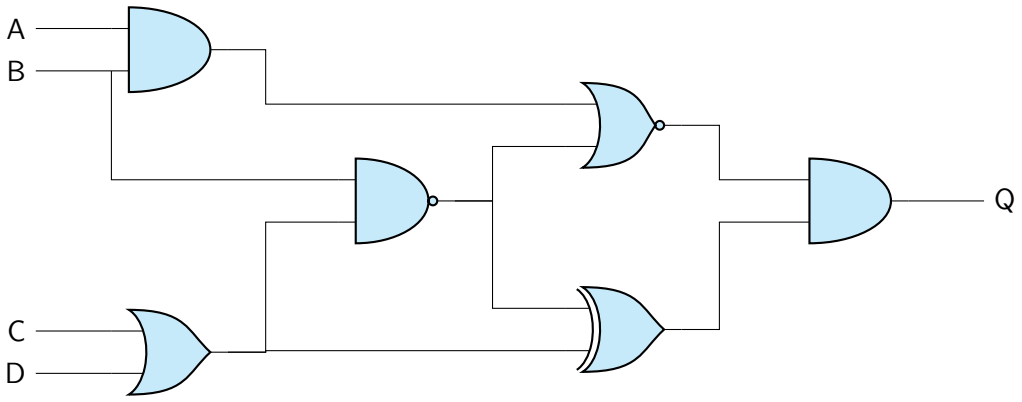

Figure 1: Logic Gate circuit diagram for for Example 1

Table 1: Truth Table for $Y = \overline{\mathrm{A}}\mathrm{B}(\mathrm{C} + \mathrm{D})$

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

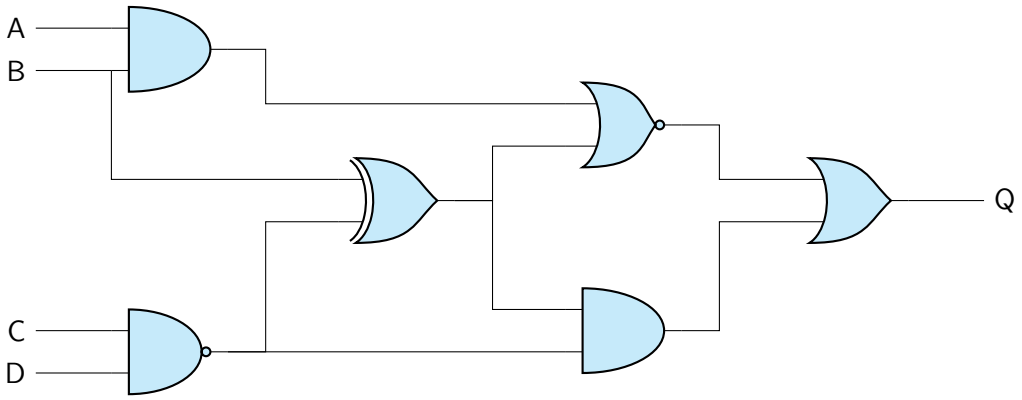

Figure 2: Logic Gate circuit diagram for for Example 2

Table 2: Truth Table for $Y = \overline{\mathrm{A}}\,\overline{\mathrm{C}} + \overline{\mathrm{A}}\,\overline{\mathrm{D}} + \overline{\mathrm{B}}$

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

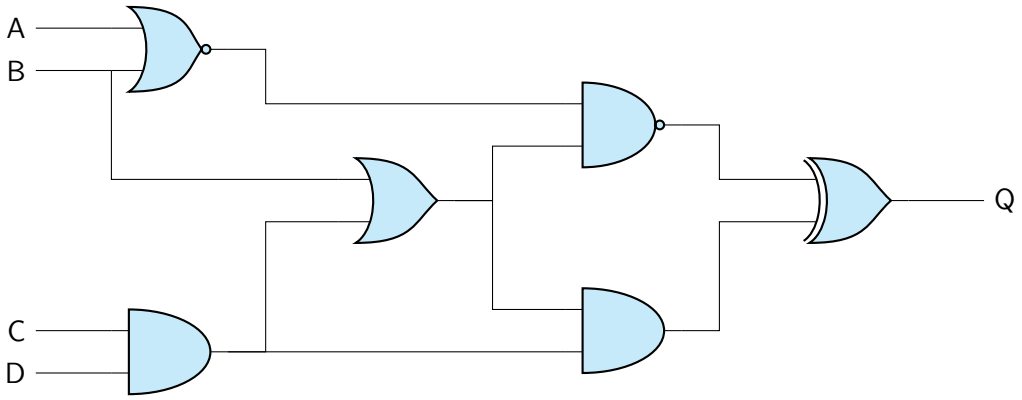

Figure 3: Logic Gate circuit diagram for for Example 3

Table 3: Truth Table for $\mathrm{Y} = \overline{\mathrm{A}}\,\overline{\mathrm{B}} + \overline{\mathrm{D}} + \overline{\mathrm{C}}$

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

4 Sources of Error

5 Discussion and Conclusion