Title: UFP Exit Condition Clarification Applied to: USB 3.2_r1.0 Sep. 22, 2017

Brief description of the functional changes:
Incorrect description of Hub UFP behavior from eSS.Disabled to Rx.Detect.
Adding a new transition condition to peripheral UFP behavior from eSS.Disabled to Rx.Detect to
accommodate for PD USB data reset.
Benefits as a result of the changes:
Match hub description in chapter 10 and PD data reset.
mater has accomplish in chapter to and t S add roots.
An assessment of the impact to the existing revision and systems that currently conform to the USB
specification:
None. Hub implementations follow chapter 10.
Peripheral device compliant to PD should add this transition condition.
An analysis of the hardware implications:
Most likely none since hub implementations follow chapter 10.
An analysis of the software implications:
None
None
An analysis of the compliance testing implications:
None. Hub UFP tested in hub compliance. Peripheral device tested in Type C functional compliance test.
None. Hub of Fitested in hub compliance. Feripheral device tested in Type Citational compliance test.

Actual Change

(a). From Text: Section 7.5.1.1

7.5.1.1 eSS.Disabled for Downstream Ports and Hub Upstream Ports

eSS.Disabled for Downstream Ports and Hub Upstream Ports does not contain any substates.

7.5.1.1.1 eSS.Disabled Requirements

- VBUS may be present during eSS.Disabled.
- The port's receiver termination shall present high impedance to ground of $Z_{\text{RX-HIGH-IMP-DC-POS}}$ defined in Table 6-21.
- The port shall be disabled from transmitting and receiving LFPS and Enhanced SuperSpeed signals.

7.5.1.1.2 Exit from eSS.Disabled

- A downstream port shall transition to Rx.Detect when directed.
- An upstream port shall transition to Rx.Detect only when VBUS transitions to valid or a USB 2.0 bus reset is detected.

(a). To Text: Section 7.5.1.1

7.5.1.1 eSS.Disabled for Downstream Ports and Hub Upstream Ports

eSS.Disabled for Downstream Ports and Hub Upstream Ports does not contain any substates.

7.5.1.1.1 eSS.Disabled Requirements

- VBUS may be present during eSS.Disabled.
- The port's receiver termination shall present high impedance to ground of $Z_{\text{RX-HIGH-IMP-DC-POS}}$ defined in Table 6-21.
- The port shall be disabled from transmitting and receiving LFPS and Enhanced SuperSpeed signals.

7.5.1.1.2 Exit from eSS.Disabled

- A downstream port shall transition to Rx.Detect when directed.
- An upstream port shall transition to Rx.Detect when VBUS transitions to valid or when directed.

(b). From Text: Section 7.5.1.2

7.5.1.2 eSS.Disabled for Upstream Ports of Peripheral Devices

eSS.Disabled of a peripheral device operates similarly to hub upstream ports, except that it only attempts a limited number of Enhanced SuperSpeed attempts upon USB 2.0 bus reset.

Page: 2

7.5.1.2.1 eSS.Disabled Substate Machine

eSS.Disabled of a peripheral device has two substates shown in Figure 7-15.

- eSS.Disabled.Default
- eSS.Disabled.Error

eSS.Disable.Default is a logical power-off state for a self-powered peripheral device.

7.5.1.2.2 eSS.Disabled Requirements

The requirements of a peripheral upstream port are the same as defined in Section 7.5.1.1.1. In addition, a peripheral upstream port shall implement a tDisabledCount counter. The operation of the tDisabledCount counter shall meet the following requirement.

- The tDisabledCount counter shall be reset to zero upon one of the following two conditions:
 - 1. Invalid VBUS
 - 2. Successful port configuration exchange
- The tDisabledCount counter shall be incremented upon entry to eSS.Disabled.Default.

7.5.1.2.3 Exit from eSS.Disabled.Default

- A peripheral upstream port shall transition to Rx.Detect if one of the following conditions are met:
 - 1. When VBUS transitions to valid.
 - 2. When a USB 2.0 bus reset is detected and tDisabledCount is less than 3.
- A peripheral upstream port shall transition to eSS.Disabled.Error if tDisabledCount is 3.

(b). To Text: Section 7.5.1.2

7.5.1.2 eSS.Disabled for Upstream Ports of Peripheral Devices

eSS.Disabled of a peripheral device operates similarly to hub upstream ports, except that it only attempts a limited number of Enhanced SuperSpeed attempts upon USB 2.0 bus reset.

7.5.1.2.1 eSS.Disabled Substate Machine

eSS.Disabled of a peripheral device has two substates shown in Figure 7-15.

- eSS.Disabled.Default
- eSS.Disabled.Error

eSS.Disable.Default is a logical power-off state for a self-powered peripheral device.

7.5.1.2.2 eSS.Disabled Requirements

The requirements of a peripheral upstream port are the same as defined in Section 7.5.1.1.1. In addition, a peripheral upstream port shall implement a tDisabledCount counter. The operation of the tDisabledCount counter shall meet the following requirement.

- The tDisabledCount counter shall be reset to zero upon one of the following two conditions:
 - 1. Invalid VBUS

Page: 3

- 2. Successful port configuration exchange
- The tDisabledCount counter shall be incremented upon entry to eSS.Disabled.Default.

7.5.1.2.3 Exit from eSS.Disabled.Default

- A peripheral upstream port shall transition to Rx.Detect if one of the following conditions are met:
 - 1. When VBUS transitions to valid.
 - 2. When a USB 2.0 bus reset is detected and tDisabledCount is less than 3.
 - 3. When directed.
- A peripheral upstream port shall transition to eSS.Disabled.Error if tDisabledCount is 3.