USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: DP Clock Sync Minimum Number of Fixes
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
Increases the number of PLL adjustments at the DP OUT Adapter before Main Link data starts to flow

Benefits as a result of the changes:
A DP OUT Adapter can get its restored clock closer to the DPTX frequency

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
At DP IN Adapter – Gate the end of link training longer. At DP OUT Adapter - Increase the counter of minimal fixes.

An analysis of the software implications:
None

An analysis of the compliance testing implications:
None

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Actual Change

(a). Section 10.4.10.1.1 DP IN Adapter Requirements

- A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true:
    - The DP IN Adapter internal status indicates link training has ended successfully.
    - The DP IN Adapter sent at least ~~three~~ nine DP Clock Sync Packets after it sent the SET_CONFIG Packet of type SET_LINK.

(b). Section 10.4.10.1.3.2 LTTPR – EQ Phase

- The DP IN Adapter alters the AUX response according to:
    - Its internal EQ_DONE, SYMBOL_LOCK & LANE_ALIGNMENT states.
    - It sent ~~three~~ at least nine DP Clock Sync Packets.
- In this example, it achieves EQ_DONE, SYMBOL_LOCK & LANE_ALIGNMENT on both Lanes and was able to send at least ~~three~~ nine DP Clock Sync Packets.

(c). Section 10.4.10.2.1 DP IN Adapter Requirements

- A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true:
    - The DP IN Adapter internal status indicates link training has ended successfully.
    - The DP IN Adapter received a SET_CONFIG Packet of type SET_LINK, carrying the same LC and LR fields that it sent to the DP OUT Adapter when link training was initiated.
    - The DP IN Adapter sent at least ~~three~~ nine DP Clock Sync Packets after it received a SET_CONFIG Packet of type STATUS_CR_DONE.

(d). Section 10.5.4 DP OUT Adapter Buffer

2. The DP OUT Adapter ensures, in an implementation specific manner, that within ~~three~~ eight PLL frequency adjustments the link symbol clock frequency difference between its own and the DPTX is such that buffer overflow and buffer underrun is avoided.