USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: CL0s Exit Timeout
Applied to: USB4 Specification Version 1.0

Brief description of the changes:
Adds a timeout when exiting CL0s

Benefits as a result of the changes:
A more robust exit flow

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Will not support this timeout

An analysis of the hardware implications:
Need to add a timeout counter

An analysis of the software implications:
None

An analysis of the compliance testing implications:
Need to add test for CL0s exit flow with no response

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Actual Change

(a). Section 7.3.1.2, Page 251

From Text:

The USB4 Port initiating exit from CL0s state shall:
1. Send a Low Frequency Periodic Signaling (LFPS) burst on all Lanes for the duration of at least 16 LFPS cycles (see Section 3.7) and for no more than tLFPSDuration.
2. Return to Electrical Idle for tPreData (see Table 3-20).
3. Start transmitting SLOS1 on each Lane of the USB4 Port. Any received CL_WAKE Ordered Sets shall be ignored.
    - A USB4 Port may exit CL0s state with SSC enabled or disabled.
4. On detection of 2 back-to-back TS2 Ordered Sets, stop sending SLOS1 and send at least 16 TS2 Ordered Sets. The first TS2 Ordered Set shall be sent within tTrainingTransition after detection of the TS2 Symbol. Before transmitting the first TS2 Ordered Sets:
    - The scrambler shall load a new seed as defined in Section 4.3.5.
    - Activate RS-FEC as defined in Section 4.3.6.1.
    - Enable SSC if SSC is disabled.
    Note: If the Adapter is in Training state (due to receiving Link errors while in CL0s state), then the Adapter proceeds with the Training state-machine rather than sending the TS2 Ordered Sets.
5. Transition to CL0 state.

To Text:

The USB4 Port initiating exit from CL0s state shall:
1. Send a Low Frequency Periodic Signaling (LFPS) burst on all Lanes for the duration of at least 16 LFPS cycles (see Section 3.7) and for no more than tLFPSDuration.
2. Return to Electrical Idle for tPreData (see Table 3-20).
3. Start transmitting SLOS1 on each Lane of the USB4 Port. Any received CL_WAKE Ordered Sets shall be ignored.
    - A USB4 Port may exit CL0s state with SSC enabled or disabled.
4. On detection of 2 back-to-back TS2 Ordered Sets, stop sending SLOS1 and send at least 16 TS2 Ordered Sets. The first TS2 Ordered Set shall be sent within tTrainingTransition after detection of the TS2 Symbol. Before transmitting the first TS2 Ordered Sets:
    - The scrambler shall load a new seed as defined in Section 4.3.5.
    - Activate RS-FEC as defined in Section 4.3.6.1.
    - Enable SSC if SSC is disabled.
    Note: If the Adapter is in Training state (due to receiving Link errors while in CL0s state), then the Adapter proceeds with the Training state-machine rather than sending the TS2 Ordered Sets.
    If the receiver did not detect 2 back-to-back TS2 Ordered Sets within tTrainingAbort2 time after the transmitter started sending SLOS1 it shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.

5. Transition to CL0 state.

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

(b). Section 4.6, Page 191

From Text:

tTrainingAbort2	The amount of time in Training state following any transition to Training state other than from CLd state and time to send LFPS when exiting CL1 or CL2.	100	--	ms

To Text:

tTrainingAbort2	The amount of time in Training state following any transition to Training state other than from CLd state, ~~and~~ time to send LFPS when exiting CL1 or CL2 and time to send SLOS1 in CL0s exit.	100	--	ms