Ve 270 Introduction to Logic Design

Lab 5
Design of a Digital Clock

UM-SJTU Joint Institute
Shanghai Jiao Tong University
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1. Objective

- To get familiarized with binary counters.
- To design a clock divider that slows down the frequency of a clock signal.
- To design a two-digit timer that counts the number of seconds from 00 to 59, and repeats.
- To display the two digits using the seven-segment displays on the FPGA board.

2. Requirement

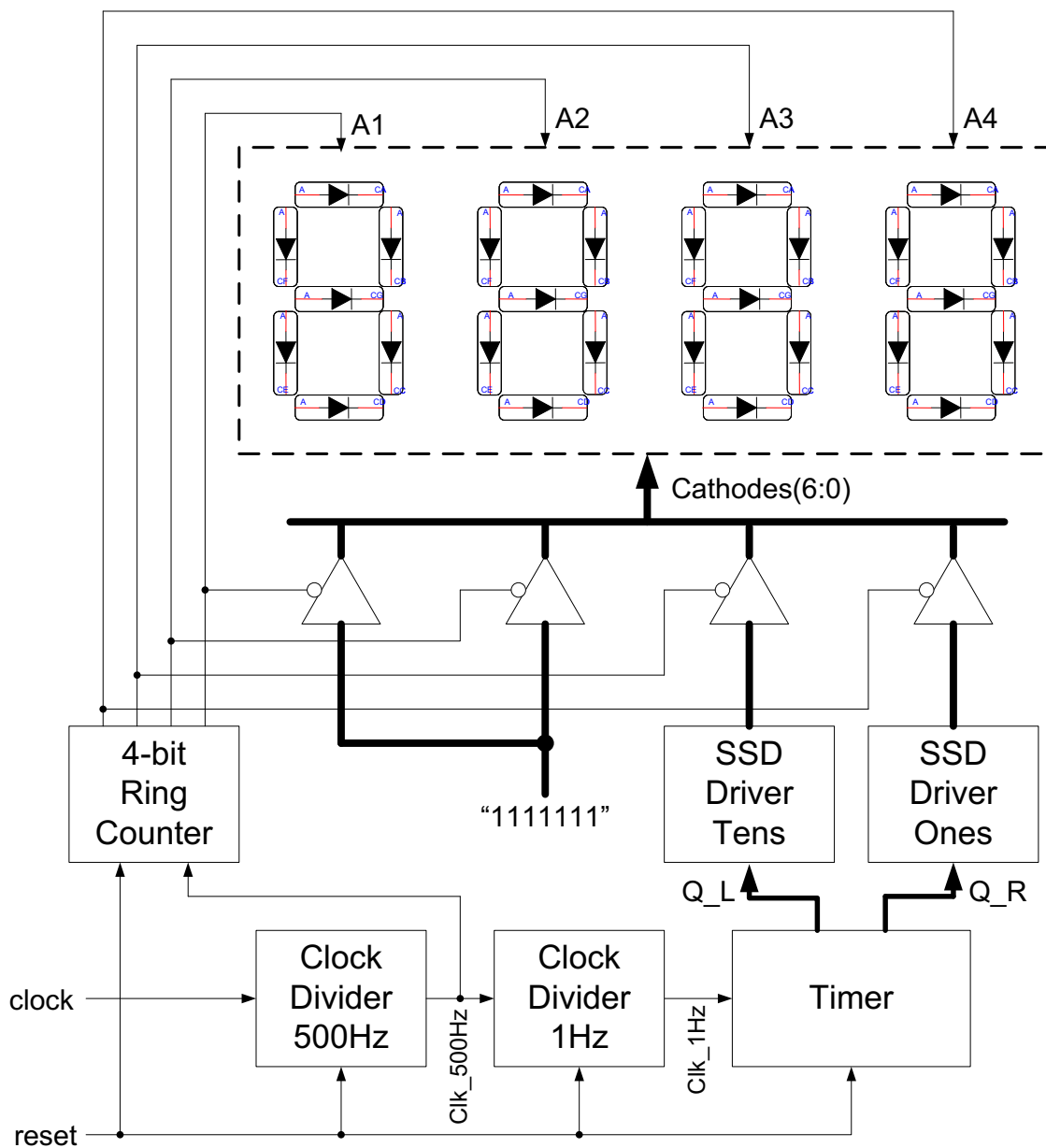Design a digital clock following the block diagram in Figure 1.

Figure 1. Block Diagram of the Digital Clock

2.1 Clock Divider

The frequency of internal clock on the FPGA board that we are using is 100MHz. However, the digital clock should be triggered by a signal with 1Hz frequency. This means the on-board clock should be divided by 100,000,000 times. Design a clock divider to slow down the on-board clock signal to 1Hz.

2.2 Two Digit Timer

The digital clock counts the number of seconds with counting sequence:

$$00 \rightarrow 01 \rightarrow 02 \rightarrow \ldots \rightarrow 09 \rightarrow 10 \rightarrow 11 \rightarrow \ldots \rightarrow 59 \rightarrow 00$$

One way to approach this task is to use two counters, one for the ten's digit and one for the one's digit. Thus, the counter for the one's digit has counting sequence of:

$$0 \rightarrow 1 \rightarrow 2 \rightarrow \ldots \rightarrow 9$$

Likewise, the incrementing of the counter for the ten's digit is triggered by the one's digit whenever it reaches its terminal count. The ten's digit counter has counting sequence of:

$$0 \rightarrow 1 \rightarrow 2 \rightarrow \ldots \rightarrow 5$$

2.3 Structure of on-board SSD

There are four common anode SSDs on the FPGA board. These four SSDs share the corresponding cathodes. In other words, the cathodes of similar segments on all four displays are connected together. The connection of the SSDs is illustrated in Figure 2. So the four displays have only one group of 7-bit cathodes instead of four groups, and all SSDs get the same signals for their cathodes. There are four separate anodes, one for each display.
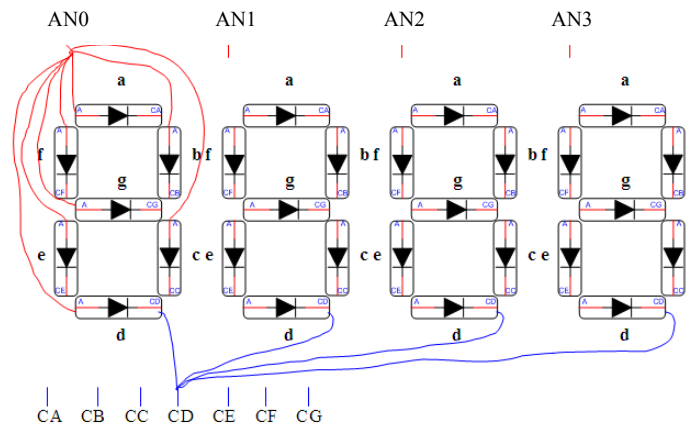

Figure 2. Structure of SSDs on Nexys2 FPGA board

Note: the four ports AN0, AN1, AN2, and AN3 on the FPGA board are not the actual anodes of the SSDs. They are the base terminals of p-type transistors. Thus providing a "0" to AN0, AN1, AN2, or AN3 will turn the corresponding SSD on. The connection is shown in Figure 3.
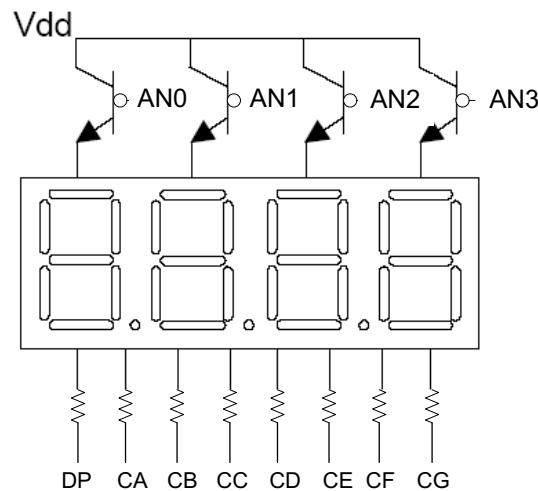
Figure 3. Power connections seven segment display.

2.4 Display of Multi-digit Number

If a 7-bit signal is provided to the cathodes and all four anodes are turned on at the same time, then the four SSDs will display the same thing. Thus, SSDs require a multiplex driving scheme. In order to display different characters on different SSDs, one anode should be turned on at a time while appropriate cathodes for the corresponding SSD shall be provided. Then the asserted anode and the appropriate 7-bit cathodes for the next SSD should be applied. If this action continues and repeats, the four SSDs will be turned on alternately displaying different characters on each SSD. If this alternate illumination is fast enough then it will appear to human eyes as if all the SSDs light up simultaneously. This driving scheme is shown as timing diagrams in Figure 4. In the figure, "digit0", "digit1", "digit2", and "digit3" are the cathodes provided to each SSD when the corresponding anode is turned on. Since only two SSDs will be used in this lab, the rest two SSDs will be provided "1111111" for their cathodes when their anodes are turned on to display nothing. In order for the digits to appear bright and continuously illuminated, all four digits should be driven once every 1 to 16 ms. In other words, each anode should be turned on at a frequency in the range of 60Hz to 1KHz. This requires the clock signal in Figure 4 should be in the range of 240Hz to 4KHz. This clock signal should also be a slower output of a clock divider.
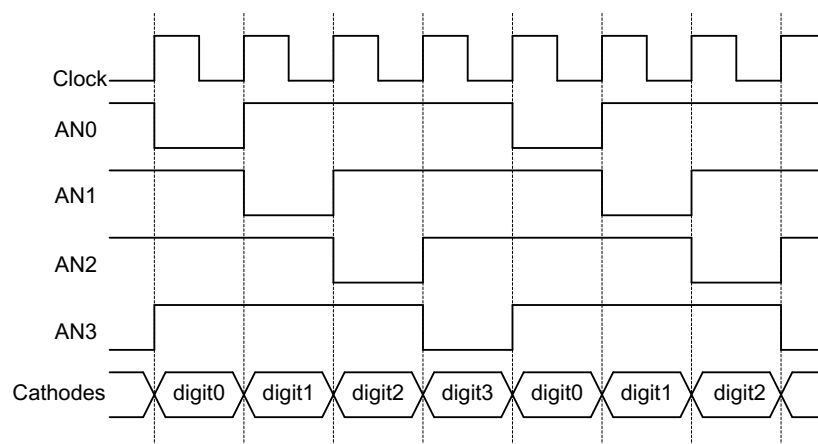

Figure 4. Driving scheme for SSDs

3. Verilog Coding

Model the digital clock with Verilog HDL following the block diagram in Figure 1. View RTL schematic generated from your Verilog code and identify the portions corresponding to the blocks in Figure 1.

4. Simulation, Synthesis, and FPGA Implementation

Simulate your Verilog model of the digital clock. Synthesize and implement your design on the Basys3 FPGA board.

Note: the 100MHz internal clock is provided to pin "W5" on the FPGA board.
5.
6. Demonstration and Deliverables

This is a 2-week lab. The full score for this lab is 200 points.

1) Demonstrate your circuits to the TAs before your lab session ends.
2) Upload source files on Canvas by **10pm, November 9, 2019**.
3) Upload peer evaluation report on Canvas by **10pm, November 9, 2019**.

Peer evaluation form:

Name	Percentage of contribution (sum to 100%)	Responsibilities
(yourself)		
(your lab partner)		