```
module D_ff (q, d, clk);
input d, clk;
output q;
reg q;
always @ (posedge clk) begin
q <= d;
end
endmodule
//////////////////////////////////////////////////////////////////////////////////
module mux (out, i0, i1, i2, i3, s1, s0);
input i0, i1, i2, i3, s1, s0;
output out;
reg out;
always @ (i0, i1, i2, i3, s1, s0) begin
case ({s1, s0})
2'b00: out=i0;
2'b01: out=i1;
2'b10: out=i2;
2'b11: out=i3;
endcase
end
endmodule
//////////////////////////////////////////////////////////////////////////////////
module hw5(Q, D, sl, sh, l, clk);
input [3:0] D;
input sl, sh, l, clk;
output [3:0] Q;
wire w3, w2, w1, w0;
mux m3 (w3, Q[3], D[3], sl, sl, sh, l);
mux m2 (w2, Q[2], D[2], Q[3], Q[3], sh, l);
mux m1 (w1, Q[1], D[1], Q[2], Q[2], sh, l);
mux m0 (w0, Q[0], D[0], Q[1], Q[1], sh, l);
D_ff D3 (Q[3], w3, clk);
D_ff D2 (Q[2], w2, clk);
D_ff D1 (Q[1], w1, clk);
D_ff D0 (Q[0], w0, clk);
endmodule
```