VE270 Mid Exam Review
Part 3: Combinational Circuit

Shi Li

2019.10.20

Combinational Circuit compared with Sequential Circuit

- Truth table for a combinational circuit
- Output depends on input

p	q	p∨q
T	T	T
T	F	T
F	T	T
F	F	F

- Characteristic table for a sequential circuit
- Output depends on input & previous state

S(t)	R(t)	Q(t)	Q(t+Δ) → Q⁺	
0	0	0	0	hold
0	0	1	1	
0	1	0	0	reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	not allowed
1	1	1	X	

Design Process

- Capture the function
  - truth table/equation from requirements
- Convert to equation
  - k-map logic optimization
- Implement the circuit
  - from the optimized logic expression

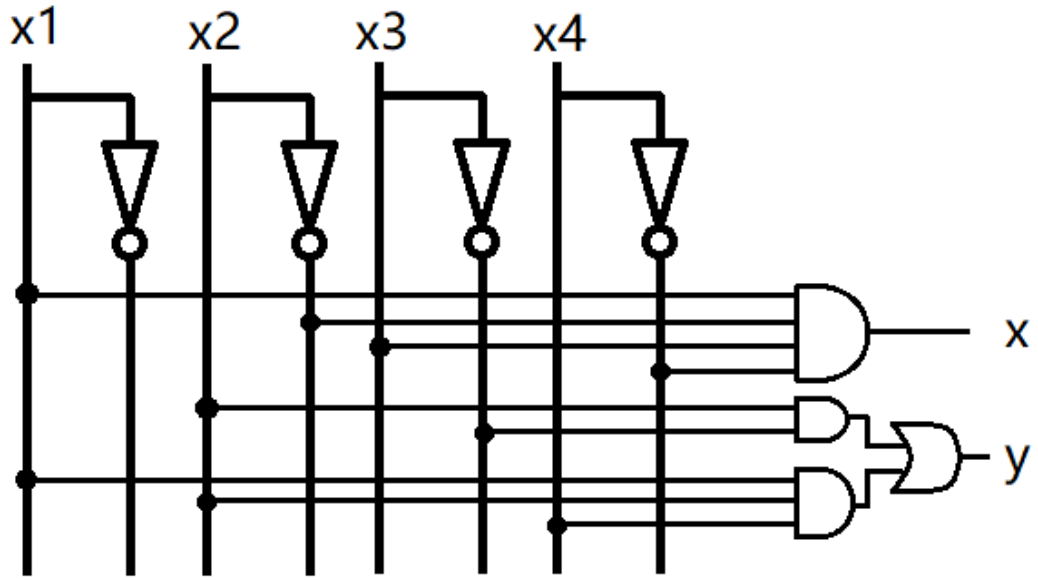
Design Process Exercise
HW3 Problem 3

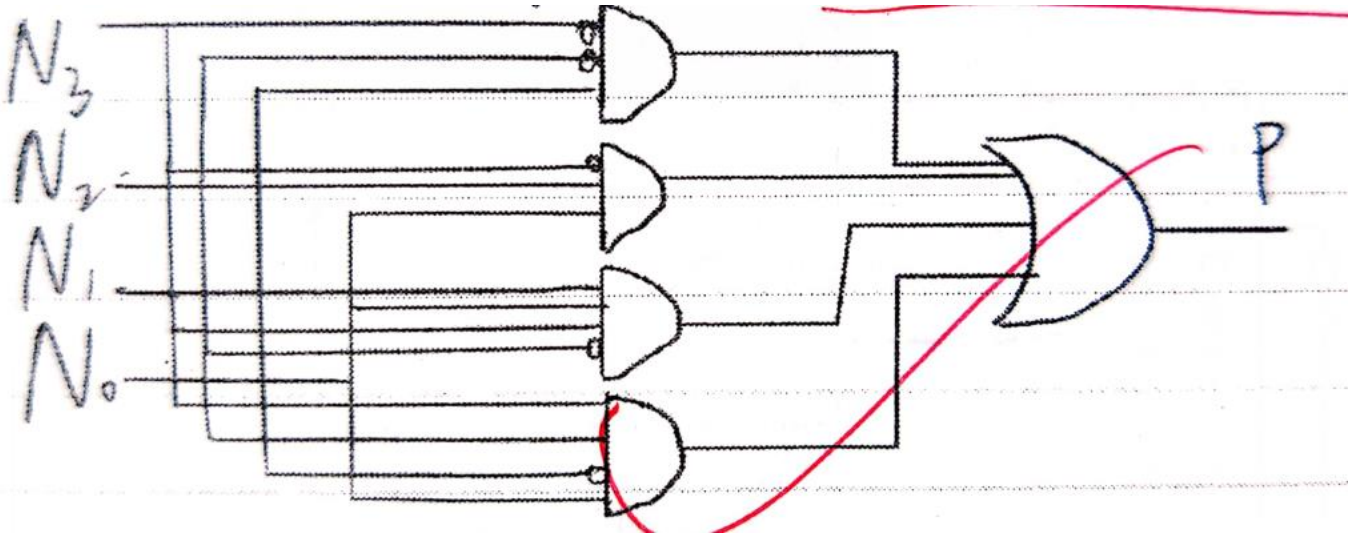
- Problem Description
- Input: 3 bits $x_2x_1x_0$, where x_0 is the least significant bit (LSB).
- Output: 1 bit L, meaning low level of fuel.
- Specification: When the input is less than 3, the output is 1. Otherwise, the output is 0.

Design Process Exercise
HW3 Problem 3

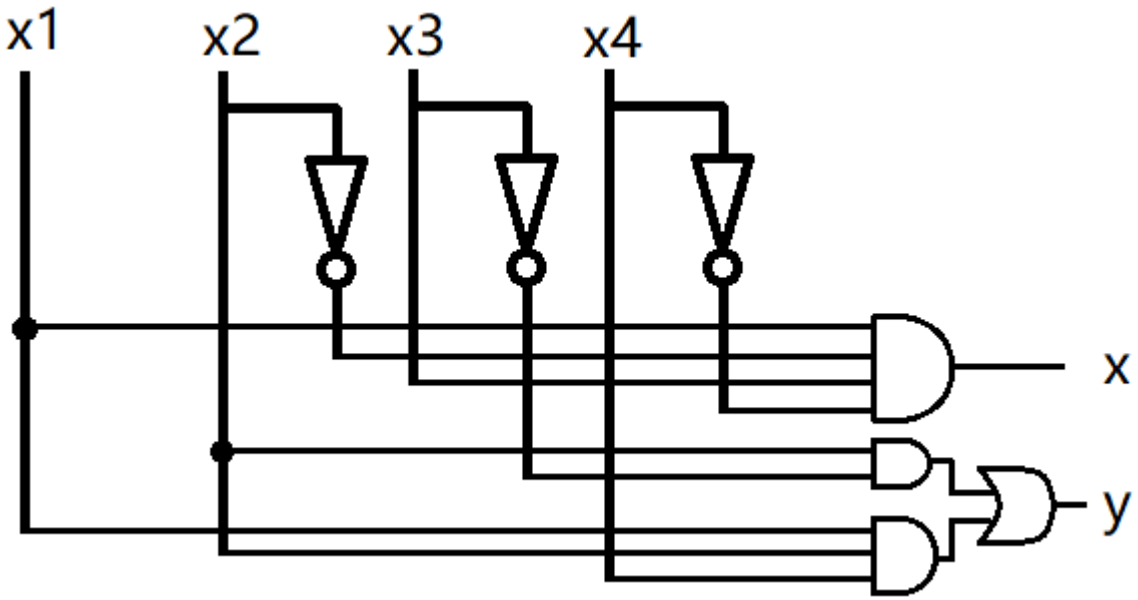
- Step 1. Capture the function
  - $L = x_2' x_1' x_0' + x_2' x_1' x_0 + x_2' x_1 x_0'$
- Step 2. Convert the equation
  - For simple equation, algebra method and k-map method are both useful.
  - However, for complicated equation, we prefer k-map method.
  - Here we use algebra method to simplify the expression for L.
  - $L = x_2'(x_1' x_0' + x_1' x_0 + x_1 x_0') = x_2'(x_1 x_0)'$
- Step 3. Implement the circuit

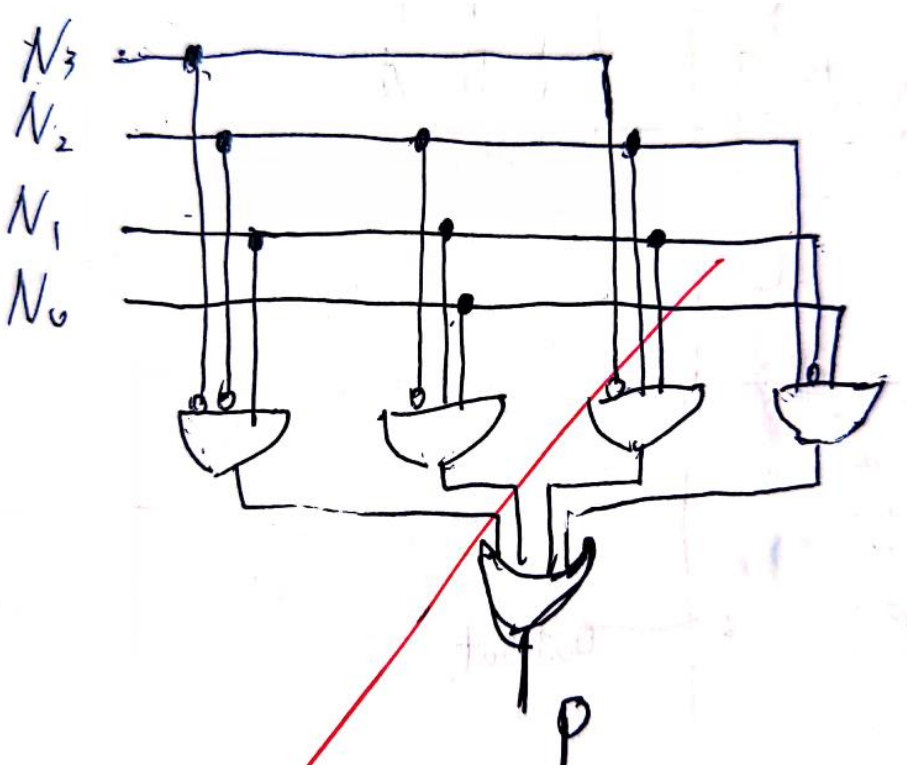
How to draw the circuit elegantly? Good Examples



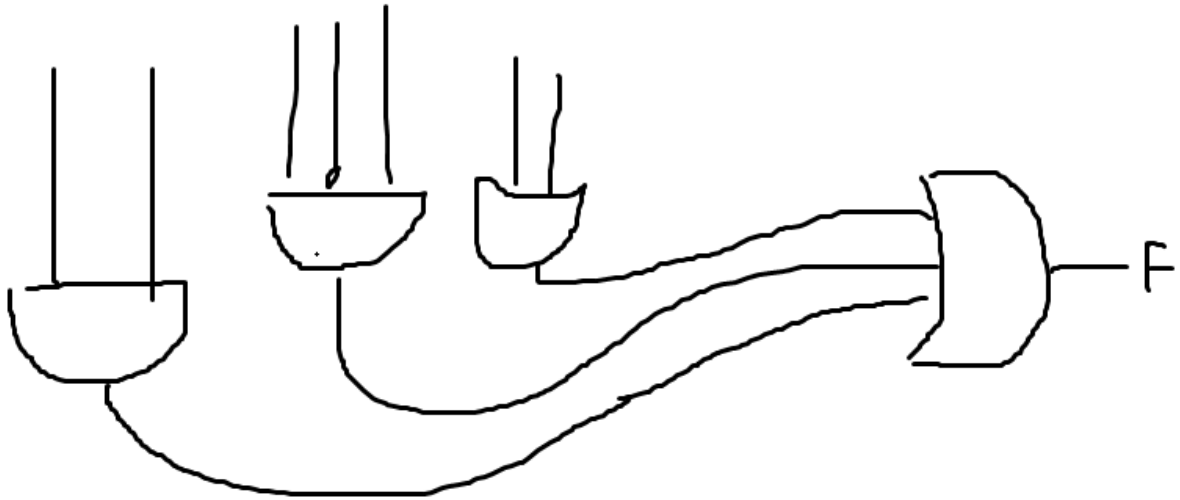


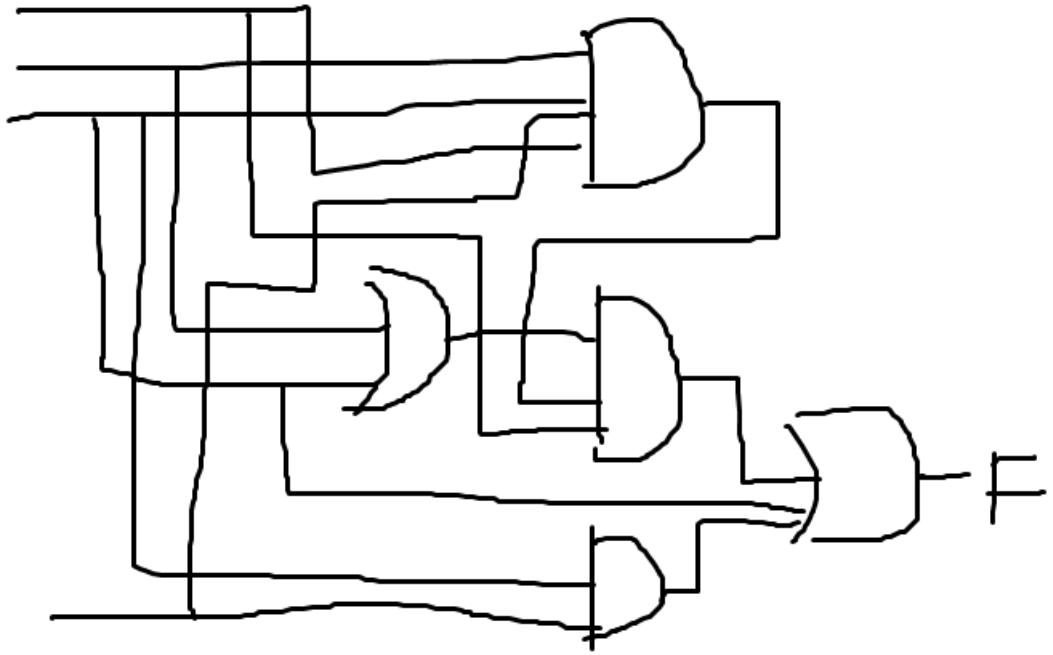
How to draw the circuit elegantly? Better Examples





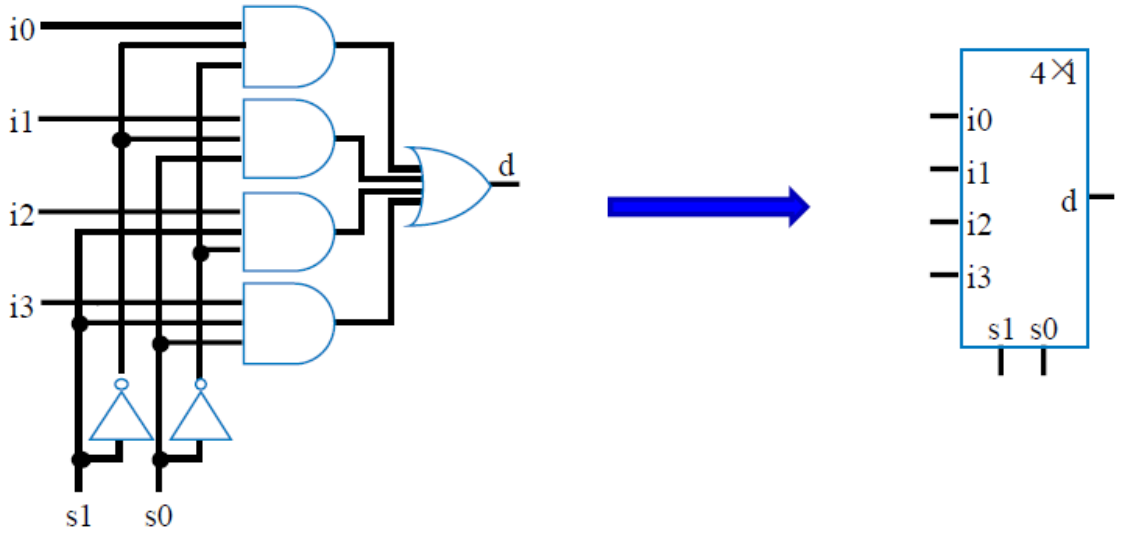
How to draw the circuit elegantly?
Bad Examples





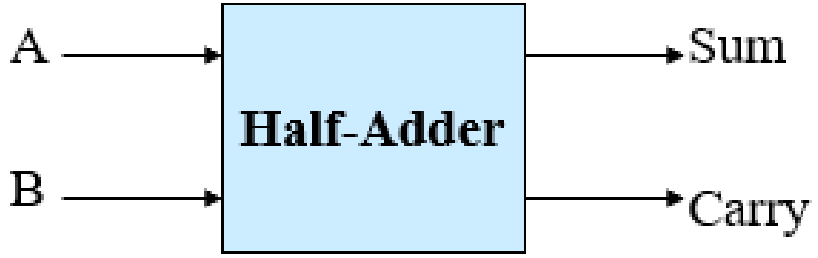
Combinational Building Blocks
1. MUX

- Example: 4 to 1 Mux
- Using 2 “switches” to choose one of the four input signals

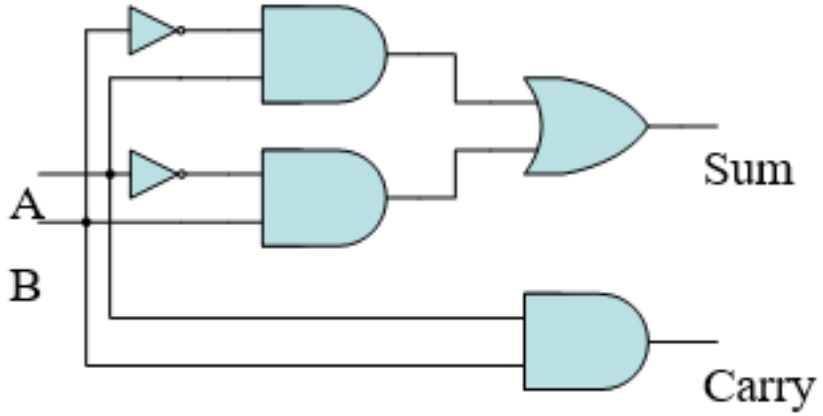


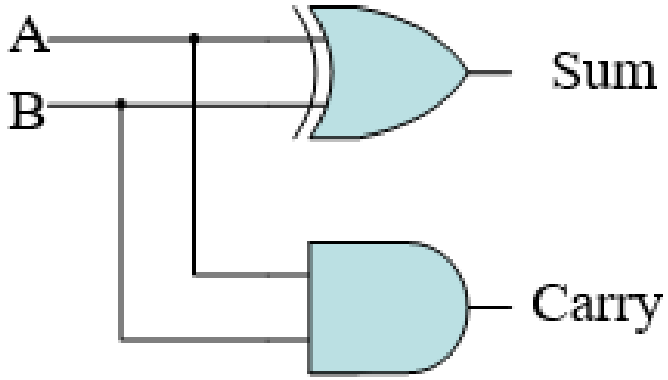
- Question: If we have 35 input from i0 to i34, how much “switches” do we need?
- Answer: 6 (i35~i63 can be seen as don’t cares)

Combinational Building Blocks
2. Adder: Half Adder

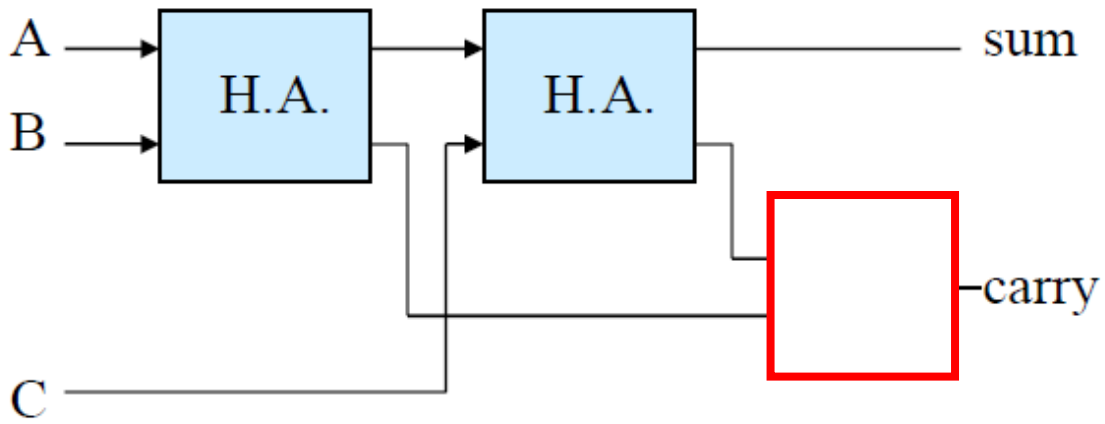


A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



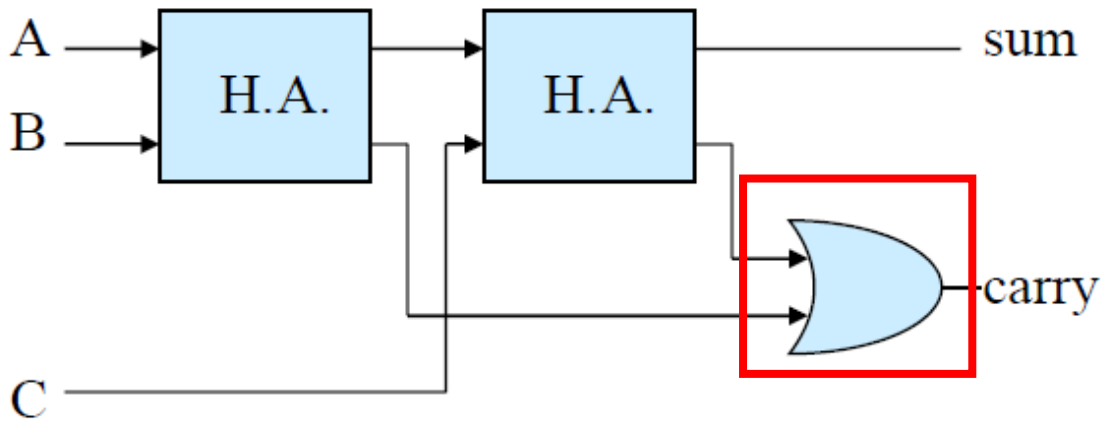


Combinational Building Blocks
2. Adder: Full Adder



Q1: Which of the following gates CAN be placed here?
Q2: Which gate is the BEST choice to be placed here?
A. AND B. OR C. XOR D. NAND

Combinational Building Blocks
2. Adder: Full Adder



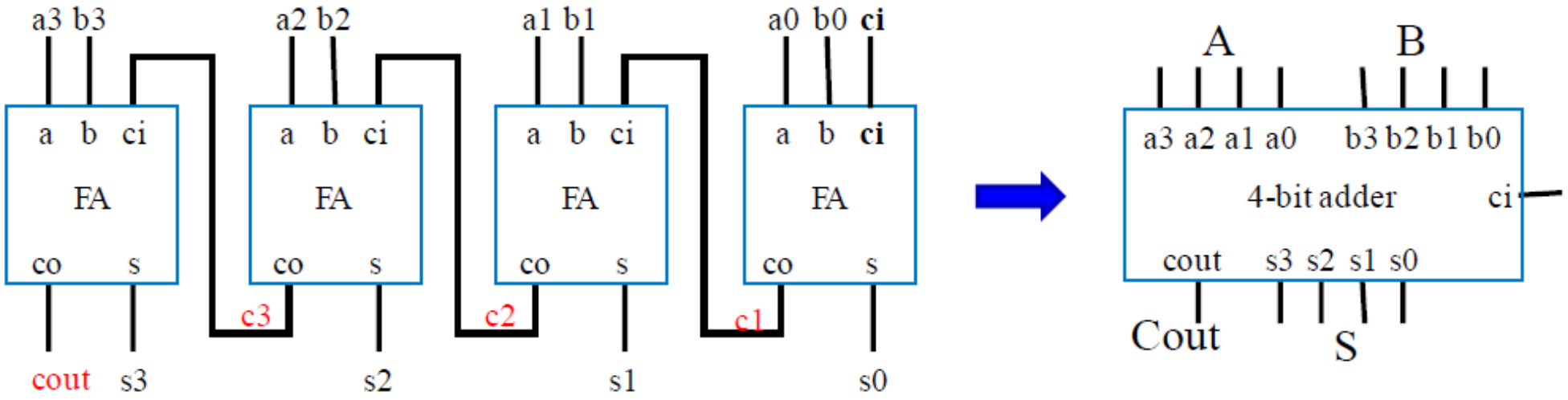
Q1: OR, XOR

Q2: OR is the best.

(4 transistors for OR gate, at least 6 transistors for XOR gate)

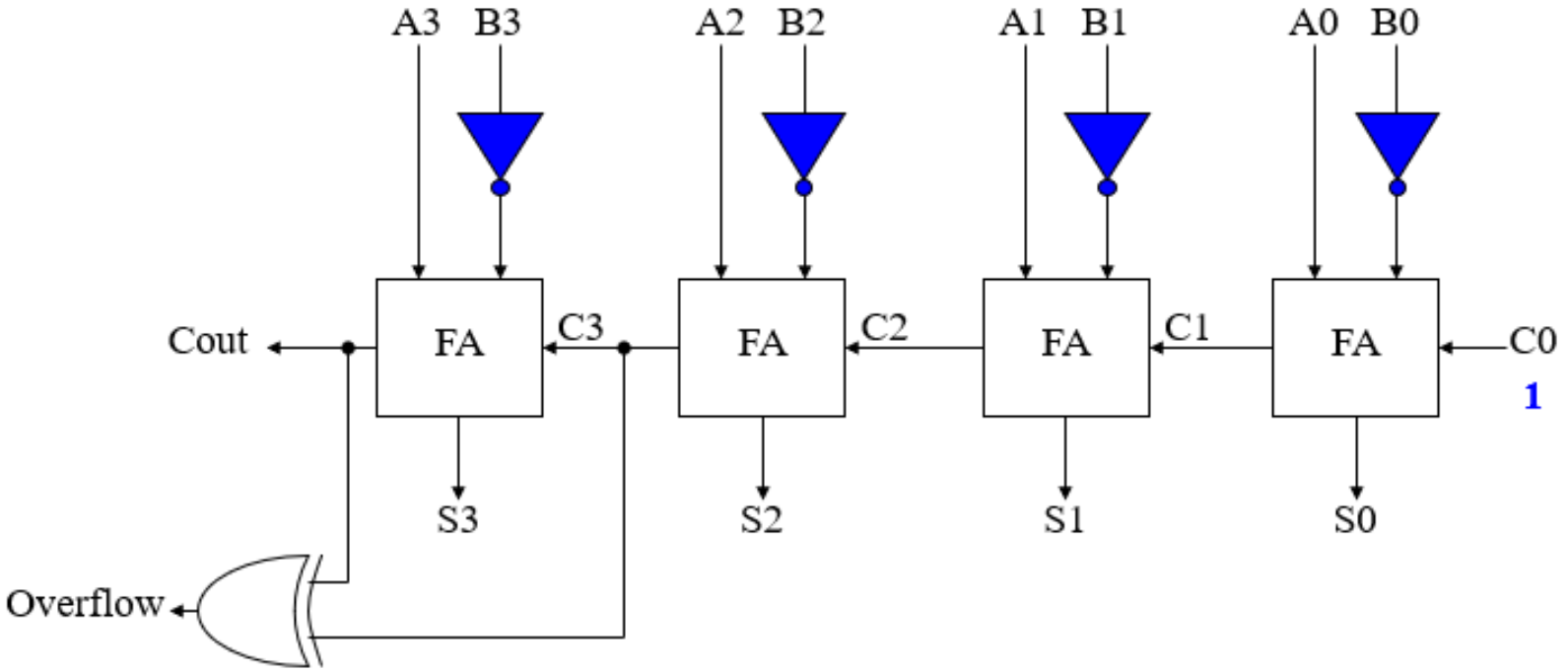
Combinational Building Blocks
2. Adder: Carry-Ripple Adder

- For a carry-ripple adder with 4-bit input, it generates 5-bit output.



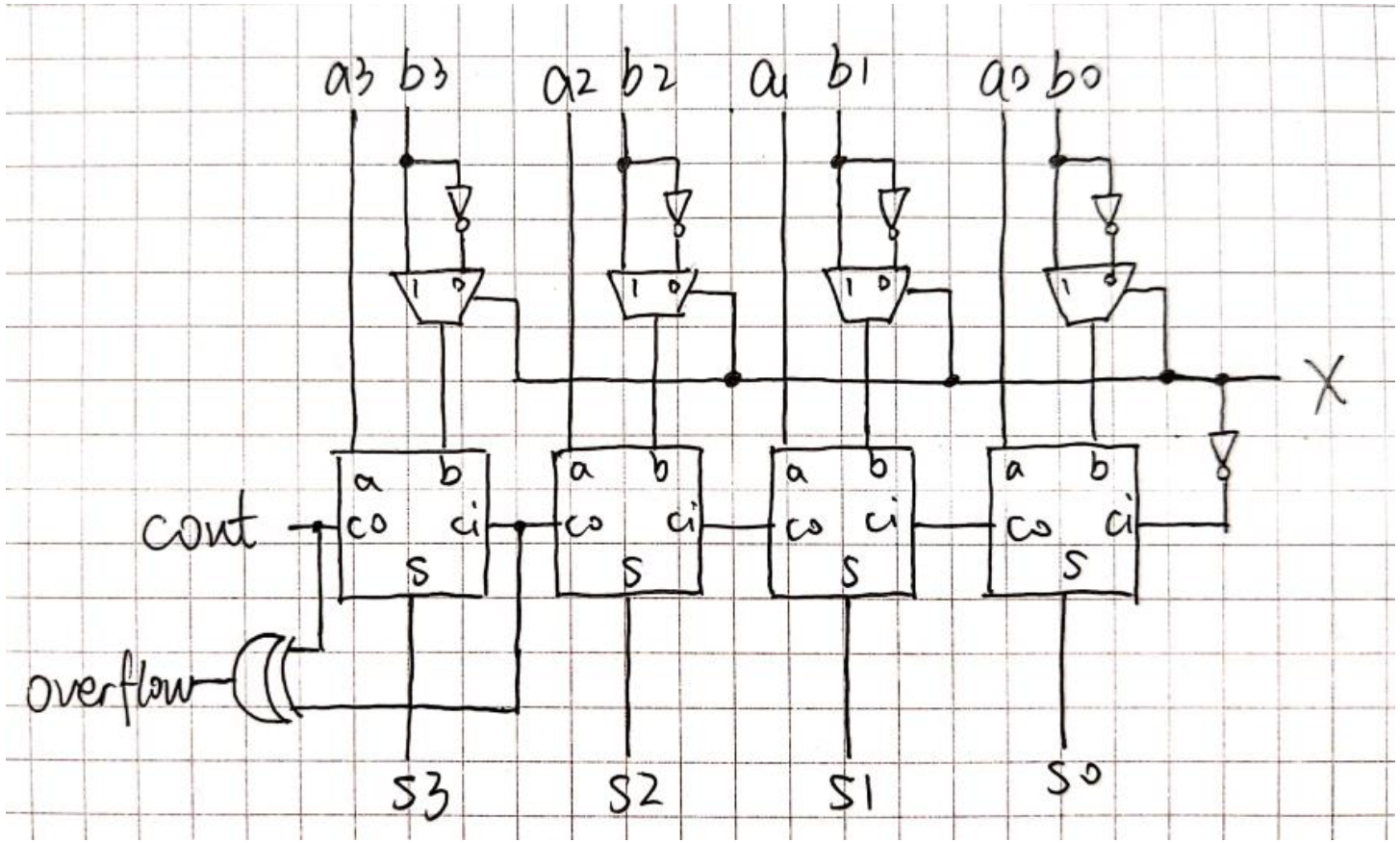
Combinational Building Blocks
2. Adder: Subtractor (for 2's complement numbers)

- When we do subtraction, we need to
- 1. add inverters to B input
- 2. set C0 to 1



Combinational Building Blocks

- Exercise: Add a switch to choose “add” mode or “subtract” mode



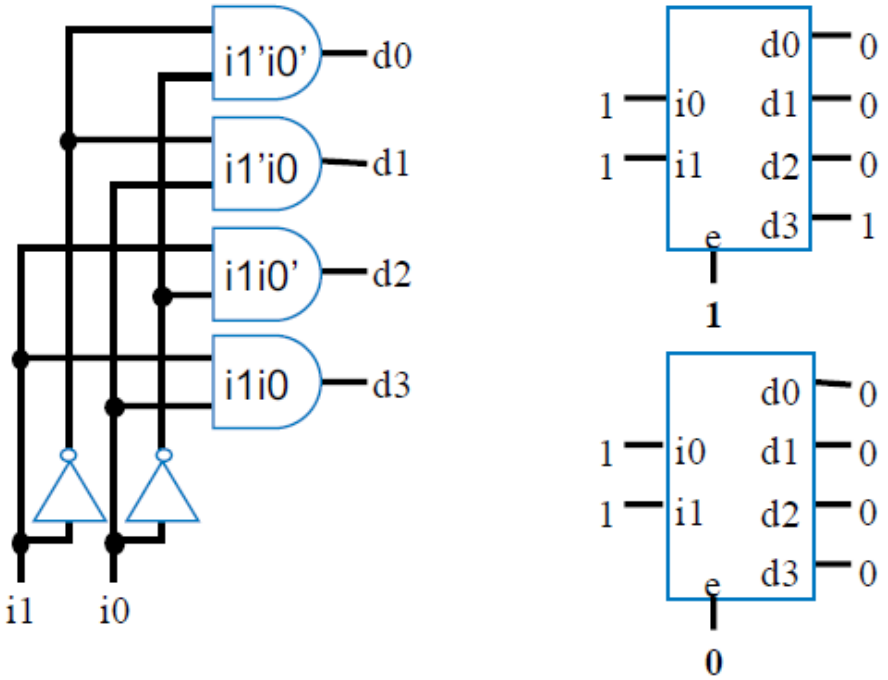
Combinational Building Blocks
3. Encoder & Decoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

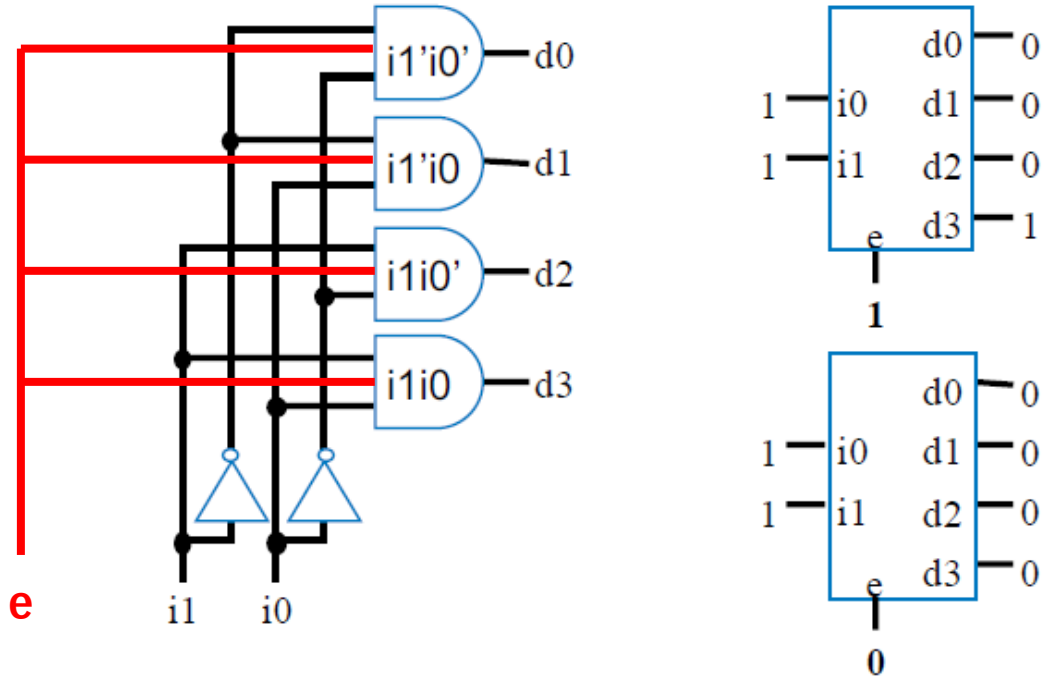
Combinational Building Blocks
3. Encoder & Decoder

- Decoder: N inputs, 2^N outputs
- Enable e (Question: How to implement it in the circuit?)
- Use decoder to implement any combinational circuit



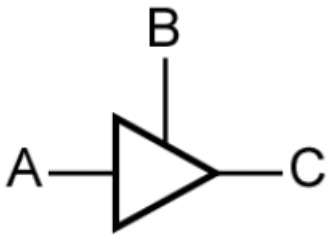
Combinational Building Blocks
3. Encoder & Decoder

- Decoder: N inputs, 2^N outputs
- Enable e (Question: How to implement it in the circuit? – Red lines)
- Use decoder to implement any combinational circuit

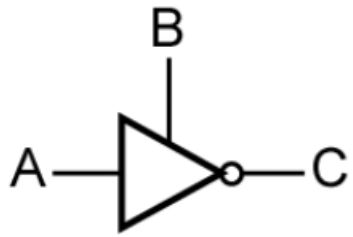


Combinational Building Blocks
4. Buffer & Tri-state Buffer

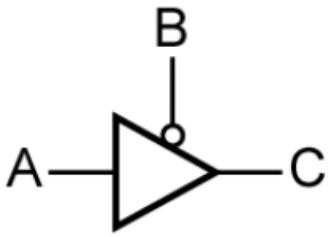
- Why we use buffers?
  - Amplify the driving capability of a signal
  - Insert delay
  - Protect input from output
- Why we use tri-state buffer?
  - Provide another state “Z”
  - Z: high impedence



B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1



B	A	C
0	0	Z
0	1	Z
1	0	1
1	1	0



B	A	C
0	0	0
0	1	1
1	0	Z
1	1	Z

Use the 60 questions to help you review.

60 Questions for VE270 Midterm Exam Review

VE270 2019 Fall TA Group

1. How do digital signals and analog signals look like?

2. How to convert binary numbers to decimal numbers?
   Example: $(1101.011)_2 = (\quad)_{10}$

3. What are the two methods to convert decimal numbers to binary numbers?
   Example: $(19.25)_{10} = (\quad)_2$

4. How to convert among binary numbers, octal numbers, and hexadecimal numbers?

5. How to convert base-m numbers to base-n numbers?