



**Ve270 Introduction to Logic Design**

**Homework 6**

**Assigned: October 29, 2019**

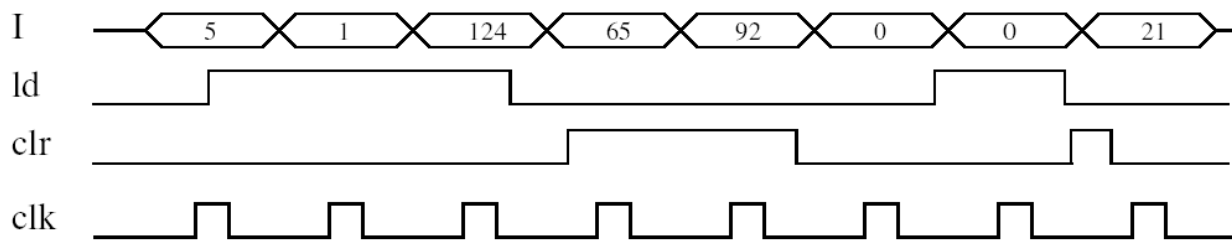
**Due: November 5, 2019, 4:00pm.**

**The homework should be submitted in hard copies.**

1. Problem 4.2 (10 points)

4.2 Trace the behavior of an 8-bit parallel-load register with 8-bit input  $I$ , 8-bit output  $Q$ , load control input  $ld$ , and synchronous clear input  $clr$  by completing the timing diagram in Figure 4.96.

Figure 4.96 is shown below.



2. Problem 4.3, using components to draw schematic (20 points)

4.3 Design a 4-bit register with 2 control inputs  $s1$  and  $s0$ ; 4 data inputs  $I3, I2, I1$ , and  $I0$ ; and 4 data outputs  $Q3, Q2, Q1$ , and  $Q0$ . When  $s1s0=00$ , the register maintains its value. When  $s1s0=01$ , the register loads  $I3...I0$ . When  $s1s0=10$ , the register clears itself to 0000. When  $s1s0=11$ , the register complements itself, so for example, 0000 would become 1111, and 1010 would become 0101. (Component design problem.)

3. Problem 4.45. Draw schematic. (20 Points).

4.45 Design a circuit whose 16-bit output is nine times its 16-bit input  $D$  representing an unsigned binary number. Ignore overflow issues. (Component use problem.)

4. Problem 4.57. Draw schematic (a), (b). (20 points)

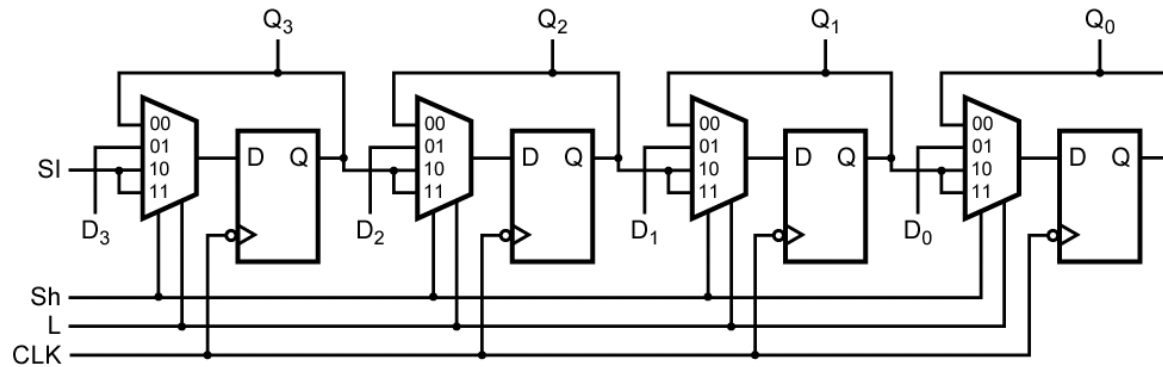
4.57 Design a circuit that outputs a 1 every 99 clock cycles:

- (a) Using an up-counter with a synchronous clear control input, and using extra logic,
- (b) Using a down-counter with parallel load, and using extra logic.

5. Problem 4.59. Draw schematic (10 Points)

4.59 Create a clock divider that converts a 14 MHz clock into a 1 MHz clock. Use a down-counter with parallel load. Clearly indicate the width of the down-counter and the counter's load value. (Component use problem.)

6. Model a Universal Shift Register (shown below) with Verilog. Simulate your design. (20 Points)



Inputs		Action
Sh (Shift)	L (Load)	
0	0	no change
0	1	load
1	X	Shift Right