40 Questions for VE270 Final Exam Review

VE270 2019 Fall TA Group

1. How to design a register with synchronous parallel load?

2. What is register file? What is the input and what is the output?

3. What is shift register? How to implement using D flip flops? How to design using Verilog?

4. What is rotate register? How to implement using D flip flops? How to design using Verilog?

5. How to design a "universal shift register"? What is the input of the universal shift register?

6. What is a shifter? What's the difference between "shifter" and "shift register"?

7. How to implement a shifter? How to design a shifter using Verilog?

8. How to use shifters to do multiplication?
   Example: Using one 4-bit shifter and one 4-bit adder to design a device such that when the input is x, the output is $5x$.

9. How to design a shifter that can shift by any amount?

10. What is FSM? What does an FSM contain?
    Example: In the following FSM, what are 1) set of states; 2) set of inputs & outputs; 3) initial state; 4) set of transitions; 5) set of actions.

11. What are Moore FSM and Mealy FSM? What's the difference?

12. What are the common state transition properties?

13. What is the standard FSM architecture?

14. What are the five steps in FSM design process?

15. How to implement Moore or Mealy FSM using Verilog?

Common FSM optimization techniques include 1) state reduction; 2) implication table; 3) state encoding, etc. Question 16~19 are discussing about FSM optimization.

16. Can you provide an example for state reduction method and perform optimization for your example?

17. What are the four steps in implication table method? Can you provide an example to perform optimization using this method?

18. How to perform optimization using state encoding method? What are the pros and cons of one-hot encoding method?

19. How to "complete" an FSM in which some states are not used?

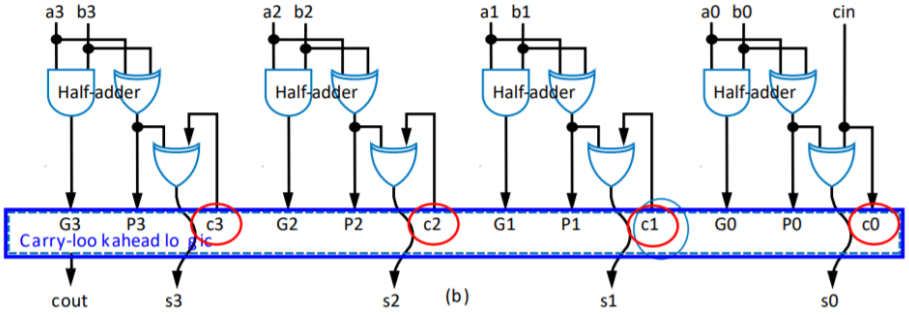
20. Given a circuit of FSM, can you determine: 1) whether it is Moore or Mealy; 2) number of states; 3) logic for next state; 4) its state table; 5) its state diagram?

21. What are the four steps in RTL design? Have you understood all the examples in lecture notes and exercises in your homework?

22. What is a carry-ripple adder? Pros and cons?

23. What is a carry-lookahead adder? Pros and cons?

24. What does P and G mean in a carry-lookahead adder? How to calculate P and G? Example: Give $P0{\sim}P3$ and $G0{\sim}G3$ if we want to calculate $1010 + 0011$.



25. Can you calculate the delay for carry-ripple adder and carry-lookahead adder?

26. How to cascade carry-lookahead adders?

27. How to design a magnitude comparator?

28. How to design a multiplier? What is "array style" and "sequential style" in multiplier design?

29. What is setup/hold time? How to fix setup/hold time violations?

30. What is "metastability"? When will we meet this situation?

31. What does a synchronizer do? What is the common solution to a synchronizer failure?

32. Can you explain the problem of bouncing switch and possible solutions?

33. What is clock skew? Is it good to used a gated clock? What are the common solutions?

34. What is 1) static hazard; 2) dynamic hazard; 3) functional hazard? How to solve?

35. What is RAM? What's the similarity and difference between RAM and register file?

36. What is SRAM and DRAM? Can you briefly describe the design of SRAM or DRAM cell?

37. What is ROM? What are its advantages over RAM? What are the common types of ROM?

38. What is PLA? What is PLA and PAL? What's the difference between PLA and PAL?

39. What is CPLD?

40. What is FPGA? What are the common types of FPGA? Can you briefly describe the internal structure of FPGA? What is CLB and LUT? How to implement a programmable switch? Example: Create a 3-input LUT to implement an AND gate.