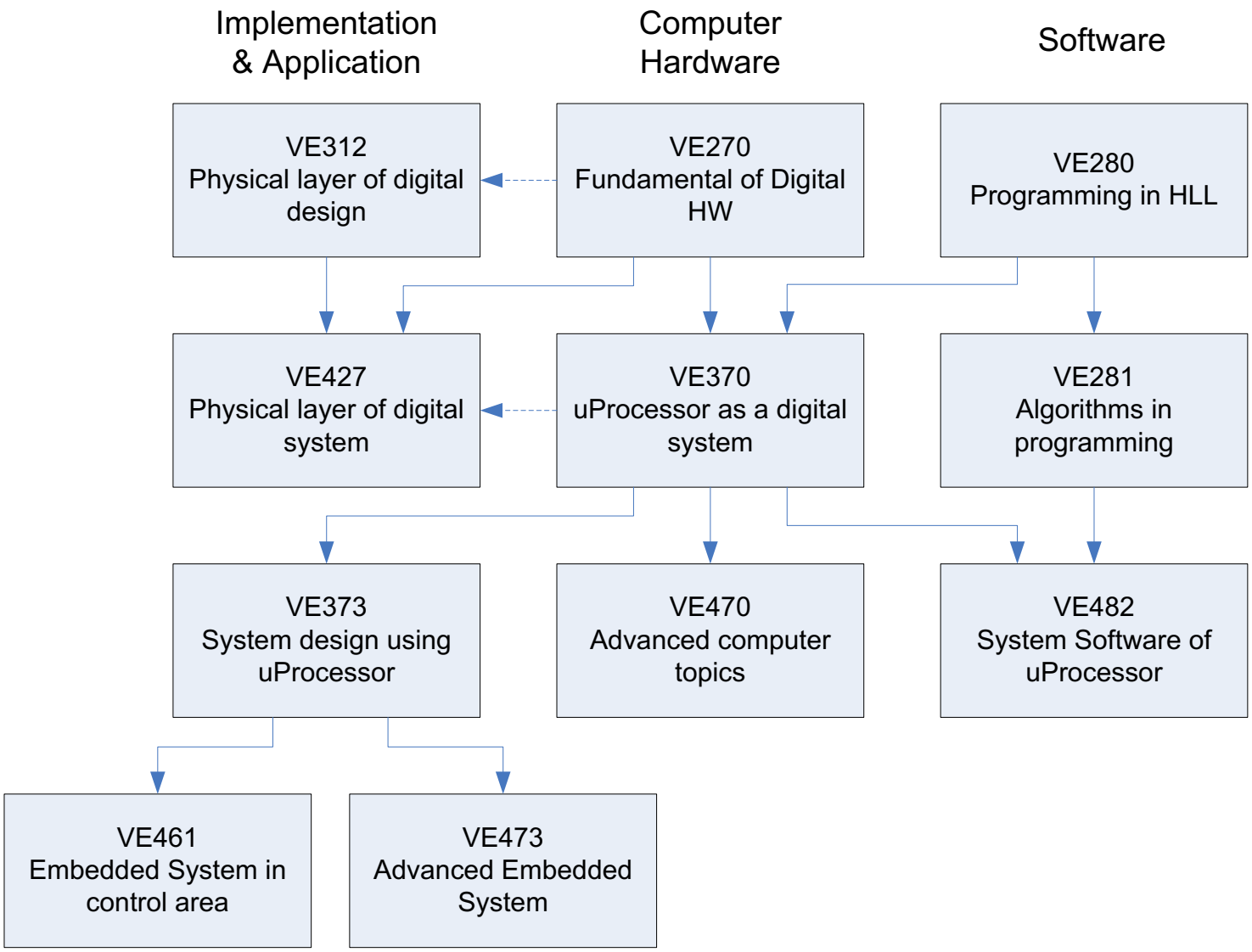
VE270 Intro to Logic Design
Course Overview

Instructional Support

- **My Office:** JI New Building 400E
- **Contact:** gzheng@sjtu.edu.cn
- **Office Hours:** W 4:00-6:00pm / Th 10:00am-12:00pm or by appointment
- **TA:** **Ms. HAO Zhiyu, cathyhaozhiyu@sjtu.edu.cn**
  Ms. SUN Yiwen, sunyw99@sjtu.edu.cn
  Ms. CHEN Yaxin, leepace666666@sjtu.edu.cn
  Mr. SHI Li, shili2017@sjtu.edu.cn

  TAs' office hours to be announced
- **Recitation class:** two identical sessions per week, time to be announced on Canvas

Courses in CE Curriculum



Purpose of the Course

- Understand the fundamental principles in design and implementation of digital logic circuits including combinational circuits, sequential circuits, and finite state machines.
- Develop skills for top-down design and bottom-up verification for digital components and systems.
- Develop skills in using contemporary computer aided tools and programmable logic devices in digital logic design.
- Improve communication skills to effectively function on a team.

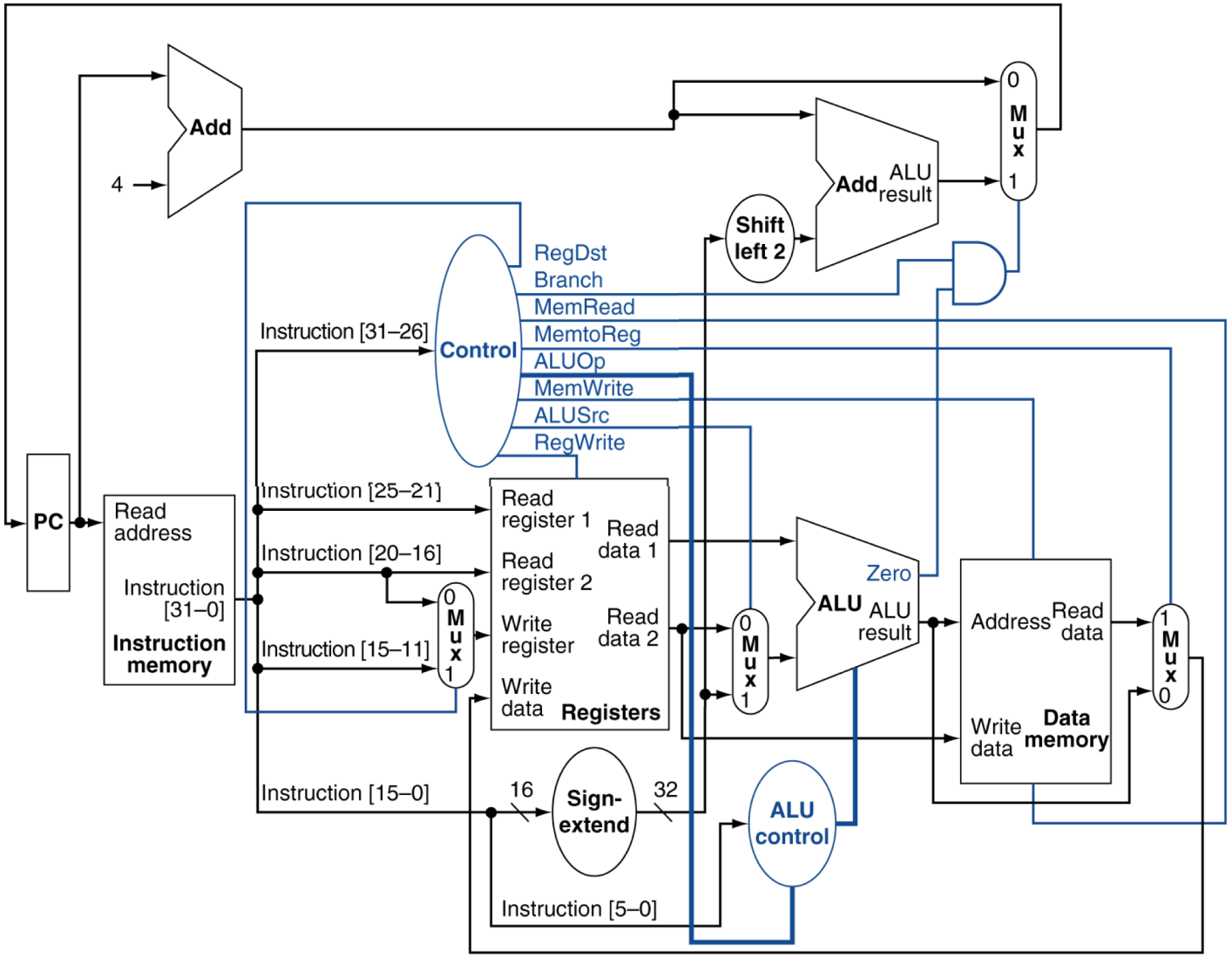
What to Take Away?

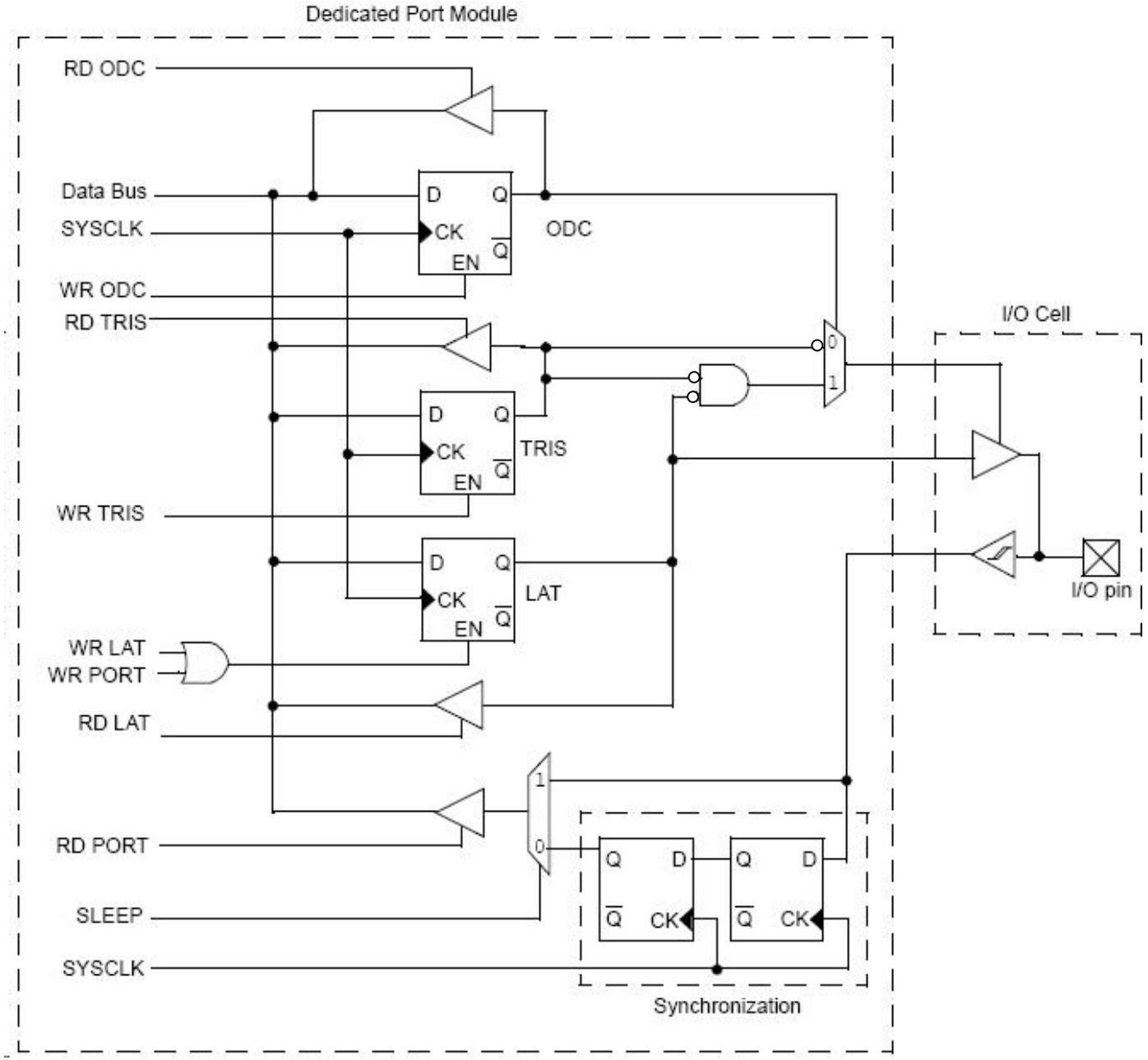
- Ability to perform simple arithmetic in binary, octal, hexadecimal, BCD number systems
- Ability to manipulate logic expressions using binary Boolean algebra.
- Ability to generate the prime implicants of logic functions of 5 or fewer variables using graphical (Karnaugh map) method, and to obtain their minimal two-level implementations with and without don't cares.
- Ability to analyze and synthesize small multi-level combinational logic circuits containing AND, OR, NOT, NAND, NOR, and XOR gates based on simple delay models.
- Ability to use basic functional & timing (clocking) properties of latches & flip-flops.
- Ability to analyze synchronous sequential circuits to extract next-state/output functions

What to Take Away? (Continue)

- Ability to translate a word statement specifying the desired behavior of a simple sequential system into a finite state machine (FSM), to simplify and build the architecture that consists of state register and next state/output logic.
- An ability to implement simple digital systems using controller and basic datapath components such as registers, memories, counters, multiplexers, ALUs, etc.
- Basic knowledge of possible issues and restrictions in digital system.
- Ability to design and test simple digital systems using a hardware description language and CAD tools
- Knowledge of programmable logic devices and ability of implementing a logic circuit in FPGA.
- Experience and communication skills to function on a team.

Seriously, what are we going to learn?




Dedicated Port Module
RD ODC
Data Bus
SYSCLK
WR ODC
RD TRIS
D
Q
CK
EN
ODC
TRIS
WR TRIS
LAT
WR LAT
WR PORT
RD LAT
RD PORT
SLEEP
SYSCLK
I/O Cell
I/O pin
Synchronization

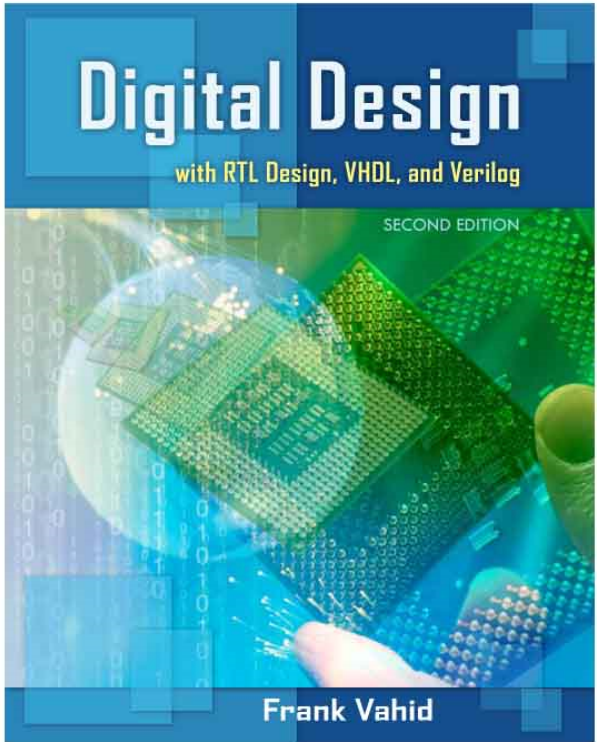
Topics to Cover and Tentative Schedule

- Boolean algebra
- Logic gates
- Combinational circuits
- Flip-flops
- Hardware Description Language (HDL)
- Sequential circuits
- Finite state machine (FSM)
- Circuit optimization
- Arithmetic circuits
- Design skills for digital components
- Computer-aided design
- Memory
- Programmable logic devices

Textbook

- **Textbook:**

  Frank Vahid, *Digital Design 2/e*, John Wiley & Sons, 2010. ISBN 9780470531082



Course Policies

- **Honor Code:** All students in the class are bound by the Honor Code of the Joint Institute (**http://umji.sjtu.edu.cn/academics/academic-integrity/honor-code/**). You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- Testing: The test procedure will be announced prior to the tests. Anyone violating the testing procedure will be given an 'F' for the test.
- Attendance: Attendance will be randomly taken. 5% will be deducted from the final grade for each absence starting from the 4^{th} one.
- Participation: Active participation in course meetings is expected for all students. With each submitted assignment, students should be prepared to explain their solutions to the class.

Course Policies

- Submission: Homework assignments are due on the specified date before the class begins. **No late homework assignments will be accepted**. Lab source files and peer evaluation reports must be uploaded before the Canvas link is deactivated. **Late submission of the lab source files and peer evaluation reports will result in 0 point for the corresponding parts of a lab. No lab grade will be given until all the files are submitted.** The instructor reserves the right to waive the penalty for emergencies (e.g. hospitalization) or arrangement made with the instructor 24 hours prior to the due date.
- Lab Demonstration: Students should successfully demonstrate a working circuit to the TAs before your lab session ends. Late demonstration is acceptable with 20% deduction from the lab grade for each day extended until all the points are deducted.

Course Policies

- Individual Assignments: Students are encouraged to discuss course topics and help each other to understand the homework assignments. However, all submissions must represent your own work. Duplicated submission is not allowed and will trigger an honor code violation investigation.
- Group Assignments: Some assignments will be team efforts. The work submitted must reflect the work of the team.

Assessment Methods

- **Homework & Quiz:**
  - Typically, one homework set is assigned each week and due in the next week.
  - Should always be prepared for taking a pop quiz for each homework assignment, in that case, HW grades will be replaced with quiz grades
  - 9-10 homework assignments (individual assignments), submitted in hard copy at beginning of the class on due date, **no late assignments accepted**
  - Two lowest grades for homework/quizzes will be dropped
- **Examination:**
  - One midterm and one final exam, written exam and paper based
  - Course outcomes are the guidelines for exam problems
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, etc

Assessment Methods

- **Lab Experiment:**
  - Utilize industrial standard hardware/software tools, software provided
  - Demonstration is required for each lab. A team may be randomly quizzed about implementation problems in a lab during the demonstration.
  - Labs will be graded on completeness, correctness, effectiveness in analyzing and presenting lab outcomes, source files and team work.
  - Lab partners will be randomly assigned.
  - 7 lab experiments, 2 students per team, starts from wk#2, switching team not allowed without instructor's permission

Lab Equipment and Software

- **Xilinx Vivado HLx (WebPACK)**

Download for free at:
https://www.xilinx.com/member/forms/download/xef.html?filename=Xilinx_Vivado_SDK_2017.2_0616_1_Win64.exe&akdm=0

(registration needed)

- **NI Multisim**

Download the Education Edition evaluation version for free at:
http://www.ni.com/gate/gb/GB_ACADEMICEVALMULTISIM/US

- **Digilent Basys 3 Xilinx Artix-7 FPGA Training board** (partially sponsored by Digilent Inc.)

Grading Policy

• Homework and Quiz	10%
• Lab	30%
• Midterm Exam	30%
• Final Exam	30%
Total	**100%**

- **Note: final letter grades will be curved**

Lab Grading Policy

- Lab grade components:
  - Demonstration and oral exam: 80% of a lab grade
  - Source File: 10% of a lab grade
  - Peer Evaluation: 10% of a lab grade
- Late demonstration is acceptable with 20% deduction from the lab grade for each day extended until all the 80% are deducted.
- Late submission of source files and peer evaluation report will result in a 0% for those two parts of the lab. A grade for a lab will not be given until source files and peer evaluation reports are submitted.

Lab Grading Policy

- Peer evaluation form

Name	Percentage of contribution (sum to 100%)	Responsibilities
(yourself)		
(your lab partner)		

Some Advices

- This course looks simple, but not necessarily true for everyone
- Attend lectures, I might talk about something useful occasionally
- Having doubts? Interrupt me and ask
- Seek help from the instructor and TAs, make good use of class time and our office hours
- Labs are very important and helpful with learning this subject, start before the lab, lab time might not be enough
- Respect the software, the software will do what's asked to do
- I reward hard working students, I don't mind giving more As; but I cannot give all As; I do fail students if I have to
- We check honor code violations seriously, you don't want to test your luck
- Check Canvas frequently for important announcements