VE270 Final Review
Part III

HAO Zhiyu

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Outline

1. RTL design
2. PG-lookahead adder

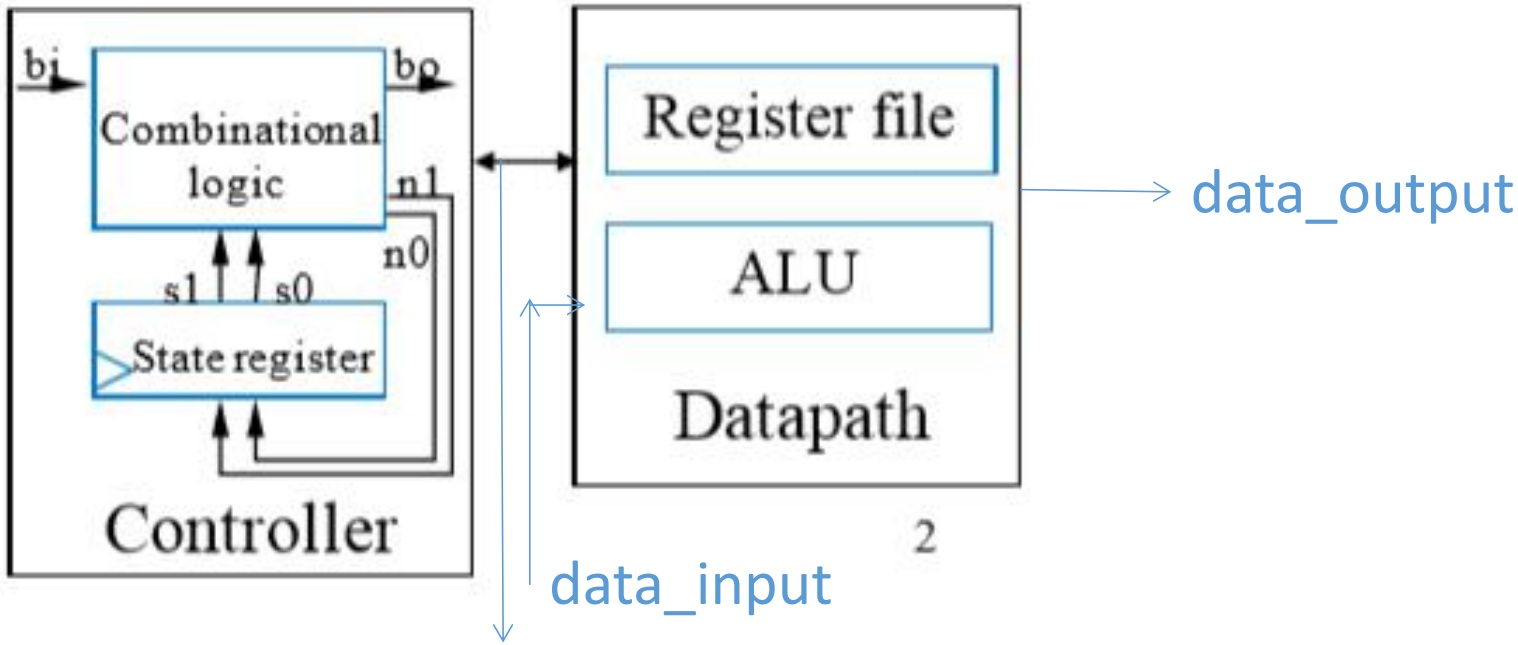
RTL design

- Controllers(FSM):

  produce simple output and control signals for datapath

- Datapath:

  Manipulate the data according to the controllers' command



RTL steps

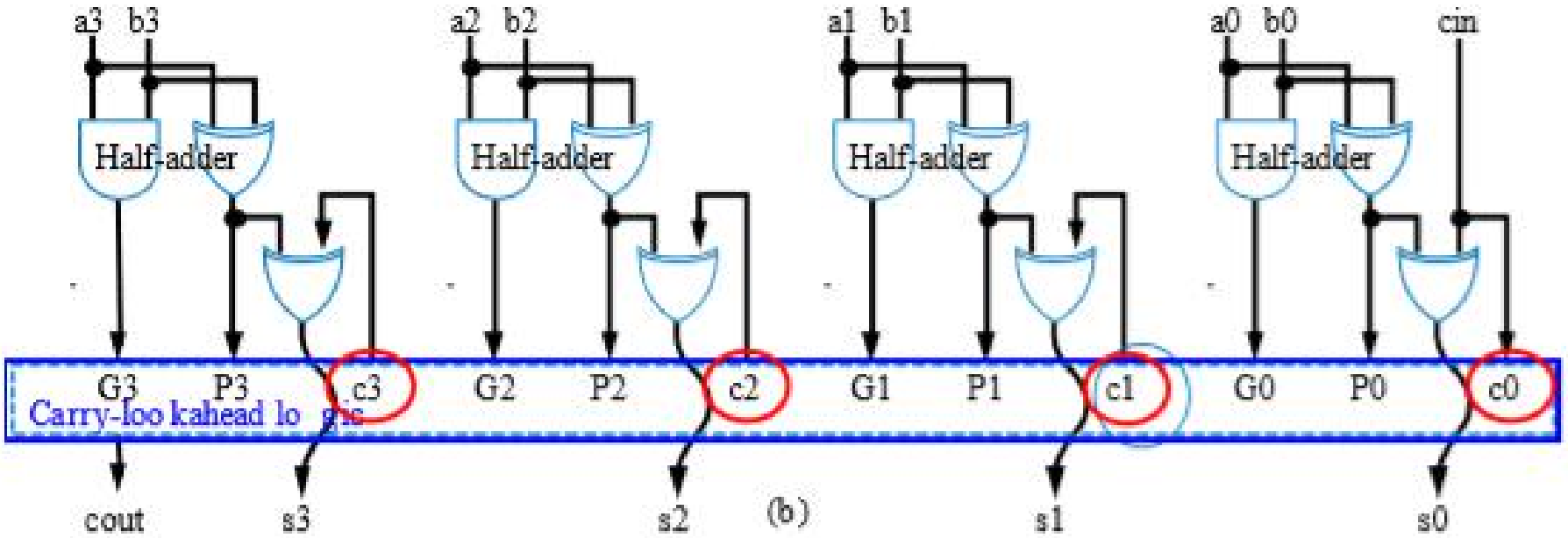
- A high level state machine
- Datapath
- Connect the datapath to a controller
- Derive the (controller) FSM from the high level state machine

PG Lookahead

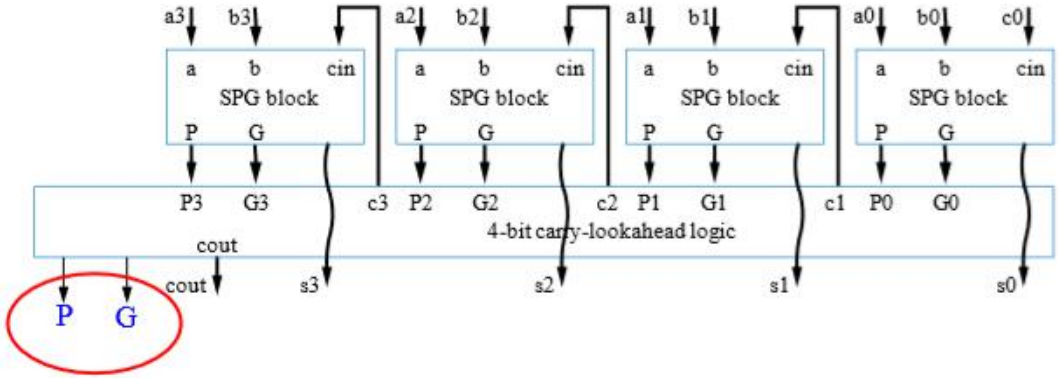
- ***Propagate***: P = a ⊕ b
- ***Generate***: G = ab

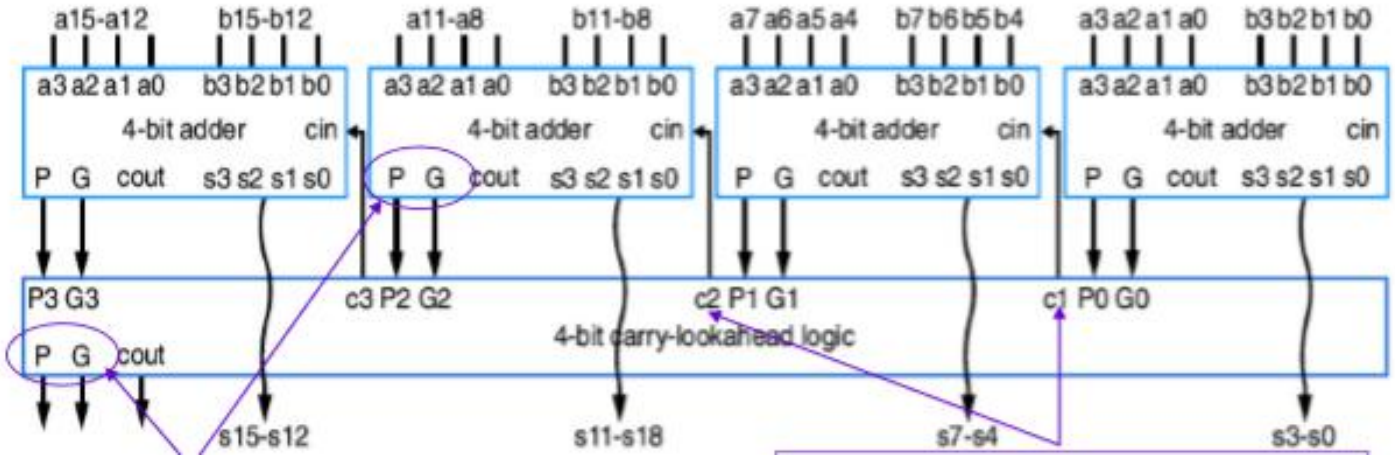
Cout = G + Pc

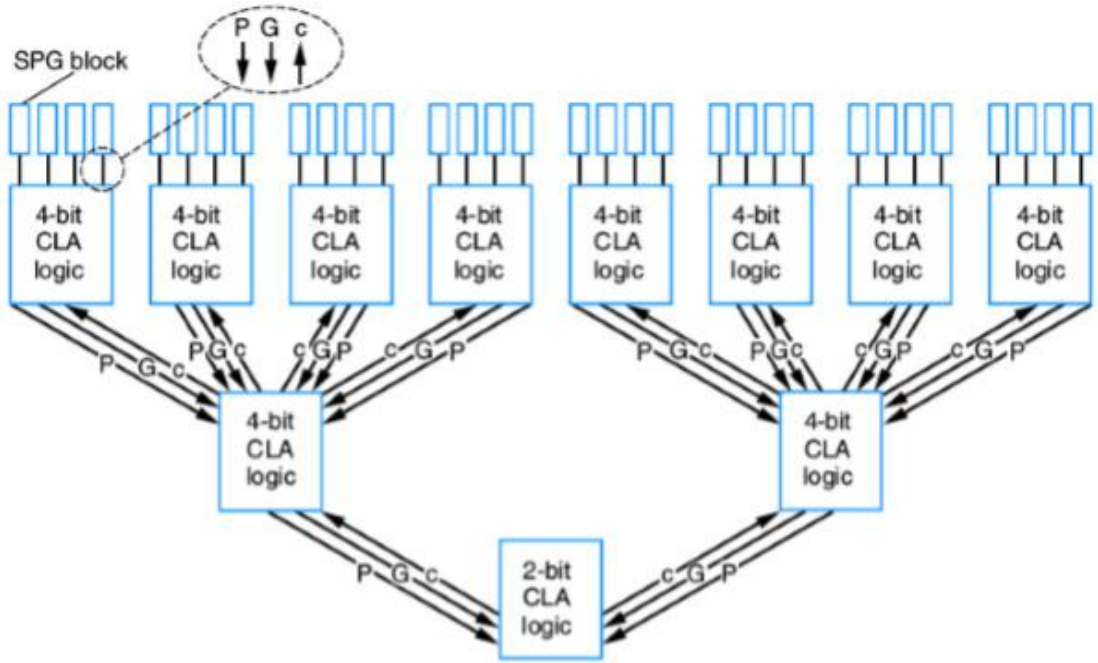
- c1 = a0b0 + (a0⊕b0)c0 = G0 + P0c0
- c2 = a1b1 + (a1⊕b1)c1 = G1 + P1c1
- c3 = a2b2 + (a2⊕b2)c2 = G2 + P2c2



Calculate the delay





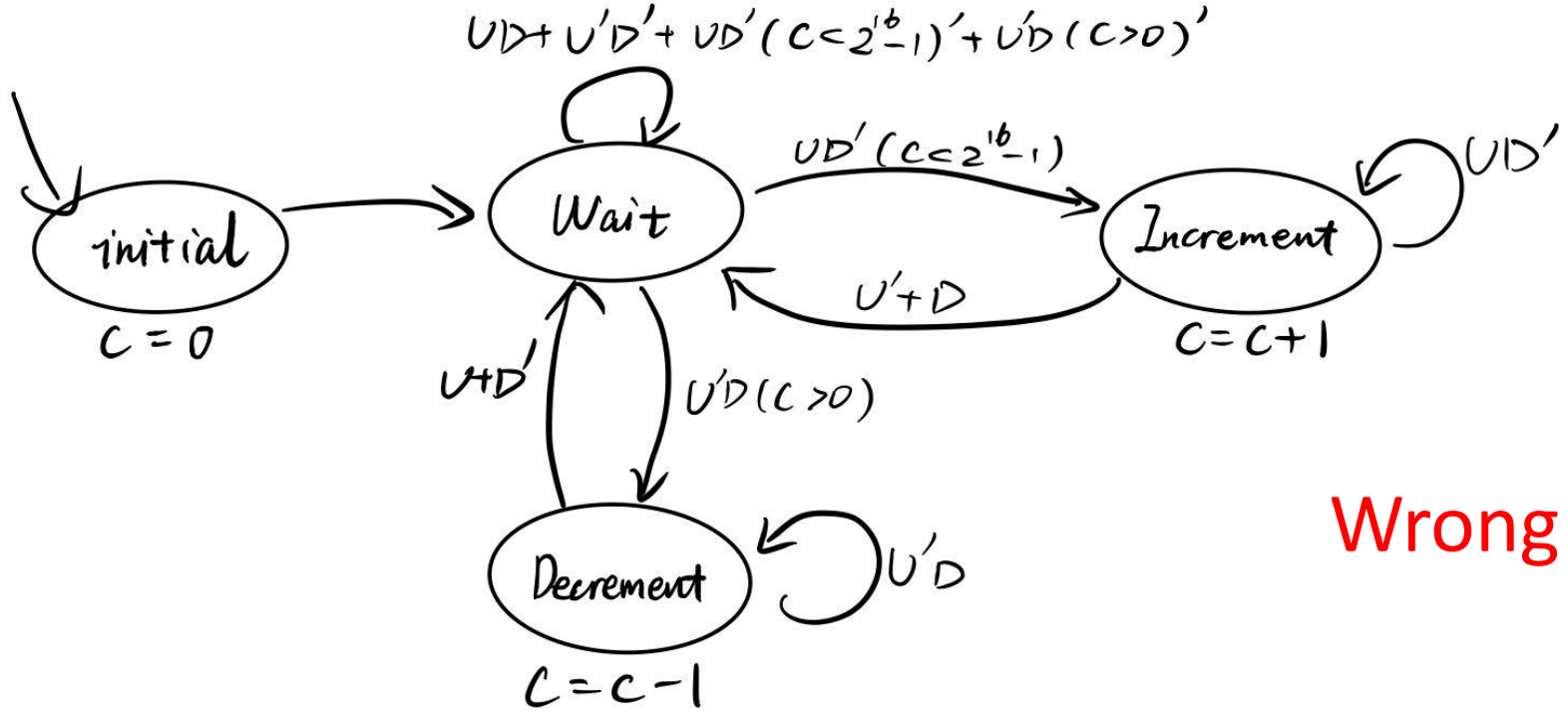


P = P3P2P1P0

G = G3+P3G2+P3P2G1+P3P2P1G0

hw8.3

5.3 Capture the following system behavior as an HLSM. The system has two single-bit inputs U and D each coming from a button, and a 16-bit output C, which is initially 0. For each press of U, the system increments C. For each press of D, the system decrements C. If both buttons are pressed, the system does not change C. The system does not roll over; it goes no higher than than the largest C and no lower than C=0. A press is detected as a change from 0 to 1; the duration of that 1 does not matter.



Wrong！ ！ ！

1. Problem 5.25 (20 points)

hw10

5.25 Assuming an inverter has a delay of 1 ns, and all other gates have a delay of 2 ns, determine the critical path for the 8-bit carry-ripple adder, assuming a design following Figure 4.31 and Figure 4.30, and: (a) assuming wires have no delay, (b) assuming wires have a delay of 1 ns.

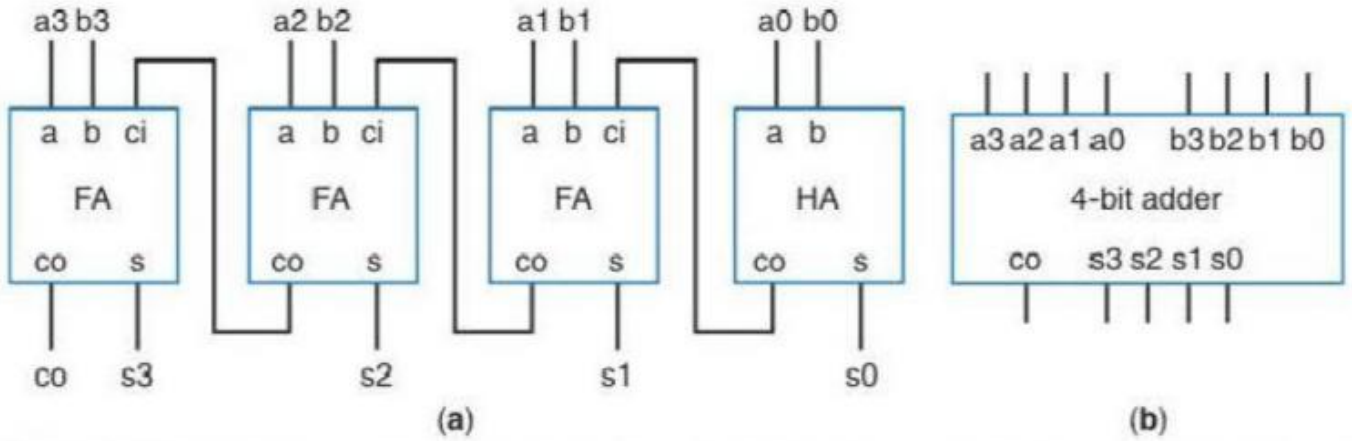


Figure 4.31 4-bit adder: (a) carry-ripple design with 3 full-adders and 1 half-adder, (b) block symbol.

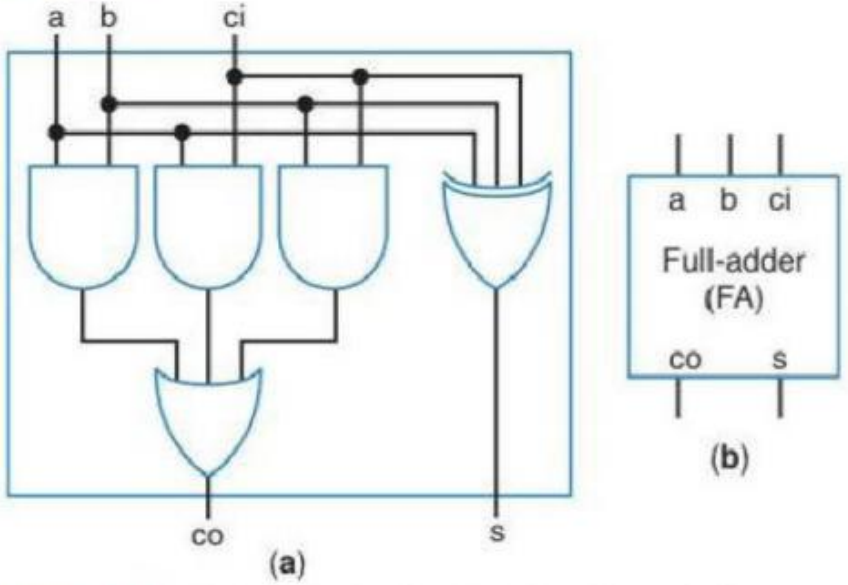


Figure 4.30 Full-adder: (a) circuit, (b) block symbol.

(a) Assume the 8-bit carry-ripple adder consists of 8 full-adders chained together. Each full-adder features a critical path delay of 4ns (an AND gate and a XOR gate). Thus, the total critical path delay for the 8-bit carry-ripple adder is 8*4ns = 32ns.

(b) Each full-adder's critical path features one internal wire between an AND and XOR gate and two wires that connect the full-adder's inputs and outputs. For the entire 8-bit carry-ripple adder, the 8 internal wires contribute 8ns to the critical path delay. Wires connecting full-adders together contribute 7ns to the critical path delay.

The initial ci and final co contribute 2ns to the critical path delay. Thus, the total critical path delay is 32ns (for gates) + 8ns + 7ns + 2ns = 49ns.