Ve270 Introduction to Logic Design

Fall 2019

Instructor: Gang Zheng, Ph.D.
Office: JI New Building 400E
Contact: (021) 3420-6765 x4005, gzheng@sjtu.edu.cn

Office Hours: W 4:00pm – 6:00pm / Th 10:00am – 12:00pm, or by appointment
Classroom: F502
Time: T/Th 4:00 – 5:40pm

TA: Ms. HAO Zhiyu, cathyhaozhiyu@sjtu.edu.cn ,
Ms. SUN Yiwen, sunyw99@sjtu.edu.cn ,
Ms. CHEN Yaxin, leepace666666@sjtu.edu.cn
Mr. SHI Li, shili2017@sjtu.edu.cn

Office Hours: TBD

Course Description:
This course is designed to cover binary and non-binary number systems, Boolean algebra, digital design techniques, logic gates, logic minimization, standard combinational circuits, sequential circuits, flip-flops, synthesis of synchronous sequential circuits, programmable logic devices, ROMs, RAMs, arithmetic circuits, and computer-aided design. Laboratory includes design and implementations of digital circuits and systems as well as CAD experiments.

Credits: 4

Prerequisites: Vg101 or equivalent

Course Objectives:
1) To teach the fundamental principles in design and implementation of digital logic circuits including combinational circuits, sequential circuits, and finite state machines.
2) To develop skills in top-down design and bottom-up verification for digital components and systems.
3) To provide hands-on experience with computer aided design tools and programmable logic devices in digital logic design.
4) To improve communication skills to effectively function on a team.

Course Outcomes:
1) Ability to perform simple arithmetic in binary, octal, hexadecimal, BCD number systems
2) Ability to manipulate logic expressions using binary Boolean algebra.
3) Ability to generate the prime implicants of logic functions of 5 or fewer variables using graphical (Karnaugh map) method, and to obtain their minimal two-level implementations with and without don't cares.
4) Ability to analyze and synthesize small multi-level combinational logic circuits containing AND, OR, NOT, NAND, NOR, and XOR gates based on simple delay models.
5) Ability to use basic functional & timing (clocking) properties of latches & flip-flops.

6) Ability to analyze synchronous sequential circuits to extract next-state/output functions
7) Ability to translate a word statement specifying the desired behavior of a simple sequential system into a finite state machine (FSM), to simplify and build the architecture that consists of state register and next state/output logic.
8) An ability to implement simple digital systems using controller and basic datapath components such as registers, memories, counters, multiplexers, ALUs, etc.
9) Basic knowledge of possible issues and restrictions in digital system.
10) Ability to design and test simple digital systems using a hardware description language and CAD tools
11) Knowledge of programmable logic devices and ability of implementing a logic circuit in FPGA.
12) Experience and communication skills to function on a team.

Textbook:

Frank Vahid, *Digital Design 2/e*, John Wiley & Sons, 2010. ISBN 9780470531082

Course Policies:

- **Honor Code:** All students in the class are bound by the Honor Code of the Joint Institute (http://umji.sjtu.edu.cn/academics/academic-integrity/honor-code/). You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- Test: Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- Attendance: Attendance will be randomly taken. 5% will be deducted from the final grade for each absence starting from the 4th one.
- Participation: Active participation in course meetings is expected for all students. With each submitted assignment, students should be prepared to explain their solutions to the class.
- Submission: Homework assignments are due on the specified date before the class begins. **No late homework assignments will be accepted**. Lab source files and peer evaluation reports must be uploaded before the Canvas link is deactivated. **Late submission of the lab source files and peer evaluation reports will result in 0 point for the corresponding parts of a lab. No lab grade will be given until all the files are submitted.** The instructor reserves the right to waive the penalty for emergencies (e.g. hospitalization) or arrangement made with the instructor 24 hours prior to the due date.
- Lab Demonstration: Students should successfully demonstrate a working circuit to the TAs before your lab session ends. **Late demonstration is acceptable with 20% deduction from the lab grade for each day extended until all the points are deducted.**
- Individual Assignments: Students are encouraged to discuss course topics and help each other to understand the homework assignments. However, all submissions must represent your own work. Duplicated submission is not allowed and will trigger an honor code violation investigation.
- Group Assignments: Some assignments will be team efforts. The work submitted must reflect the work of the team.

Course Outline: *Tentative and subject to change.*

Week	Dates	Topics	Reading
1	9/10	Course introduction, introduction to logic design	1.1 – 1.3, 2.1 – 2.4, 2.8
	9/12	Number systems, basic logic gates, truth table	
2	9/17	Representation of Boolean functions (Lab 1, 1 week)	2.5, 2.6
	9/19	Logic optimization and K-map	6.1, 6.2
3	9/24	Combinational building blocks (Lab 2, 2 weeks)	2.7, 2.9, 2.10
	9/26	Combinational building blocks	2.7, 2.9, 2.10
4	10/1	**National Holiday, no class**	
	10/3	**National Holiday, no class**	
5	10/8	Latches, Flip-Flops	3.2
	10/10	Hardware Description Language	9 & Notes
6	10/15	Hardware Description Language (Lab 3, 1 week)	9 & Notes
	10/17	Counters	4.6 – 4.8
7	10/22	Registers and shifters (Lab 4, 1 week)	4.1 – 4.5
	10/24	**Midterm Exam**	
8	10/29	FSM and controllers (Lab 5, 2 weeks)	3.3 – 3.4
	10/31	FSM and controllers	3.3 – 3.4
9	11/5	FSM optimizations and tradeoffs	6.3
	11/7	FSM optimizations and tradeoffs	6.3
10	11/12	RTL design and examples (Lab 6, 2 weeks)	5.1 – 5.5
	11/14	RTL design and examples	5.1 – 5.5
11	11/19	Arithmetic components	4.9 – 4.10
	11/21	Arithmetic components	4.9 – 4.10
12	11/26	Timing issues (Lab 7, 2 weeks)	Lecture Notes
	11/28	Memory Components	5.7
13	12/3	Programmable Logic Devices	Lecture Notes
	12/5	*Advanced Topics (if time allows)*	
14		**Final Exam**	

Course Assessment Methods:

Homework & Quiz:
Homework & quiz problems are designed for students to revisit the important concepts in design and analysis of logic circuits they have learned in preceding lectures, and for the instructor to ensure the appropriate delivery and comprehension of important knowledge. Homework & quiz are also assigned for students to gain confidence in engineering problem solving skills on the circuitry, component, and system levels. Typically, one homework set is assigned each week and due in the next week. Students should always be prepared for taking a pop quiz for each homework assignment. In that case, grade of that homework set will be replaced with the grade of the quiz. Two lowest grades for homework/quizzes will be dropped.

Examination:
The examinations are to measure the level of achievement of the Course Outcomes. Examinations are written and paper based. Requirements of the examinations will be announced prior to the exams. The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis, design, etc.

Lab Experiment:
The labs are designed for students to practice basic understanding of various logic components and logic operations, and to give multiple ways to meet the design requirements. In addition, the labs utilize contemporary software tools in aid of the design projects. Demonstration is required for each lab. A team may be randomly quizzed about implementation problems in a lab during the demonstration. Labs will be graded on completeness, correctness, effectiveness in analyzing and presenting lab outcomes, source files and team work. Lab partners will be randomly assigned.

Special Facilities, Equipment, and Materials Utilized

- Xilinx Vivado HLx (WebPACK)
  Download for free at:
  https://www.xilinx.com/member/forms/download/xef.html?filename=Xilinx_Vivado_SDK_2017.2_0616_1_Win64.exe&akdm=0
  (registration needed)
- NI Multisim
  Download the Education Edition evaluation version for free at:
  http://www.ni.com/gate/gb/GB_ACADEMICEVALMULTISIM/US
- Digilent Basys 3 Xilinx Artix-7 FPGA Training board (partially sponsored by Digilent Inc.)

Grading Policy:

Homework and Quiz	10%
Lab	30%
Midterm Exam	30%
Final Exam	30%
Total	**100%**

Note: final letter grades will be curved.

Lab grading policy:

Demonstration and oral examination	80% of lab grade
Source File	10% of lab grade
Peer Evaluation	10% of lab grade

Late demonstration is acceptable with 20% deduction from the lab grade for each day extended until all the 80% are deducted. Late submission of source files and peer evaluation report will result in a 0% for those two parts of the lab. A grade for a lab will not be given until source files and peer evaluation reports are submitted.